SRI INDU COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

LAB MANUAL

ON

R20ECE21L1:ELECTRONIC DEVICES AND CIRCUITS LAB

II B. TECH I SEMESTER

R20ECE21L1: ELECTRONIC DEVICES AND CIRCUITS LAB

B.Tech. II Year I Sem.   **L T P C**
                                                             0 0 2 1

List of Experiments (Twelve experiments to be done):

Verify any twelve experiments in H/W Laboratory

1. PN Junction diode characteristics A) Forward bias B) Reverse bias.

2. Zener diode characteristics and Zener as voltage Regulator

3. Full Wave Rectifier with & without filters

4. Input and output characteristics of BJT in CE Configuration

5. Input and output characteristics of FE in CS Configuration

6. Common Emitter Amplifier Characteristics

7. Common Base Amplifier Characteristics

8. Common Source amplifier Characteristics

9. Measurement of h-parameters of transistor in CB, CE, CC configurations

10. Switching characteristics of a transistor

11. SCR Characteristics.

12. Types of Clippers at different reference voltages

13. Types of Clampers at different reference voltages

14. The steady state output waveform of clampers for a square wave input

Major Equipment required for Laboratories:

1. Regulated Power Suppliers, 0-30V

2. 20 MHz, Dual Channel Cathode Ray Oscilloscopes.

3. Functions Generators-Sine and Square wave signals

4. Multimeters

5. Electronic Components

Experiment-1
PN Junction diode characteristics A) Forward bias B) Reverse bias

**AIM**: 1. To plot Volt-Ampere Characteristics P-N Junction Diode.

APPARATUS:

S.No	Name of the Apparatus	Range	Quantity
1	Diodes IN 4007 (Ge and Si)		1
2	Resistors	1KΩ, 100Ω	1
3	Regulated Power Supply	(0-30)V DC	1
4	Bread Board		1
5	Digital Ammeter	(0-200)μA/(0-200)mA	1
6	Digital Voltmeter	(0-20)V DC	1
7	Connecting Wires	As Required	

THEORY:-

A p-n junction diode conducts only in one direction. The V-I characteristics of the diode are curve between voltage across the diode and current through the diode. When external voltage is zero, circuit is open and the potential barrier does not allow the current to flow. Therefore, the circuit current is zero. When P-type (Anode is connected to +ve terminal and n- type (cathode) is connected to –ve terminal of the supply voltage, is known as forward bias. The potential barrier is reduced when diode is in the forward biased condition. At some forward voltage, the potential barrier altogether eliminated and current starts flowing through the diode and also in the circuit. The diode is said to be in ON state. The current increases with increasing forward voltage.

When N-type (cathode) is connected to +ve terminal and P-type (Anode) is connected to –ve terminal of the supply voltage is known as reverse bias and the potential barrier across the junction increases. Therefore, the junction resistance becomes very high and a very small current (reverse saturation current) flows in the circuit. The diode is said to be in OFF state. The reverse bias current due to minority charge carriers.

CIRCUIT DIAGRAM:

(i)   FORWARD BIAS:
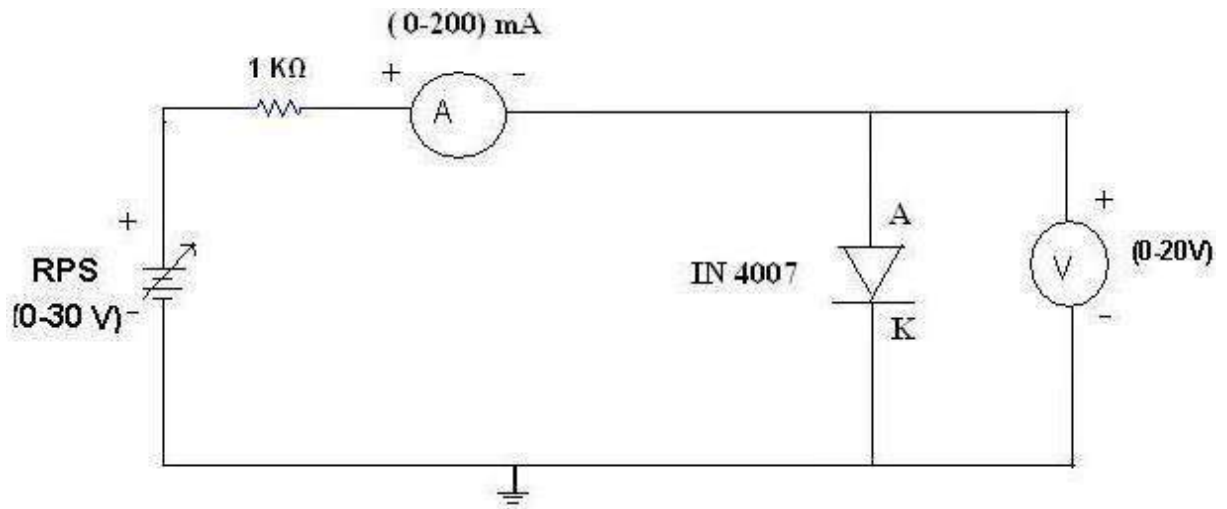
(ii)   REVERSE BIAS:
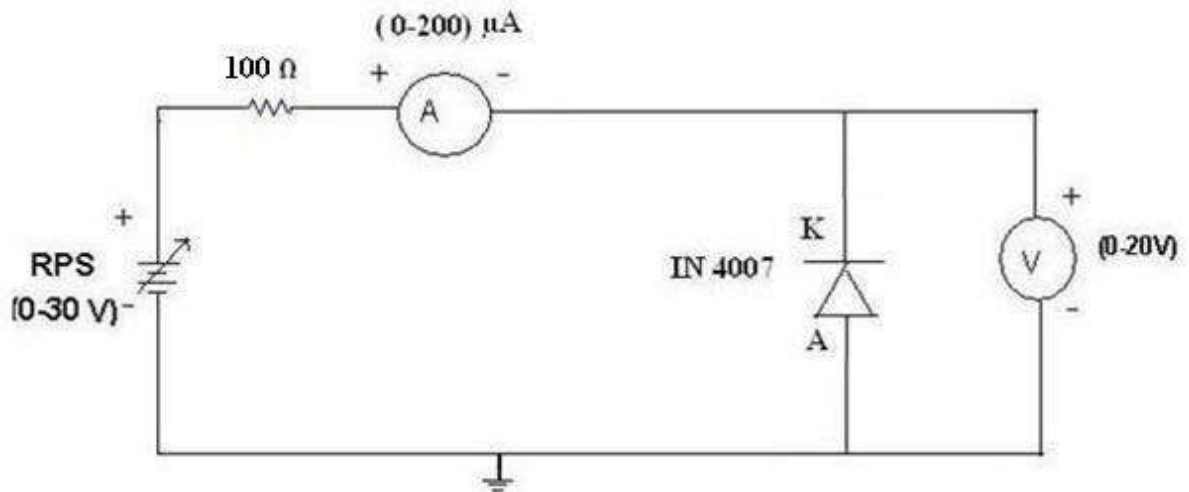
V-I CHARACTERISTICS:
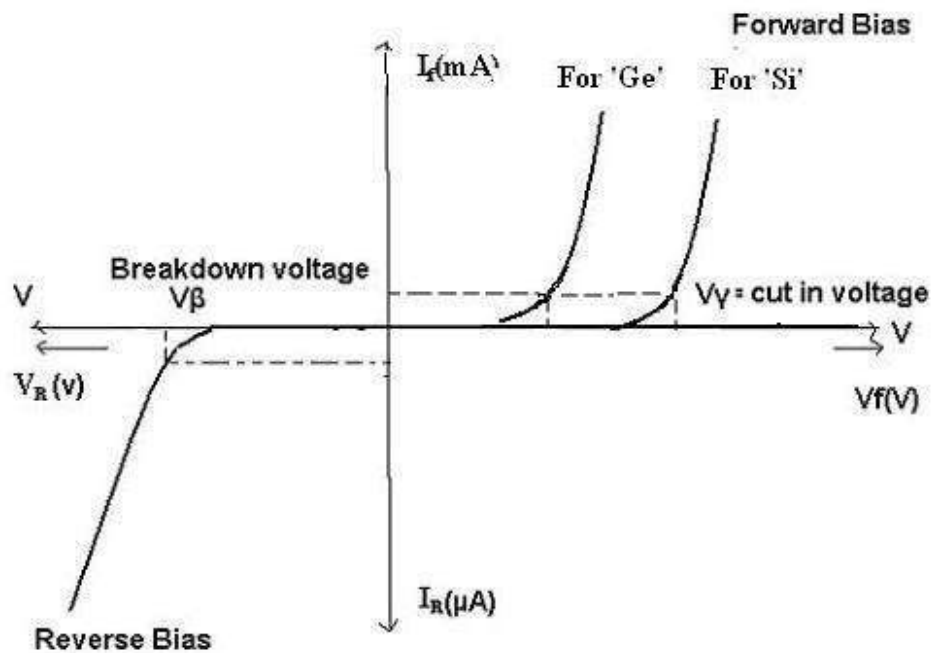
PROCEDURE:

(i) FORWARD BIAS (For 'Ge' and 'Si' Diode):

1. Connections are made as per the circuit diagram.

2. For forward bias, the RPS +ve is connected to the anode of the diode and RPS –ve is connected to the cathode of the diode,

3. Switch ON the power supply and increases the input voltage (supply voltage) in Steps.

4. Note down the corresponding current flowing through the diode and voltage across the diode for each and every step of the input voltage.

5. The readings of voltage and current are tabulated.

6. Graph is plotted between voltage on x-axis and current on y-axis.

OBSERVATIONS:

Forward Bias:

S.No.	Applied voltage (volts)	Voltage across Diode (volts)	Current through Diode (mA)

PROCEDURE:

(ii) REVERSE BIAS :

1. Connections are made as per the circuit diagram.

2. For reverse bias, the RPS +ve is connected to the cathode of the diode and RPS –ve is connected to the anode of the diode.

3. Switch ON the power supply and increase the input voltage (supply voltage) in Steps.

4. Note down the corresponding current flowing through the diode and voltage across the diode for each and every step of the input voltage.

5. The readings of voltage and current are tabulated.

6. The Graph is plotted between voltage on x-axis and current on y-axis.

OBSERVATIONS:

REVERSE BIAS

S.No.	Applied voltage (volts)	Voltage across Diode (volts)	Current through Diode (µA)

PRECAUTIONS:

1. While doing the experiment do not exceed the ratings of the diode. This may lead to damage the diode.

2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.

3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.

RESULT: The Forward and Reverse Bias characteristics for a p-n diode are observed

Experiment-2
## Zener diode characteristics and Zener as voltage Regulator

AIM: 1. To observe and draw the V-I characteristics and Regulation characteristics of a

Zener diode.

2. To find the Zener Break down voltage in reverse biased condition.

APPARATUS*:*

S.No	Name of the Apparatus	Range	Quantity
1	Zener Diode (IN 4735A)		1
2	Resistors	1KΩ, 10KΩ	1
3	Regulated Power Supply	(0-30)V DC	1
4	Bread Board		1
5	Digital Ammeter	(0-200)mA	1
6	Digital Voltmeter	(0-20)V DC	1
7	Connecting Wires	As Required	

CIRCUIT DIAGRAM:

(i) V-I CHARACTERISTICS:
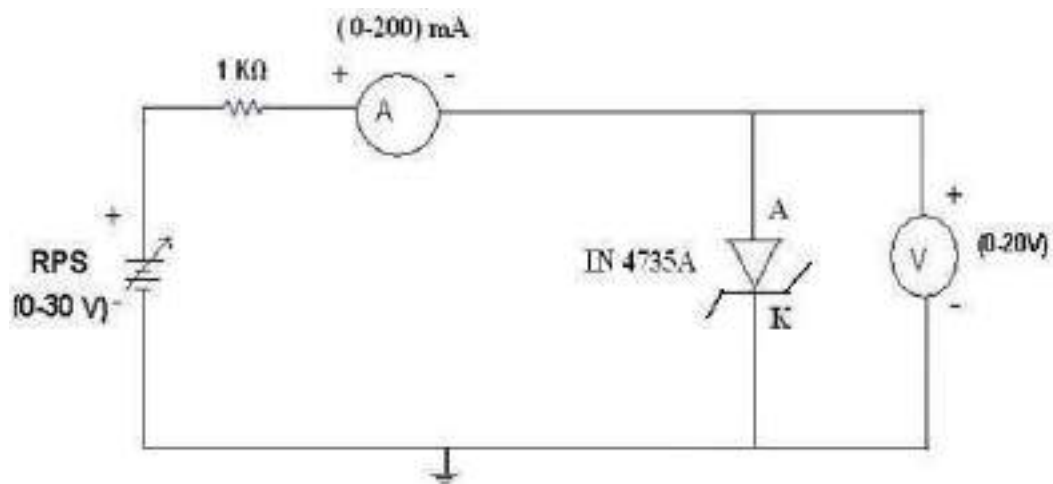
(ii) REGULATION CHARACTERISTICS:
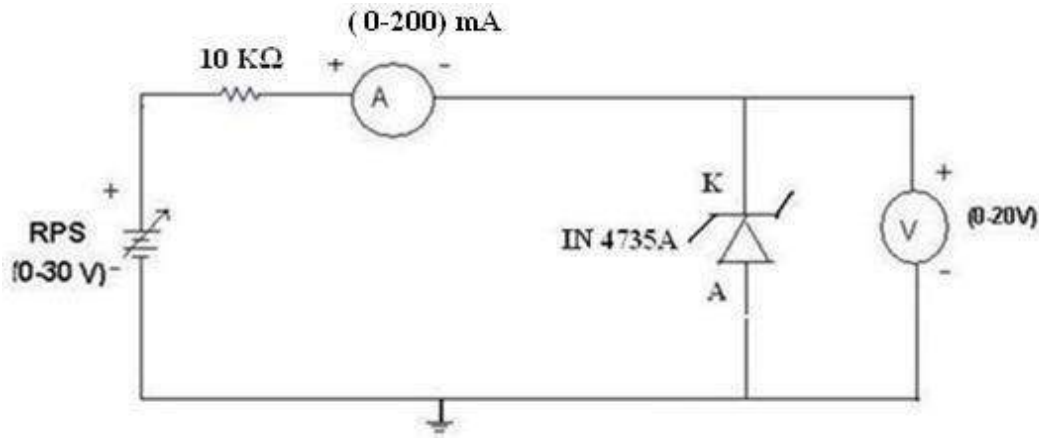
THEORY:

      A zener diode is heavily doped p-n junction diode, specially made to operate in the break down region. A p-n junction diode normally does not conduct when reverse biased. But if the reverse bias is increased, at a particular voltage it starts conducting heavily. This voltage is called Break down Voltage. High current through the diode can permanently damage the device

      To avoid high current, we connect a resistor in series with zener diode. Once the diode starts conducting it maintains almost constant voltage across the terminals what ever may be the current through it, i.e., it has very low dynamic resistance. It is used in voltage regulators.

PROCEDURE:

(i) V-I CHARACTERISTICS:

1. Connections are made as per the circuit diagram.

2. The Regulated power supply voltage is increased in steps.

3. The zener current (lz), and the zener voltage (Vz.) are observed and then noted in the tabular form.

4. A graph is plotted between zener current (Iz) on y-axis and zener voltage (Vz) on x-axis.

(ii) REGULATION CHARACTERISTICS:

1. Connections are made as per the circuit diagram.

2. The Regulated power supply voltage is increased in steps.

3. The voltage across the diode (Vz.) remains almost constant although the current through the diode increases. This voltage serves as reference voltage.

4. The zener current (lz), and the zener voltage (Vz.) are observed and then noted in the tabular form.

4. A graph is plotted between zener current (Iz) on y-axis and zener voltage (Vz) on x-axis.

OBSERVATIONS:

(i) V-I CHARACTERISTICS:

S.No	Zener Voltage (Vz) (volts)	Zener Current (Iz) (mA)

(ii) REGULATION CHARACTERISTICS:

S.No	Zener Voltage (Vz) (volts)	Zener Current (Iz) (mA)

<u>**V-I & REGULATION CHARACTERISTICS**</u>:
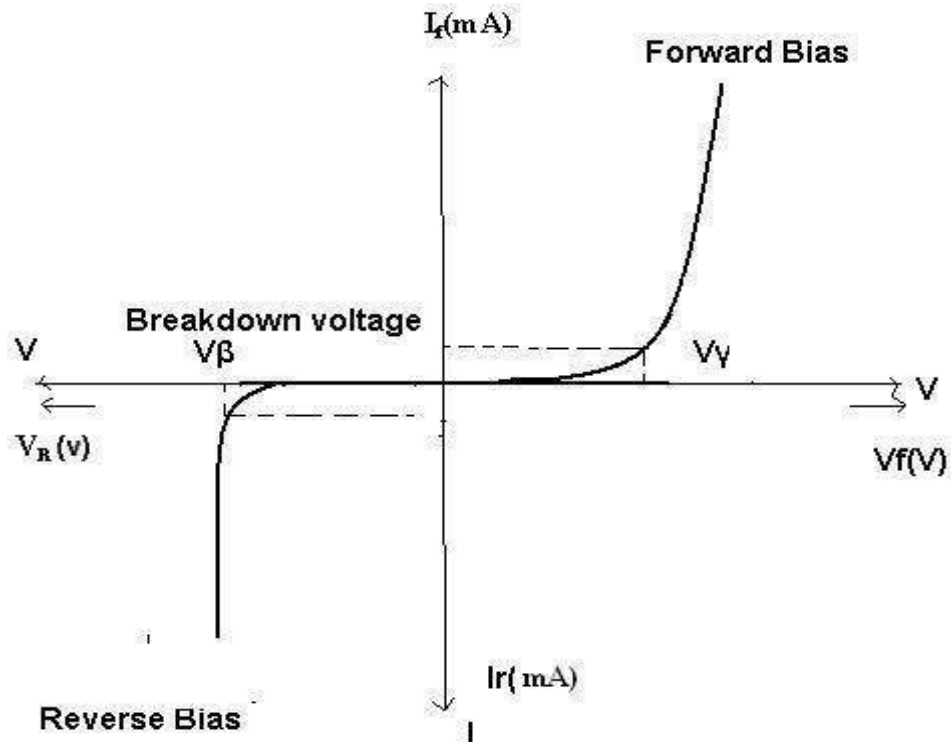
PRECAUTIONS:

1. While doing the experiment do not exceed the ratings of the zener diode. This may lead to damage the diode.

2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.

3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.

RESULT: The V-I characteristics and Regulation characteristics of a zener diode are observed.

EXPERIMENT -3
FULL WAVE RECTIFIER WITH AND WITHOUT FILTERS

AIM: 1. To obtain the load regulation and ripple factor of a full-wave rectifier by using

(a). without Filter

(b). with Filter

2. To observe the input and output waveforms of a full-wave rectifier.

APPARATUS:

S.No	Name of the Apparatus	Range	Quantity
1	Diodes IN 4007 (Si)		2
2	Decade Resistance Box	(1KΩ-10 KΩ)	1
3	Transformer	230 V AC	1
4	Capacitor	100μF	1
5	Bread Board		
6	Digital Voltmeter	(0-20)V (AC & DC)	2
7	Connecting Wires	As Required	

THEORY:

The circuit of a center-tapped full wave rectifier uses two diodes D1&D2. During positive half cycle of secondary voltage (input voltage), the diode D1 is forward biased and D2is reverse biased.

The diode D1 conducts and current flows through load resistor R_L. During negative half cycle, diode D2 becomes forward biased and D1 reverse biased. Now, D2 conducts and current flows through the load resistor R_L in the same direction. There is a continuous current flow through the load resistor R_L, during both the half cycles and will get unidirectional current as show in the model graph. The difference between full wave and half wave rectification is that a full wave rectifier allows unidirectional (one way) current to the load during the entire 360 degrees of the input signal and half-wave rectifier allows this only during one half cycle (180 degree).

CIRCUIT DIAGRAM:

(a) WITHOUT FILTER:
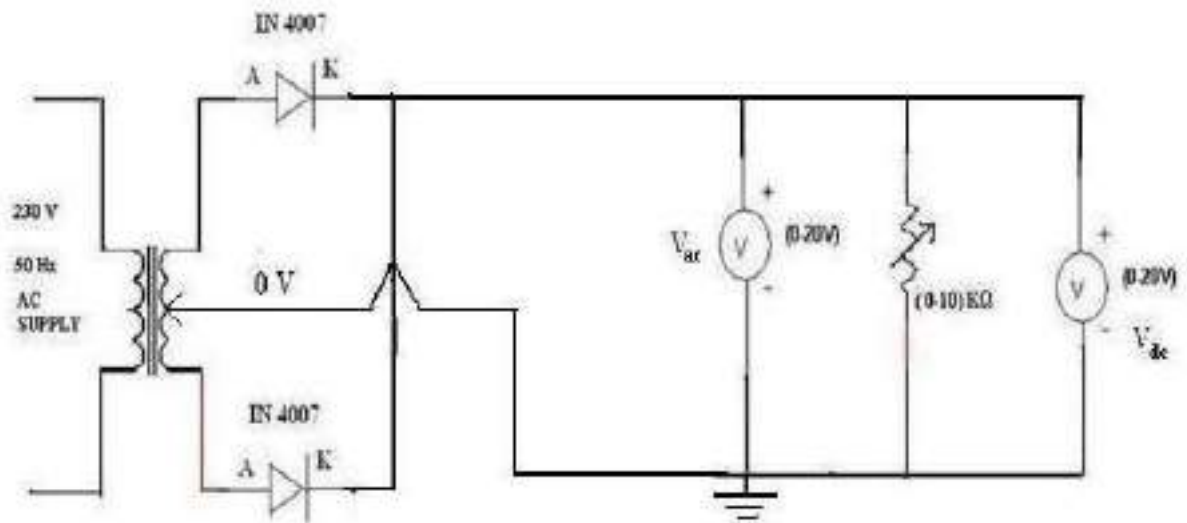
(b) WITH FILTER:
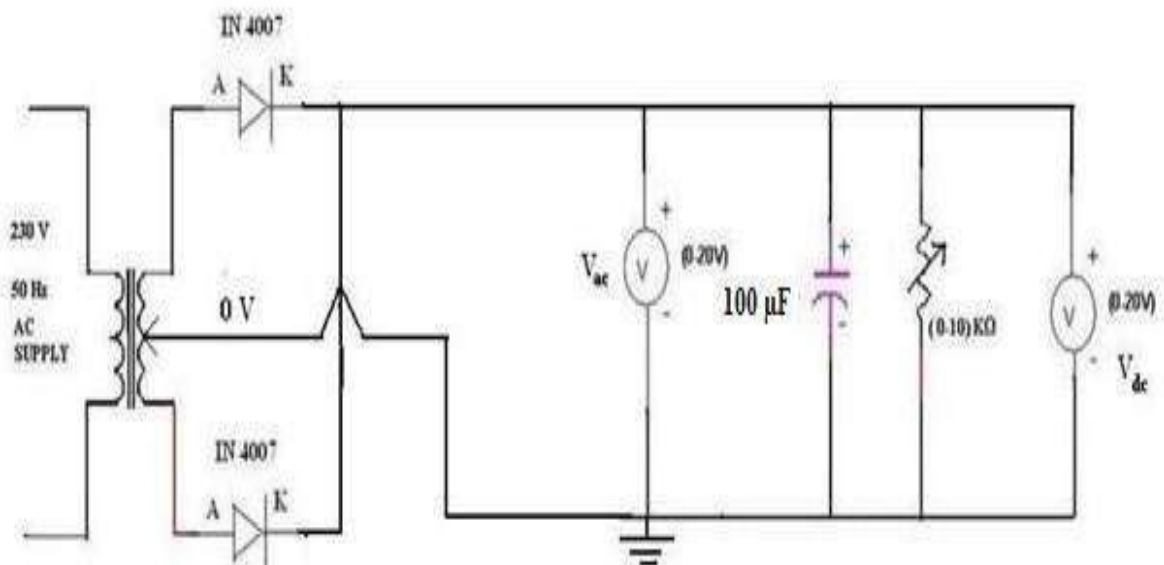
PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Connect the primary side of the transformer to ac mains and the secondary side to the rectifier input.
3. By using the multimeter, measure the ac input voltage of the rectifier and, ac and dc voltage at the output of the rectifier.
4. Find the theoretical value of dc voltage by using the formula,

$$V_{dc}=2V_m/\Pi$$

Where, $V_m= \sqrt{2}V_{rms}$, (V_{rms}=output ac voltage.)

5. Now, the Ripple factor is calculated by using the formula

$$\Gamma = \textbf{ac output voltage } (V_{ac})/\textbf{dc output voltage } (V_{dc})$$

6. By increasing the value of the resistance from 1 KΩ to 10KΩ, the voltage across the load (V_L) and current (I_L) flowing through the load are measured.
7. Draw a graph between load voltage (V_L) and load current (I_L) by taking V_L on X-axis and I_L on y-axis.
8. From the value of no-load voltage (V_{NL}), the % regulation is to be calculated from the theoretical calculations given below.

INPUT AND OUTPUT WAVEFORMS:

AC Input Waveform

Output from D1 and D2

C Charges   C Discharges   Smoothed Output From Capacitor
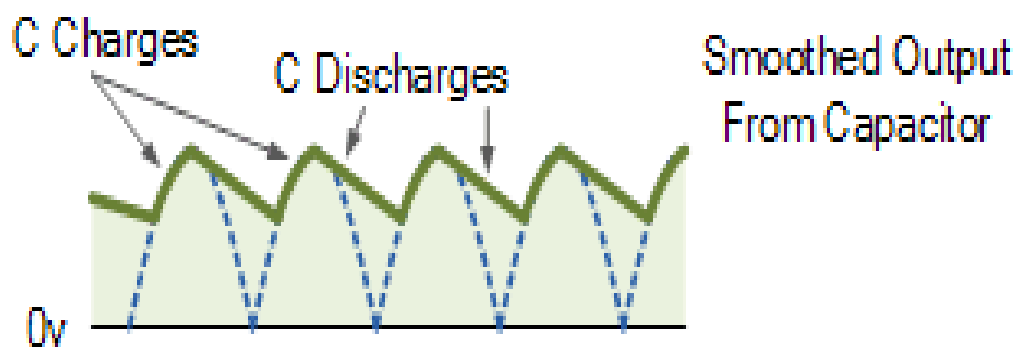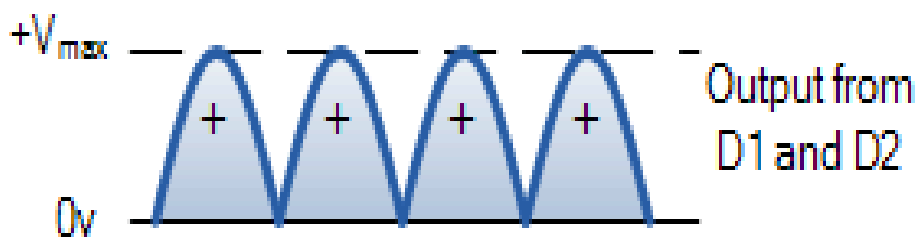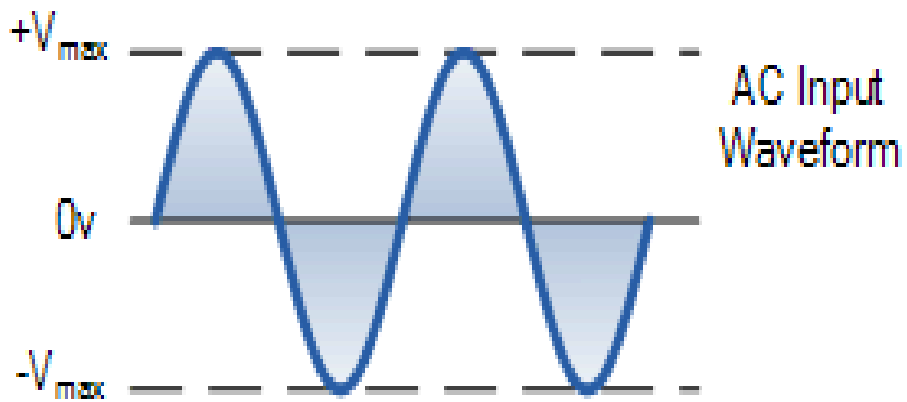
THEORETICAL CALCULATIONS FOR RIPPLE FACTOR & % REGULATION:

(a) WITHOUT FILTER:

For a Full-Wave Rectifier,

$$V_{rms} = V_m/\sqrt{2}$$

$$V_{dc} = 2V_m/\Pi$$

Therefore, Ripple factor $\Gamma = \sqrt{(V_{rms}/V_{dc})^2 - 1} = \underline{\textbf{0.482}}$

$$\% \text{ regulation} = [(V_{NL} - V_{FL})/V_{FL}] * 100$$

(b) WITH FILTER:

Ripple factor for a Full-Wave Rectifier is $\Gamma = 1/(2\sqrt{3}\, fRC)$.

Where   f = 50Hz

C = 100μF

R = (1-10) KΩ

Therefore, for 1KΩ, Ripple factor, $\Gamma = \underline{\textbf{0.0577}}$

$$\% \text{ regulation} = [(V_{NL} - V_{FL})/V_{FL}] * 100$$

OBSERVATIONS:

(a) WITH OUT FILTER:

$V_{NL} = \underline{} V$

S.No	Load Resistance (KΩ)	$V_{ac}(v)$	$V_{dc}(v)$	$\Gamma = V_{ac}/V_{dc}$	% Regulation

(b) *WITH FILTER:* V_{NL} = _____ V

PRECAUTIONS:

S.No	Load Resistance (KΩ)	V_{ac}(v)	V_{dc}(v)	$\Gamma = V_{ac}/V_{dc}$	% Regulation

1. The primary and secondary sides of the transformer should be carefully identified.

2. The polarities of the diode should be carefully identified.

3. While determining the % regulation, first Full load should be applied and then it should be decremented in steps.

RESULT:

The Ripple factor and the % regulation for the Full-Wave Rectifier with and without filters are calculated.

1. The Ripple factor of Full-Wave Rectifier without filter is _____

2. The Ripple factor of Full-Wave Rectifier with filter is _____

3. The % Regulation of Full-Wave Rectifier without filter is _____

4. The % Regulation of Full-Wave Rectifier with filter is _____

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Experiment -4

INPUT AND OUTPUT CHARACTERISTICS OF BJT IN CE CONFIGURATION

</div>

AIM: 1. To draw the input and output characteristics of transistor connected in CE

Configuration

2. To find Input Resistance (R_i), Output Resistance (R_o) and Current amplification

Factor (β) of the given transistor.

APPARATUS:

S.No	Name of the Apparatus	Range	Quantity
1	Transistor (BC-107)		1
2	Resistors	1KΩ, 470Ω	1
3	Regulated Power Supply	(0-30)V DC	1
4	Bread Board		1
5	Digital Ammeters	(0-200)μA/(0-200)mA	2
6	Digital Voltmeters	(0-20)V DC	2
7	Connecting Wires	As Required	

THEORY:

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and out put is taken across the collector and emitter terminals. Therefore the emitter terminal is common to both input and output.

The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement I_B increases less rapidly with V_{BE}. Therefore input resistance of CE circuit is higher than that of CB circuit.

The output characteristics are drawn between I_c and V_{CE} at constant I_B. the collector current varies with V_{CE} unto few volts only. After this the collector current becomes almost constant, and independent of V_{CE}. The value of V_{CE} up to which the collector current changes with V_{CE} is known as Knee voltage. The transistor always operated in the region above Knee voltage, I_C is always constant and is approximately equal to I_B. The current amplification factor of CE configuration is given by β = $\Delta I_C / \Delta I_B$

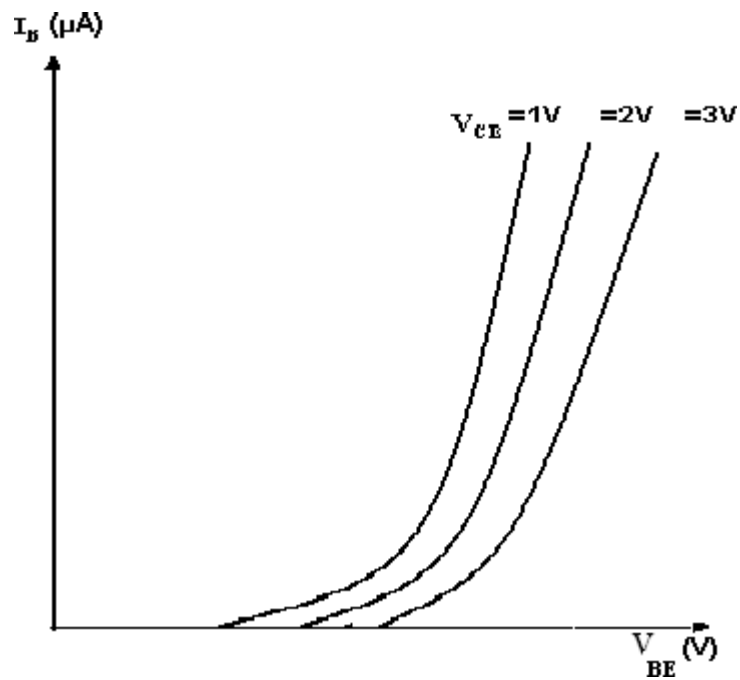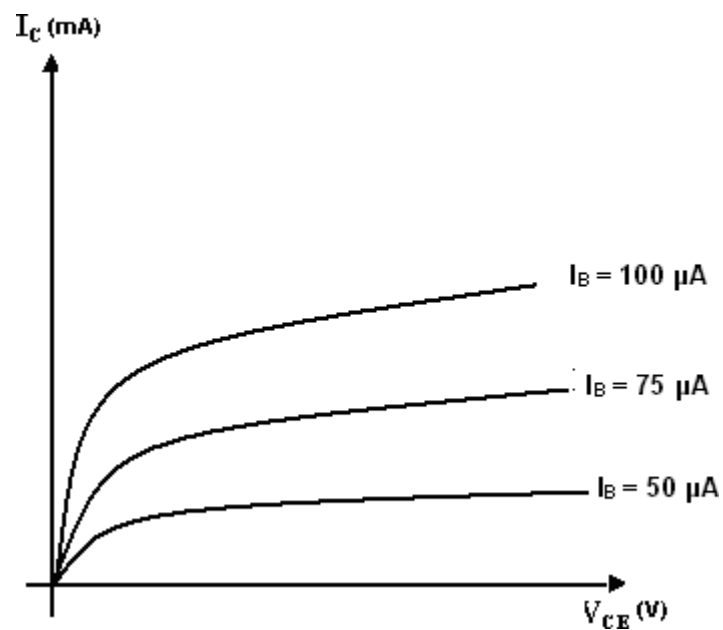### CIRCUIT DIAGRAM:

PROCEDURE:

(i) INPUT CHARACTERSTICS:

1. Connect the circuit as per the circuit diagram.
2. For plotting the input characteristics the output voltage V_{CE} is kept constant at 1V and for different values of $V_{BE,}$ note down the values of I_B.
3. Repeat the above step by keeping V_{CE} at 2V and 3V.
4. Tabulate all the readings.
5. Plot the graph between $V_{BE\,on}$ x-axis and I_B on y-axis forconstant $V_{CE.}$

(ii) OUTPUT CHARACTERSTICS:

1. Connect the circuit as per the circuit diagram.
2. For plotting the output characteristics the input current I_B is kept constant at 50μA and for different values of V_{CE}, note down the values of I_C.
3. Repeat the above step by keeping I_B at 75μA and 100μA.
4. Tabulate the all the readings.
5. Plot the graph between V_{CE} on x-axis and I_C on y-axis for constant I_B.

OBSERVATIONS:

(i) INPUT CHARACTERISTICS:

S.No	$V_{CE} = 1V$		$V_{CE} = 2V$		$V_{CE} = 3V$	
	V_{BE} (V)	I_B (µA)	V_{BE} (V)	I_B (µA)	V_{BE} (V)	I_B (µA)

(ii)   OUTPUT CHARACTERISTICS:

S.No	$I_B = 50$ µA		$I_B = 75$ µA		$I_B = 100$ µA	
	V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C(mA)	V_{CE}(V)	I_C (mA)

MODEL GRAPH:

(i)   INPUT CHARACTERISTICS:

(ii) OUTPUT CHARACTERISTICS:

PRECAUTIONS:

1. While doing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base and collector terminals of the transistor.

CALCULATIONS:

1. **Input resistance:** To obtain input resistance find ΔVBE and ΔIB at constant VCE on one of the input characteristics. Then

$$R_i = \Delta V_{BE} / \Delta I_B \ (V_{CE} \text{ constant})$$

2. **Output resistance:** To obtain output resistance, find ΔIC and ΔVCE at constant I_B.

$$R_o = \Delta V_{CE} / \Delta I_C \ (I_B \text{ constant})$$

3. The current amplification factor of CE configuration is given by

$$\beta = \Delta I_C / \Delta I_B$$

RESULT: The input and output characteristics of a transistor in CE configuration are drawn. The Input (R_i) and Output resistances (R_o) and β of a given transistor are calculated.

1. The Input resistance (R_i) of a given Transistor is_____
2. The Output resistance (R_o) of a given Transistor is_____
3. The Current amplification factor is_____

Experiment -5
INPUT AND OUTPUT CHARACTERISTICS OF FE IN CS CONFIGURATION

AIM: 1. To draw the Drain and Transfer characteristics of a given FET in CS

Configuration.

2. To find the drain resistance (rd), amplification factor (μ) and Trans-Conductance

(gm) of the given FET.

APPARATUS:

S.No	Name of the Apparatus	Range	Quantity
1	JFET (BFW-10)		1
2	Resistors	100KΩ, 100Ω	1
3	Regulated Power Supply	(0-30)V DC	1
4	Bread Board		1
5	Digital Ammeter	(0-200)mA	1
6	Digital Voltmeter	(0-20)V DC	2
7	Connecting Wires	As Required	

THEORY:

A FET is a three terminal device, having the characteristics of high input impedance and less noise, the Gate to Source junction of the FET s always reverse biased. In response to small applied voltage from drain to source, the n-type bar acts as sample resistor, and the drain current increases linearly with V_{DS}. With increase in I_D the ohmic voltage drop between the source and the channel region reverse biases the junction and the conducting position of the channel begins to remain constant. The V_{DS} at this instant is called "pinch of voltage".

If the gate to source voltage (V_{GS}) is applied in the direction to provide additional reverse bias, the pinch off voltage ill is decreased. In amplifier application, the FET is always used in the region beyond the pinch-off.

$$I_{DS} = I_{DSS} (1 - V_{GS}/V_P)^2$$

CIRCUIT DIAGRAM:
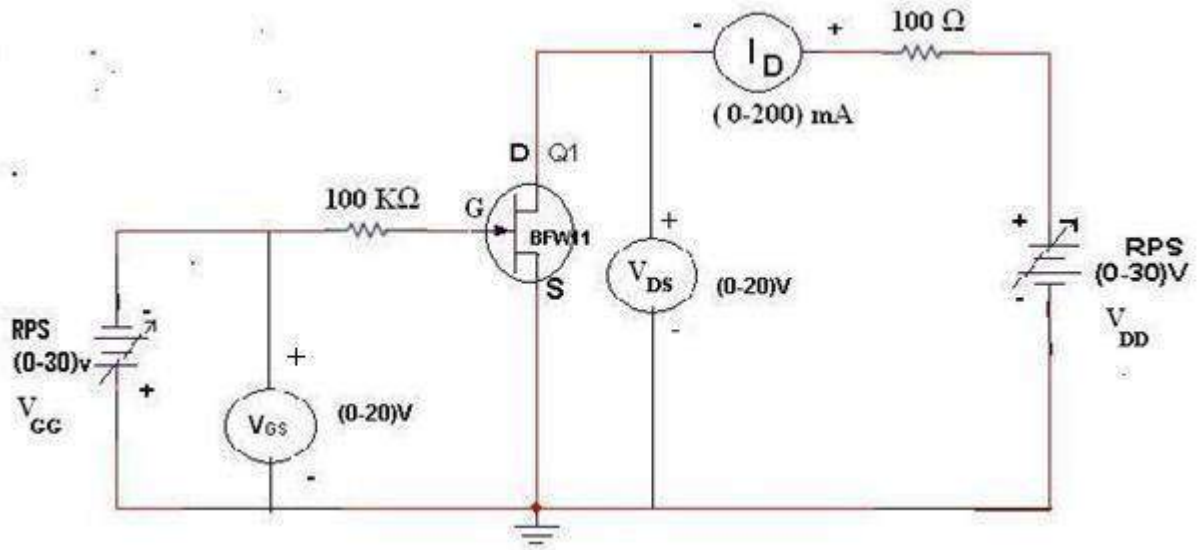
PROCEDURE:

1. All the connections are made as per the circuit diagram.

2. To plot the drain characteristics, keep V_{GS} constant at 0V.

3. Vary the V_{DD} and observe the values of V_{DS} and I_D.

4. Repeat the above steps 2, 3 for different values of V_{GS} at -1V and -2V.

5. All the readings are tabulated.

6. To plot the transfer characteristics, keep V_{DS} constant at 0.5V.

7. Vary V_{GG} and observe the values of V_{GS} and I_D.

8. Repeat steps 6 and 7 for different values of V_{DS} at 1V and 1.5V.

9. The readings are tabulated.

10. From drain characteristics, calculate the values of drain resistance (r_d) by using the formula

$$r_d = \Delta V_{DS}/\Delta I_D$$

11. From transfer characteristics, calculate the value of trans-conductance (g_m) by using the formula

$$g_m = \Delta I_D/\Delta V_{GS}$$

12. Amplification factor (μ) = drain resistance (r_d) x Trans-conductance (g_m)

$$\mu = \Delta V_{DS}/\Delta V_{GS}$$

OBSERVATIONS:

(i) DRAIN CHARACTERISTICS:

S.No	VGS = 0V		VGS = -1V		VGS = -2V	
	V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)

(ii) TRANSFER CHARACTERISTICS:

S.No	VDS =0.5V		VDS=1V		VDS =1.5V	
	V_{GS} (V)	I_D (mA)	V_{GS} (V)	I_D (mA)	V_{GS} (V)	I_D (mA)

MODEL GRAPH:

(i) DRAIN CHARACTERISTICS:
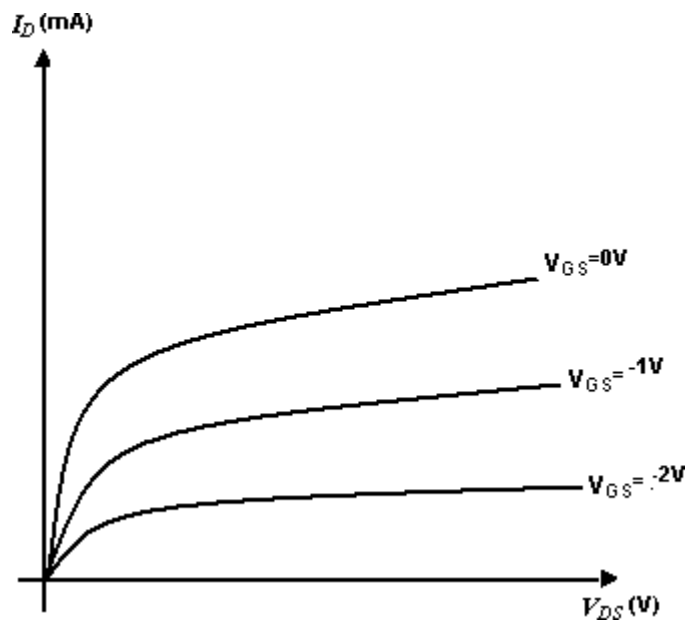
(ii) TRANSFER CHARACTERISTICS:
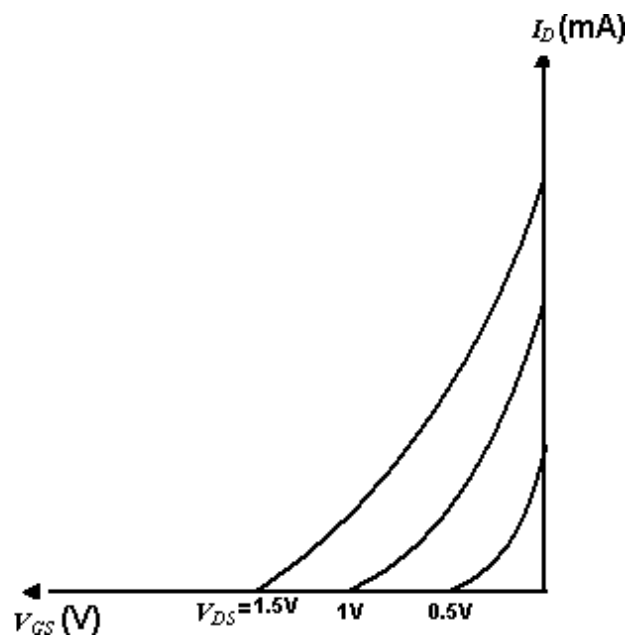
PRECAUTIONS:

1. While doing the experiment do not exceed the ratings of the FET. This may lead to damage the FET.

2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.

3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.

4. Make sure while selecting the Source, Drain and Gate terminals of the FET.

RESULT:

1. The drain and transfer characteristics of a given FET are drawn.

2. The drain resistance (r_d), amplification factor (μ) and Trans-conductance (g_m) of the given FET are calculated.

      (i)   The drain resistance (r_d) of FET is _____

      (ii)   Trans-conductance (g_m) of FET is _____

      (iii)   Amplification factor (μ) of FET is _____

Experiment-6
Common Emitter Amplifier characteristics

AIM: 1. To obtain the frequency response of the Common Emitter BJT Amplifier.

2. To Measure the Voltage gain and Bandwidth of CE amplifier.

APPARATUS:

s

S.No	Name of the Apparatus	Range	Quantity
1	Transistor (BC-107)		1
2	Resistors	1KΩ, 4.7KΩ, 10KΩ, 15 KΩ , 68 KΩ	1
3	Capacitors	10μF 47 μF	2 1
4	Bread Board		1
5	Regulated Power Supply	(0-30)V DC	1
6	Function Generator	(100-1M)Hz	1
7	CRO	(100-20M)Hz	1
7	Connecting Wires	As Required	

THEORY:

The CE amplifier provides high gain &wide frequency response. The emitter lead is common to both input & output circuits and is grounded. The emitter-base circuit is forward biased. The collector current is controlled by the base current rather than emitter current. The input signal is applied to base terminal of the transistor and amplifier output is taken across collector terminal. A very small change in base current produces a much larger change in collector current. When +ve half-cycle is fed to the input circuit, it opposes the forward bias of the circuit which causes the collector current to decrease, it decreases the voltage more –ve. Thus when input cycle varies through a -ve half-cycle, increases the forward bias of the circuit, which causes the collector current to increases thus the output signal is common emitter amplifier is in out of phase with the input signal.

CIRCUIT DIAGRAM:
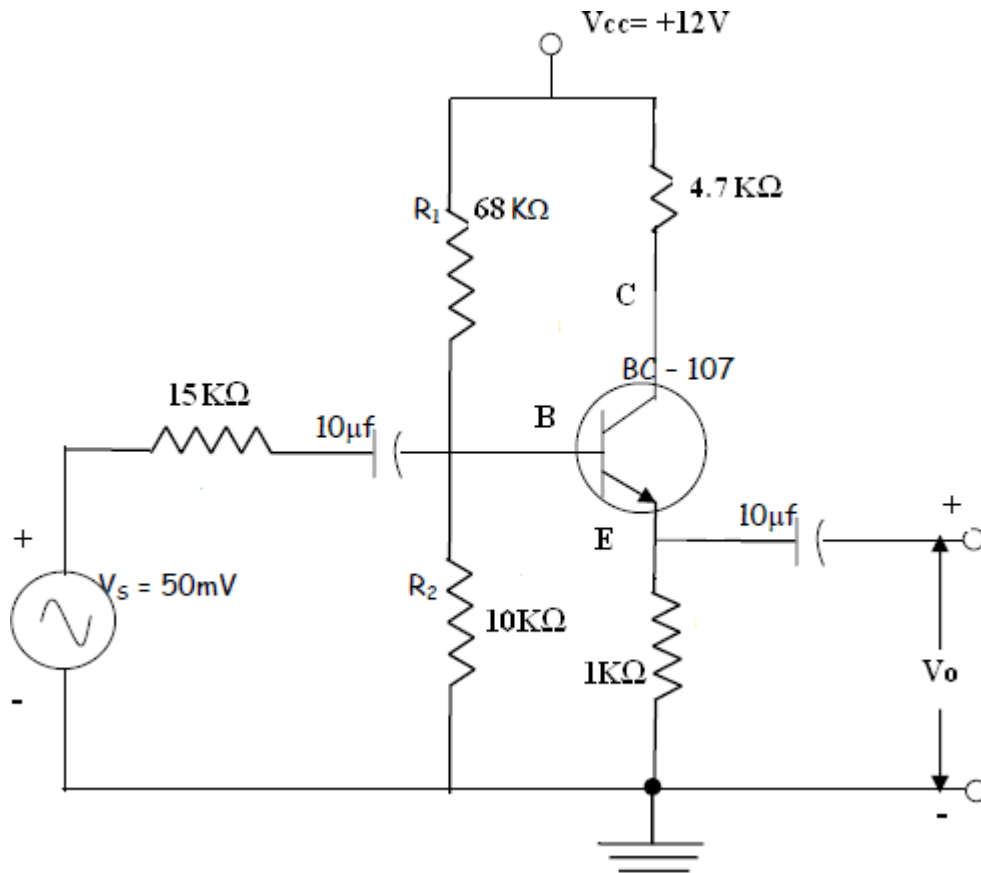
PROCEDURE:

1. Connect the circuit as per the circuit diagram.

2. Set Source Voltage Vs = 50mV (say) at 1 KHz frequency, using function generator.

3. Keeping the input voltage constant, vary the frequency from 50Hz to 1MHz in regular steps and note down the corresponding output voltage.

4. Calculate the Voltage Gain by using the formula

$$A_v = \text{Output voltage } (V_0) \text{ / Input voltage } (V_s)$$

5. Calculate the Voltage Gain in dB by using Voltage Gain $A_v(dB) = 20 \log_{10} (V_o/V_s)$.

6. Plot the Graph by taking Voltage gain (dB) on x-axis and frequency (Hz) on y-axis.

7. The Bandwidth of the amplifier is calculated from the graph using the expression,

Bandwidth, BW=f_2-f_1

Where f_1 is lower 3-dB frequency

f_2 is upper 3-dB frequency

OBSERVATIONS:

$V_s =$ _____ V

S.No	Input Frequency (Hz)	Output Voltage (V_o) (volts)	Voltage Gain=V_o/V_s	Voltage Gain (dB) =$20 \log_{10} (V_o/V_s)$

FREQUENCY RESPONSE:
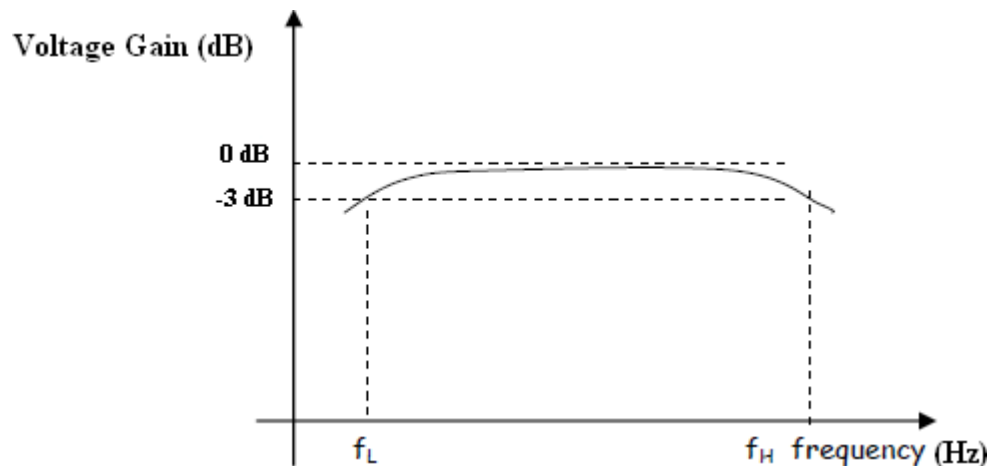
PRECAUTIONS:

1. While doing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.

2. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.

3. Make sure while selecting the emitter, base and collector terminals of the transistor.

RESULT: The Voltage gain and Bandwidth of CE amplifier is measured and the frequency response of the CE Amplifier is obtained.

1. The Voltage gain of CE Amplifier is _____.
2. The Bandwidth of CE Amplifier is _____.

Experiment-7
SWITCHING CHARACTERISTICS OF A TRANSISTOR

AIM: To design and observe the performance of a transistor as a switch

APPARATUS REQUIRED:

1. Transistor (BC107)   -   1 No.

2. Resistor 6.8 kΩ, 33 kΩ, 1kΩ

3. Bread board Trainer

4. Function Generator

5. Cathode Ray Oscilloscope

6. Connecting Wires
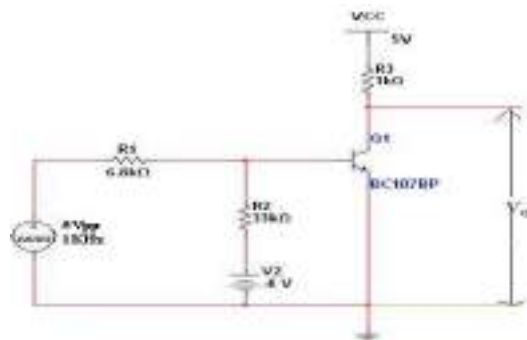
CICRUIT DIAGRAM:

PROCEDURE:

1. Connect the circuit as per circuit diagram.

2. Apply square wave of 5V with frequency of 1KHz from function generator.

3. Observe the input and output waveforms.

EXPECTED WAVEFORMS:
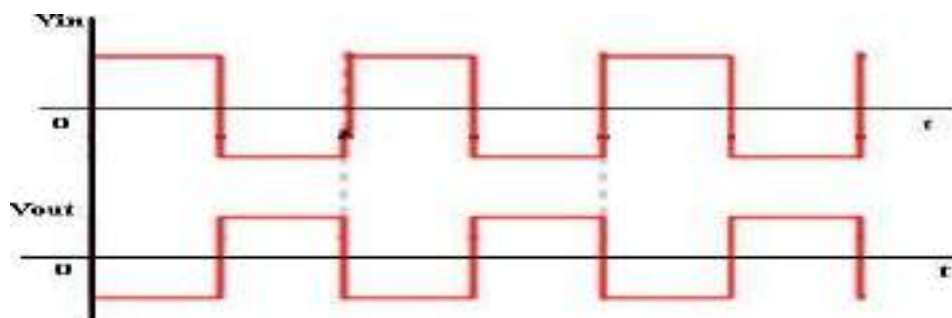
RESULT:

Experiment-8
SCR CHARACTERISTICS

AIM: 1. To draw the V-I characteristics of SCR.

      2. To find the Break-over voltage (V_{BO}) and Holding current (I_H) of SCR.

APPARATUS:

S.No	Name of the Apparatus	Range	Quantity
1	SCR (TYN616)		1
2	Resistors	1KΩ, 10KΩ	1
3	Regulated Power Supply	(0-30)V DC	1
4	Bread Board		1
5	Digital Ammeter	(0-200)mA,(0-200)µA	2
6	Digital Voltmeter	(0-20)V DC	1
7	Connecting Wires	As Required	

THEORY:

It is a four layer semiconductor device being alternate of P-type and N-type silicon. It consists of 3 junctions J_1, J_2, J_3 the J_1 and J_3 operate in forward direction and J_2 operates in reverse direction and three terminals called anode A, cathode K, and a gate G. The operation of SCR can be studied when the gate is open and when the gate is positive with respect to cathode. When gate is open, no voltage is applied at the gate due to reverse bias of the junction J_2 no current flows through R_2 and hence SCR is at cut off. When anode voltage is increased J_2 tends to breakdown.
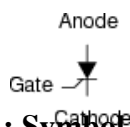
Fig.: Symbol of SCR

When the gate positive, with respect to cathode J_3 junction is forward biased and J_2 is reverse biased .Electrons from N-type material move across junction J_3 towards gate while holes from P-type material moves across junction J_3 towards cathode. So gate current starts flowing, anode current increase is in extremely small current junction J_2 break down and SCR conducts heavily. When gate is open the break over voltage is determined on the minimum forward voltage at which SCR conducts heavily. Now most of the supply voltage appears across the load resistance. The holding current is the maximum anode current gate being open, when break over occurs.

CIRCUIT DIAGRAM:
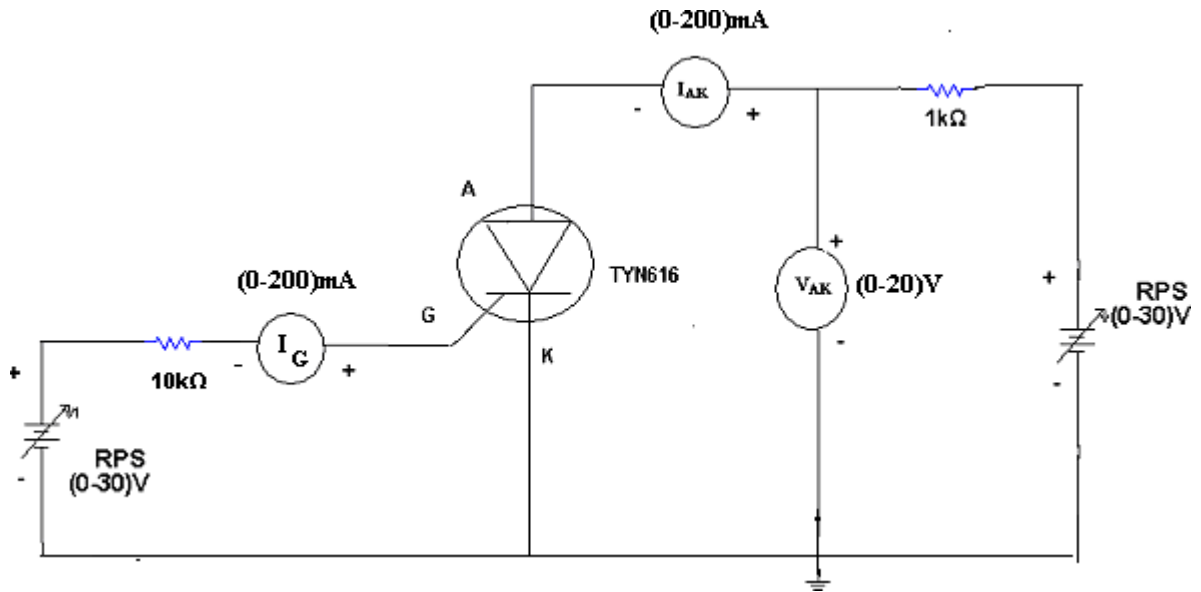
## PROCEDURE:

1. All the connections are made as per the circuit diagram.

2. Keep the gate current (I_G) open i.e. $I_G = 0$ mA.

3. Vary the anode to cathode supply voltage and note down the readings of Voltage V_{AK} (V), and Current I_{AK} (µA).

4. Now Keep the gate current (I_G) at a standard value of 10 mA i.e. $I_G = 10$ mA.

5. Again vary the anode to cathode supply voltage and note down the corresponding readings of Voltage V_{AK} (V), and Current I_{AK} (mA).

6. Plot the graph by taking V_{AK} (V) on x-axis and Current I_{AK} (mA) on y-axis.

7. Measure the Break-over voltage (V_{BO}) and Holding current (I_H) of SCR from the graph.

OBSERVATIONS:

S.No	$I_G = 0$ mA		$I_G = 10$ mA	
	V_{AK} (V)	I_{AK} (µA)	V_{AK} (V)	I_{AK} (mA)

MODEL GRAPH:
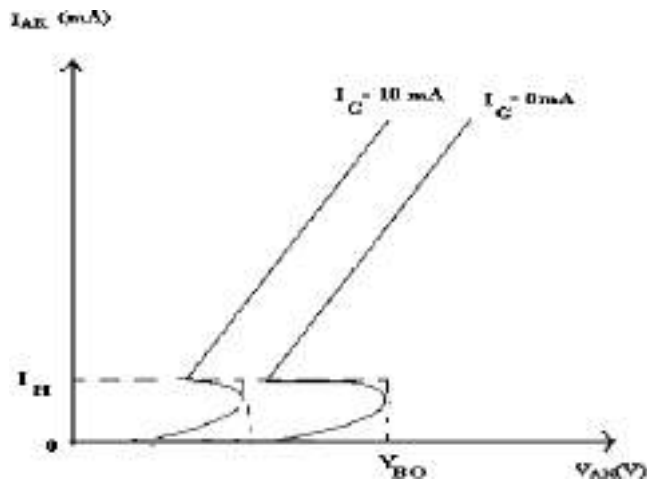
PRECAUTIONS:

1. While doing the experiment do not exceed the ratings of the SCR. This may lead to damage the SCR.

2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.

3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.

4. Make sure while selecting the Anode, Cathode and Gate terminals of the SCR.

RESULT: The V-I characteristics of SCR are drawn and the Break-over voltage (V_{BO}), Holding current (I_H) of SCR are found.

1. The Break-over voltage (V_{BO}) of SCR is_____.

2. The Holding current (I_H) of SCR is_____.

# Experiment-9
TYPES OF CLIPPERS AT DIFFERENT REFERENCE VOLTAGES

AIM: To observe the output wave form for various types of Clipping circuits.

APPARATUS:

1. Diodes (1N4007) -2 Nos
2. Resistors (1 KΩ -1 No)
3. Function generator
4. Bread board trainer
5. Cathode Ray Oscilloscope (CRO)
6. Connecting Wires.

CIRCUIT DIAGRAM:

1. **Shunt Positive Clipper:**
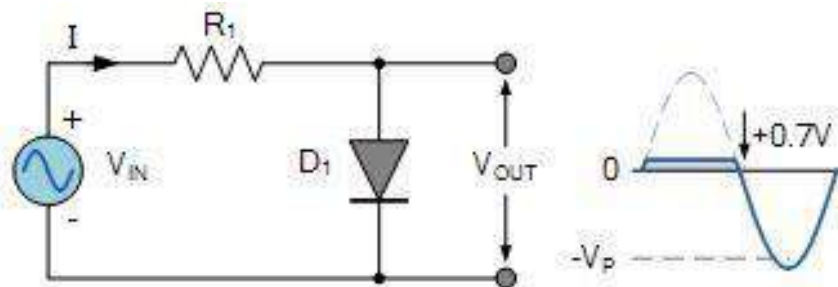

2. **Shunt Negative Clipper:**
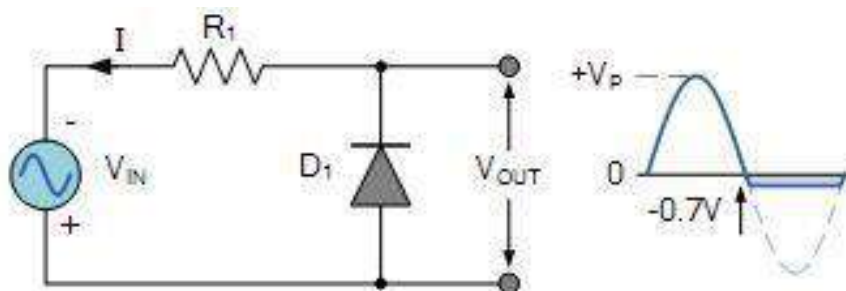
3. **Shunt Positive clipper with reference voltage**
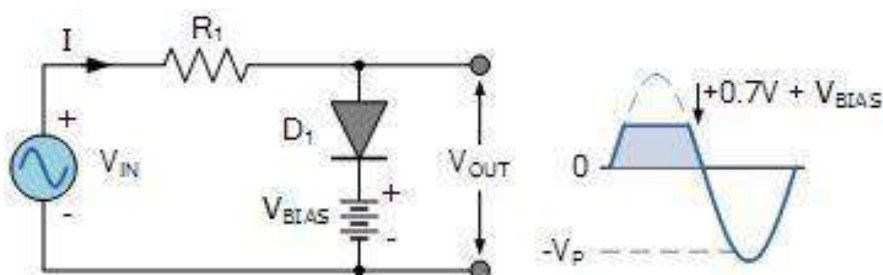
4. Shunt Negative Clipper with Reference Voltage:
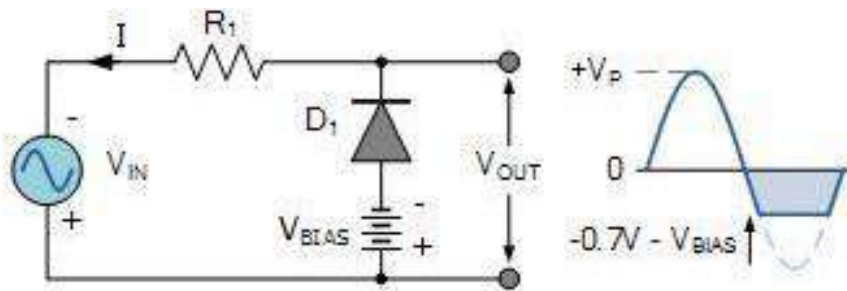
5. Clipping at two reference voltages :
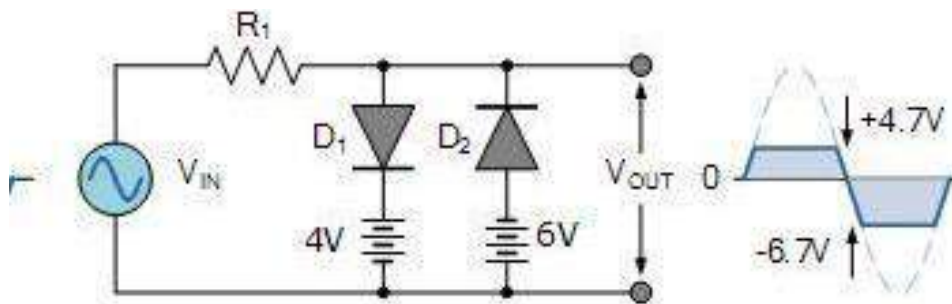
PROCEDURE:

1. Make the circuit connections as per circuit diagram
2. Set the sinusoidal input wave form with magnitude of 5 volts and frequency of 1KHz in the function generator
3. Apply sinusoidal input from function generator to the circuit.
4. Sketch the respective output waveforms.
5. Repeat above procedure for each circuit.

Result:

Experiment-10
TYPES OF CLAMPERS AT DIFFERENT REFERENCE VOLTAGES

AIM: To observe the output wave form for various types of Clamping circuits.

APPARATUS:

1. Diodes (1N4007)-1.No.s

2. Resistors (1 kΩ -1)

3. Capacitor - 10μf

4. Function generator

5. Bread board Trainer

6. Cathode Ray Oscilloscope (CRO)

7. Connecting Wires

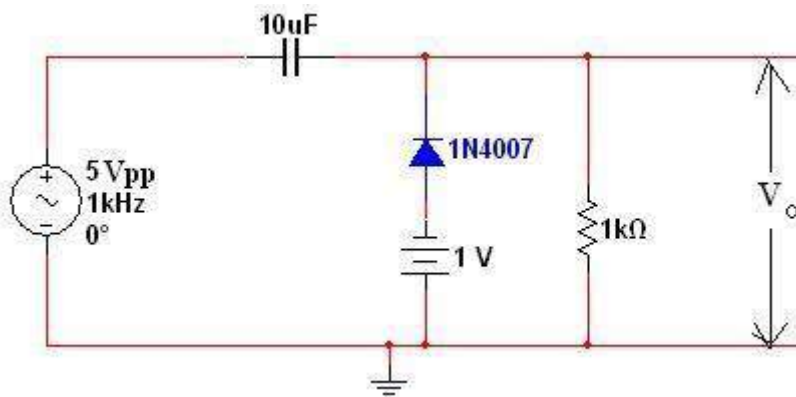**CICRUIT DIAGRAM**:

1.**Positive peak clamper**
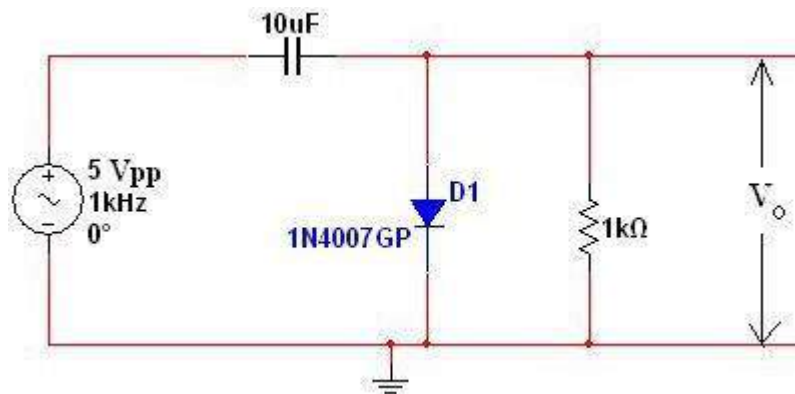
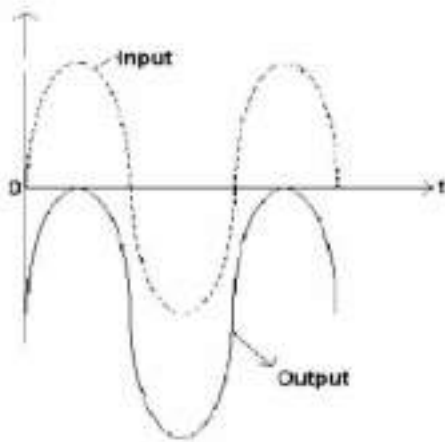2. **Negative peak clamper**
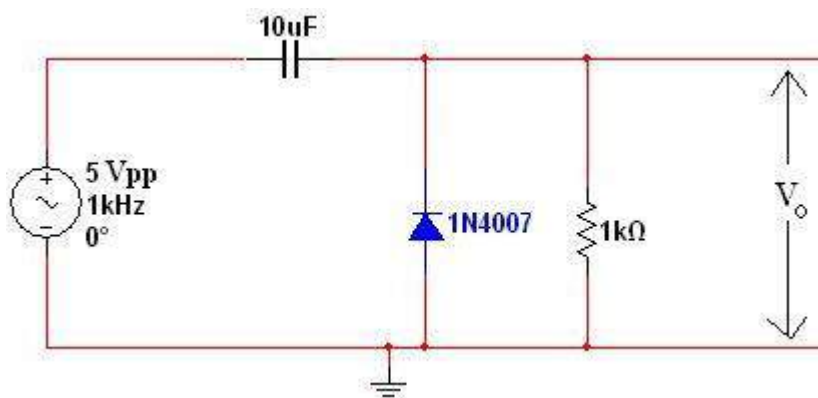
3. Positive peak bias clamper
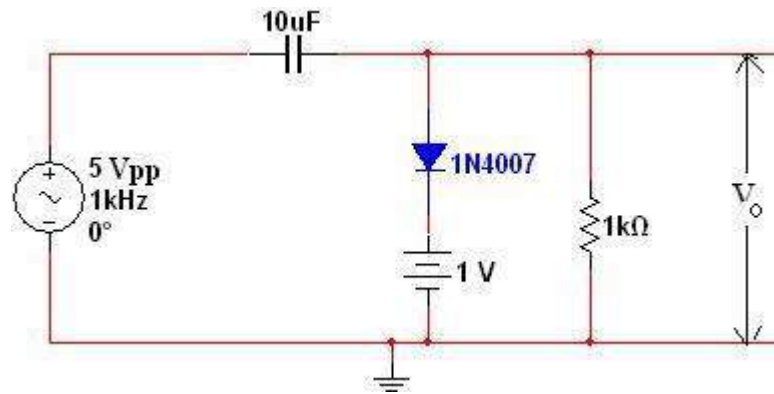
**4. Negative peak bias clamper**

PROCEDURE:

1. Make the circuit connections as per circuit diagram
2. Set the sinusoidal input wave form with magnitude of 5 volts and frequency of 1KHz in the function generator
3. Apply sinusoidal input from function generator to the circuit.
4. Sketch the respective output waveforms.
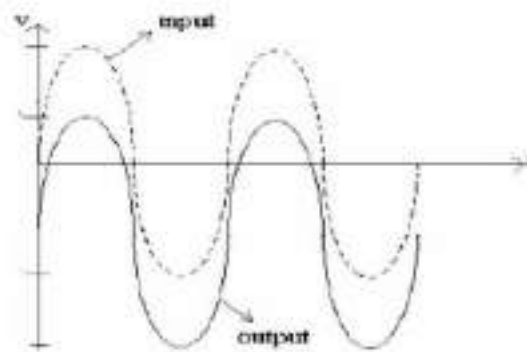5. Repeat above procedure for each circuit.

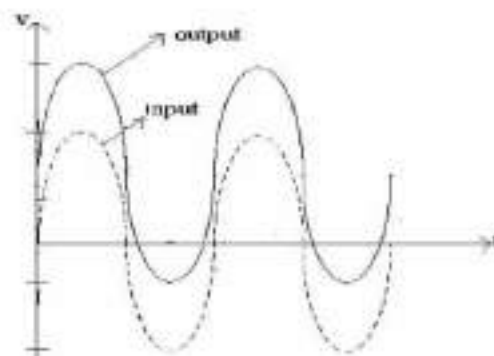**EXPECTED WAVE FORMS:**

Positive peak clamping to 0V:

Negative peak clamping to 0V
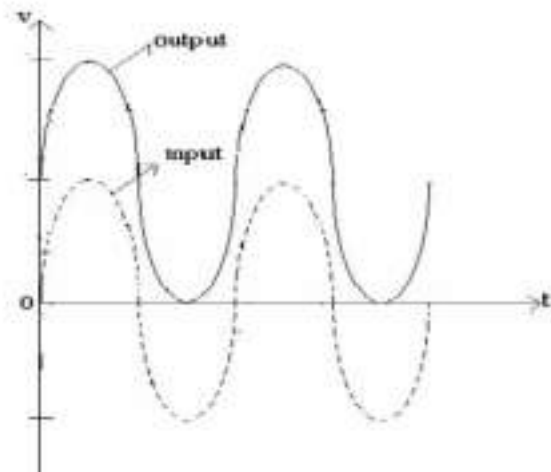
Positive peak clamping to 1v

Negative peak clamping to Vr= 1 v

RESULT: