UNIT - I

P-N Junction Diode

Theory of P-N Junction :-

→ Combining p-type S.C & n-type S.C forms PN Jn.

→ Connecting di (two) electrodes to the PN Jn forms PN Jn. diode.

→ The donor ion is indicated schematically by a plus sign because after this impurity atom "donates" an electron, it becomes a Positive ion.

→ The acceptor ion is indicated by a minus sign because, after this atom "accepts" an electron, it becomes a negative ion.

- when P & N type are combining together by an appropriate scheme like Ion implantation or diffusion.
- Properly formed PN Jn will be having p-type on one side & n-type on the another side.
- P-type S.C have acceptor ions & carriers are holes (Positively charged) & n-type " " donor " & " electrons

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According to Mass-Action Law for N-type $P_n n_n = n_i^2$

$$\therefore \boxed{N_D \simeq \frac{n_i^2}{P_n}}$$

P-Type S.C :-

$P + N_D = n + N_A$

Let $n_p \rightarrow$ Concentration of free electrons

$P_p \rightarrow$ " holes

$N_A \rightarrow$ " donor atoms

In P-type S.C. N_D (Donor doping) = 0. Hence

$P_p = n_p + N_A$

$\because P_p >> n_p \Rightarrow N_A \simeq P_p$

$\because P_p n_p = n_i^2 \Rightarrow \boxed{N_A \simeq \frac{n_i^2}{n_p}}$

(Mass-action law)

Drift velocity :-

- A charged particle moving under force of attraction/repulsion is said to have drift
- The average velocity with which the charge carriers drift in a define direction under the influence of an applied electric field is called drift velocity V_d.'
- drift velocity is proportional to the electric field $\Rightarrow \boxed{V_d = \mu E}$

where $\mu \rightarrow$ Mobility of charge carriers

$E \rightarrow$ applied electric field

$V_d \rightarrow$ drift velocity

Mobility :- $\boxed{\mu = \frac{V_d}{E}}$ ($m^2/V\text{-sec}$) It is the ratio of drift velocity (in m/s) per unit applied electric field (in V/m)

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There will be difference in the Concentration or there will be a Concentration gradient of holes from P to N side or Concentration gradient of electrons from N to P side.

Whenever there is a Concentration gradient then the Carriers holes & electrons will try to flow from a higher Concentration region to lower Concentration region just like whenever there is a pressure difference in the water level b/w two places then higher pressure water will flow down to place where pressure of water is low.

Similarly because of difference in Concentration, holes will start moving from P type to N type. This process is called diffusion.

Here these holes will be crossing Jn from left side to right side & electrons will be " " Right side to left side

This process is diffusion. Diffusion of holes & electrons will take place whenever we bring PN Jn together.

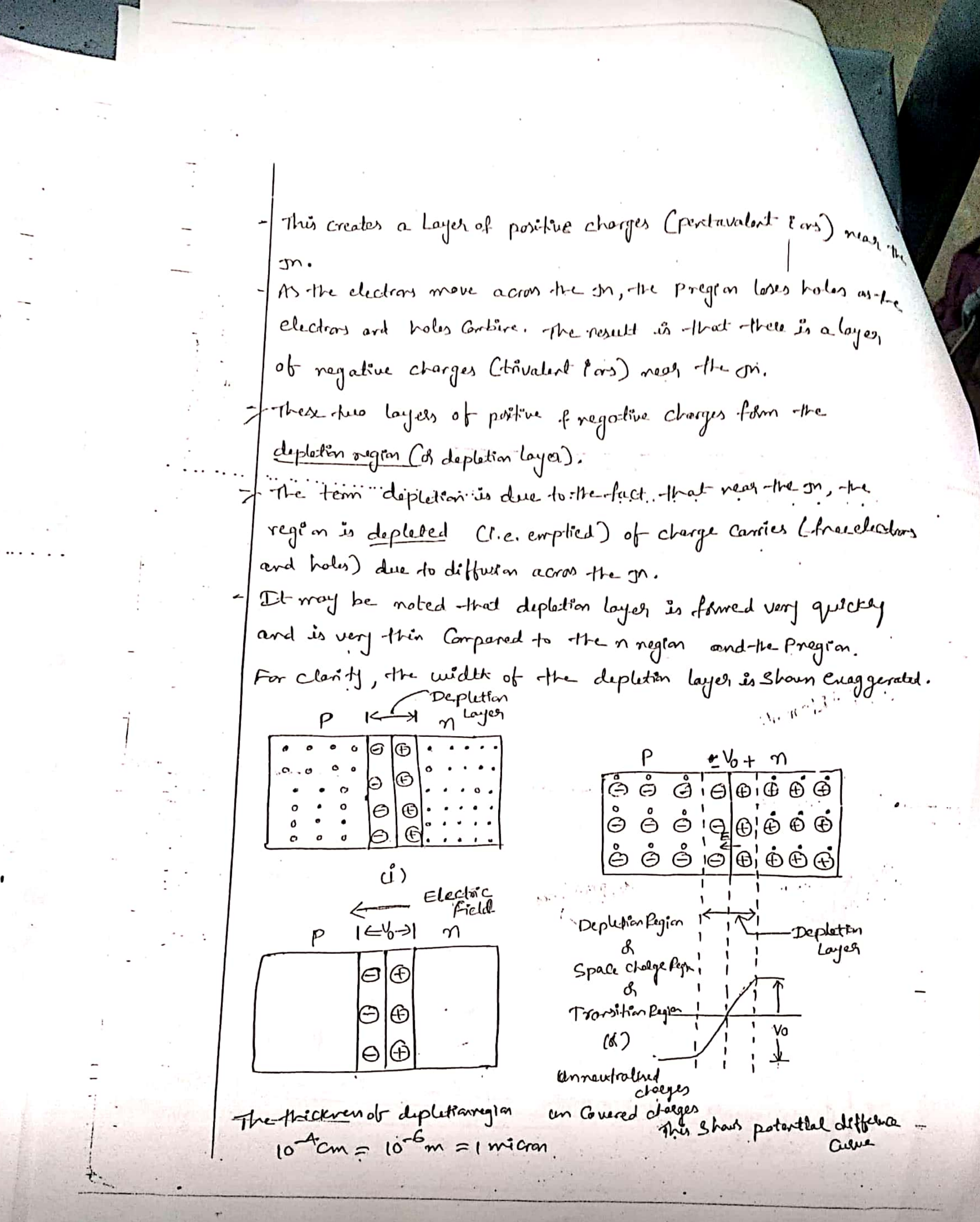
As this Carriers, holes from left side cross over to the right side
electrons from Right side cross over to the left side
then there will be recombination of charge because holes will be recombined by free electrons. & electrons will be recombine with holes.

At the instant of pn-Jn formation, the free electrons near the Jn in the n region begin to diffuse across the Jn into the p region where they combine with holes near the Jn.

The result is that n region loses free electrons as they diffuse into the Jn.

Diffusion current is because of majority charge carriers | Drift current have opposite direction to the Diffusion current.

Drift current is because of minority carriers | under the influence of e field, holes move from N to P, electrons from P to N (minority carriers)



- This creates a layer of positive charges (pentavalent ions) near the jn.
- As the electrons move across the jn, the p region loses holes as the electrons and holes combine. The result is that there is a layer of negative charges (trivalent ions) near the jn.
- These two layers of positive & negative charges form the <u>depletion region</u> (or depletion layer).
- The term depletion is due to the fact that near the jn, the region is <u>depleted</u> (i.e. emptied) of charge carriers (free electrons and holes) due to diffusion across the jn.
- It may be noted that depletion layer is formed very quickly and is very thin compared to the n region and the p region. For clarity, the width of the depletion layer is shown exaggerated.

The thickness of depletion region
10^{-4} cm $= 10^{-6}$ m $= 1$ micron.

This shows potential difference curve

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- Once pn Jn is formed and depletion Layer created, the diffusion of free electrons stops.
- In other words, the depletion region acts as a barrier to the further movement of free electrons across the Jn. The positive and negative charges set up an electric field. This is shown in fig.
- The electric field is a barrier to the free electrons in the n-region. There exists a potential difference across the depletion layer and is called barrier potential (V_0).
- The barrier potential (built in potential) of a pn Jn depends upon several factors including the type of semiconductor material, the amount of doping and temp. The typical barrier potential is approximately:

For Silicon, $V_0 = 0.7V$, For Germanium, $V_0 = 0.3V$

e^- are minority carriers in P-type
h^+ are in N-type

Conductivity:-

(continuation after mobility)

$\because$ Distance (L) = time × velocity $\quad\quad \because V_d \rightarrow$ drift velocity

$$\therefore t = \frac{L}{V_d}$$

The total amount of charge in unit volume $= nq$

The total charge in the conductor, $Q = nq \times (\text{volume}) = nqAL$ $\quad \because V = \text{Area} \times \text{length}$

$$\therefore \text{The current, } I = \frac{Q}{t} = \frac{nqAL}{L/V_d} = nqAV_d = nqA\mu E$$

I (current) rate of flow of electrons i.e. charge flowing per second

Current density $J = \frac{I}{A} = nq\mu E$, this is the current per unit area of cross-section

We can replace the quantity $nq\mu$ by a constant σ,

Conductivity of the conductor $\sigma = nq\mu$

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$$\boxed{J = \sigma E}$$

$\because R = \frac{1}{G}$

$\because V = IR \Rightarrow I = GV$

$\sigma \rightarrow$ Conductivity

$\rho \rightarrow$ resistivity

$$\boxed{\sigma = \frac{1}{\rho}} \quad (S/m)$$

Electrical Properties of Semi Conductor Materials

Conductivity !.

we know that, $\sigma = nq\mu \rightarrow (1)$

→ Conduction in Conductors is due to electrons, where as, conduction in S.C due to two types of charge carriers, i.e, electrons and holes

on the basis of eqn. (1), the Conductivity σ of a S.C material can be obtained as

$\sigma_n = nq\mu_n \rightarrow$ due to electrons

$\sigma_p = pq\mu_p \rightarrow$ due to holes

$\sigma = \sigma_n + \sigma_p$

$\sigma = nq\mu_n + pq\mu_p = q[n\mu_n + p\mu_p]$

$\mu_n \rightarrow$ Mobility of free electrons

$\mu_p \rightarrow$ Mobility of holes

$q \rightarrow$ charge of a Carrier

$n, p \rightarrow$ Electron, hole Concentrations

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Conductivity of Intrinsic S.C

→ In case of intrinsic S.C, no. of free electrons is equal to no. of holes.

$$n = p = n_i$$

$$\therefore \sigma_i = q n_i [\mu_n + \mu_p]$$

Conductivity of N-type S.C

In case of N-type S.C, hole concentration is negligible when compared with electron concentration i.e., $n >> p$.

Let N_D be the concentration of free electrons donated by donor impurities.

$$\sigma_N \simeq q N_D \mu_n$$

P-type ||ly $\sigma_P \simeq q N_A \mu_p$

Intrinsic Concentration

In an Intrinsic S.C, as the temp is increased, more & more no. of covalent bonds are broken which results in a large electron and hole concentration. It is found that the intrinsic concentration varies with temp T, it is given by

$$n_i^2 = A_0 T^3 e^{-E_{G0}/KT}$$

where E_{G0} → The forbidden energy gap at 0°K (eV).

K → Boltzman Constant (eV/°K).

A_0 → Constant which is independent of temp

T → Temperature (°K).

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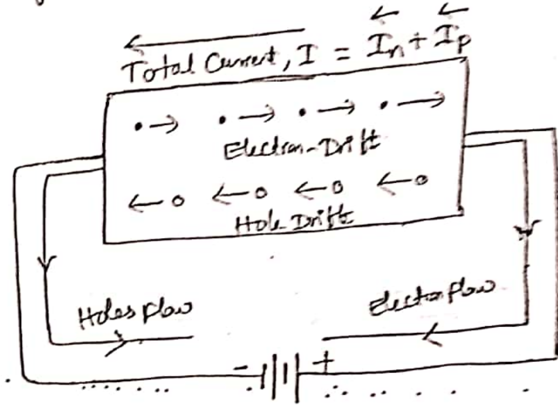
Drift current

If a battery is Connected across a S.C bar as shown in fig.



Battery

then electrons being negative charged particles moves towards the positive terminal of the battery and holes being positive charged particles moves towards the negative terminal of the battery. Hence, the movement (drift) of holes and Electrons contribute to electric current. This is Called as drift Current.

Diffusion Current

Let us Consider a S.C bar in which the concentration of charge carriers (electrons or holes) in one region is greater than the other region of the S.C

High charge Concentration | Low charge Concentration

⇒ Diffusion Current

→ Distance (x)

Because of charge gradient, the charge carriers in the high Concentration region move towards the Low Concentration region. This process is Called diffusion.

and thus produced electric current is called as diffusion current.
The current density due to this diffusion is proportional to the carrier density gradient.

Current density due to hole diffusion is given by

i.e, $J_p \propto \frac{dp}{dx}$ $\quad \because \frac{dp}{dx}$ = Concentration gradient
↳ change in the concentration w.r.to 'x'

$J_p = q D_p \frac{dp}{dx}$ $\quad J_n \propto \frac{dn}{dx}$

$\frac{dp}{dx}$ = Slope of the graph

& Current density due to electron diffusion is given by

$$J_n = +q D_n \frac{dn}{dx}$$

where D_p → Hole diffusion constant (m^2/s)

D_n → Electron diffusion constant (m^2/s)

$\frac{dp}{dx}$ → Density gradient of holes.

$\frac{dn}{dx}$ → Density gradient of electrons

D_p, D_n are diffusion constants given by Einstein's Relationship

V_T → voltage equivalent of temp.

$$\boxed{\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = V_T} = KT = \frac{KT}{q} = \frac{T}{11,600} = \frac{300}{11,600} = 26mV$$

$K \rightarrow 8.62 \times 10^{-5} eV/°K$

$K \rightarrow 1.38 \times 10^{-23} J/°K$

$$V_T = KT$$

At room temp i.e, at 27°C,

$$T = 273 + 27 = 300°K$$

$$V_T = KT = 8.62 \times 10^{-5} \times 300 = 0.026V \text{ (at } 300°K)$$

Total Current :- total current in a s.c may be possible to have the currents contributed by both charge gradient & electric field thus the total current is given by

$$J_n = nq\mu_n E + qD_n \frac{dn}{dx}$$

$$J_p = pq\mu_p E - qD_p \frac{dp}{dx}$$

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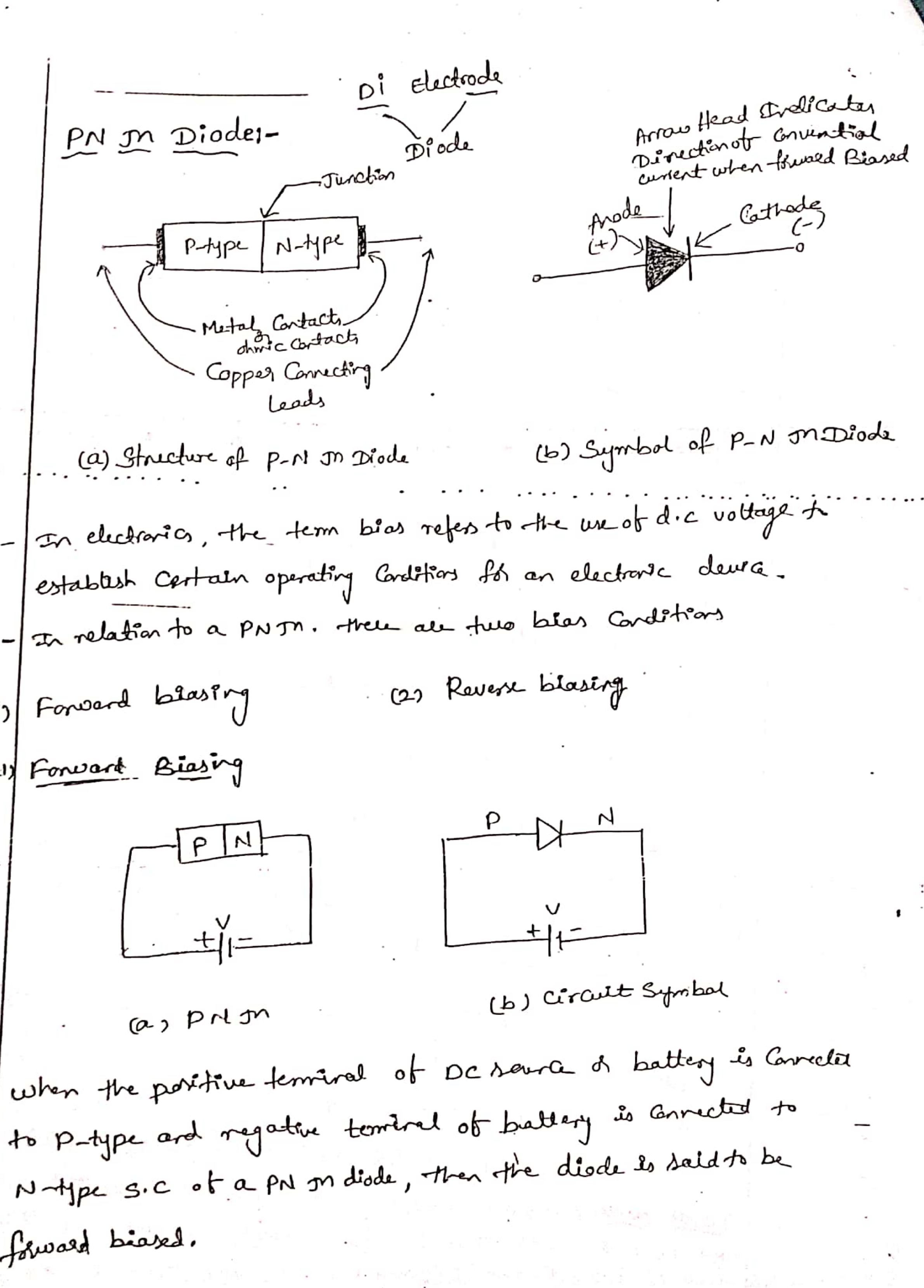
PN Jn Diode:-

Di Electrode → Diode



(a) Structure of P-N Jn Diode

(b) Symbol of P-N Jn Diode

- In electronics, the term bias refers to the use of d.c voltage to establish certain operating conditions for an electronic device.
- In relation to a PN Jn. there are two bias conditions

(1) Forward biasing (2) Reverse biasing

(1) Forward Biasing

(a) PN Jn

(b) Circuit Symbol

- When the positive terminal of DC source or battery is connected to P-type and negative terminal of battery is connected to N-type S.C of a PN Jn diode, then the diode is said to be forward biased.

Operation:-

- when the PN Jn is F.B, the holes (positive charges) on the P-side are repelled from the '+'ve terminal of the battery & are forced to move towards the Jn
  ||ly the electrons ('-'ve charges) on the n-side are repelled from the '-'ve terminal of the battery & are driven towards the Jn.
- Because of their acquired energy from the voltage source some of the holes & electrons enter the depletion Layer & recombine themselves. As a result, both the depletion region width & potential barrier reduces.
- when the bias voltage is progressively increased beyond the barrier potential (For Si $V_0 = 0.7V$, For Ge $V_0 = 0.3V$) then the electron from the N-side cross the PN Jn and are attracted by the '+'ve terminal of battery on the P-side.
- ||ly the holes from the P-side cross the PN Jn and are attracted by the '-'ve terminal of battery on the N-side.
- Both these charge carriers flow constitutes a Majority current.

$V_D = 0 \; = W_d$
$V_D > 0 \; = W_d'$
$V_D \uparrow \; W_d \downarrow$
Temp ↑ width current ↑

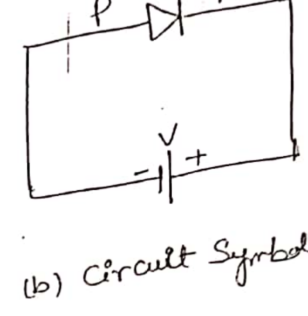
diffusion current
recombination current
Holes flow
electrons flow
P N
W
No External field
External field

(2) Reverse Biasing

P N

V

(a) PN Jn



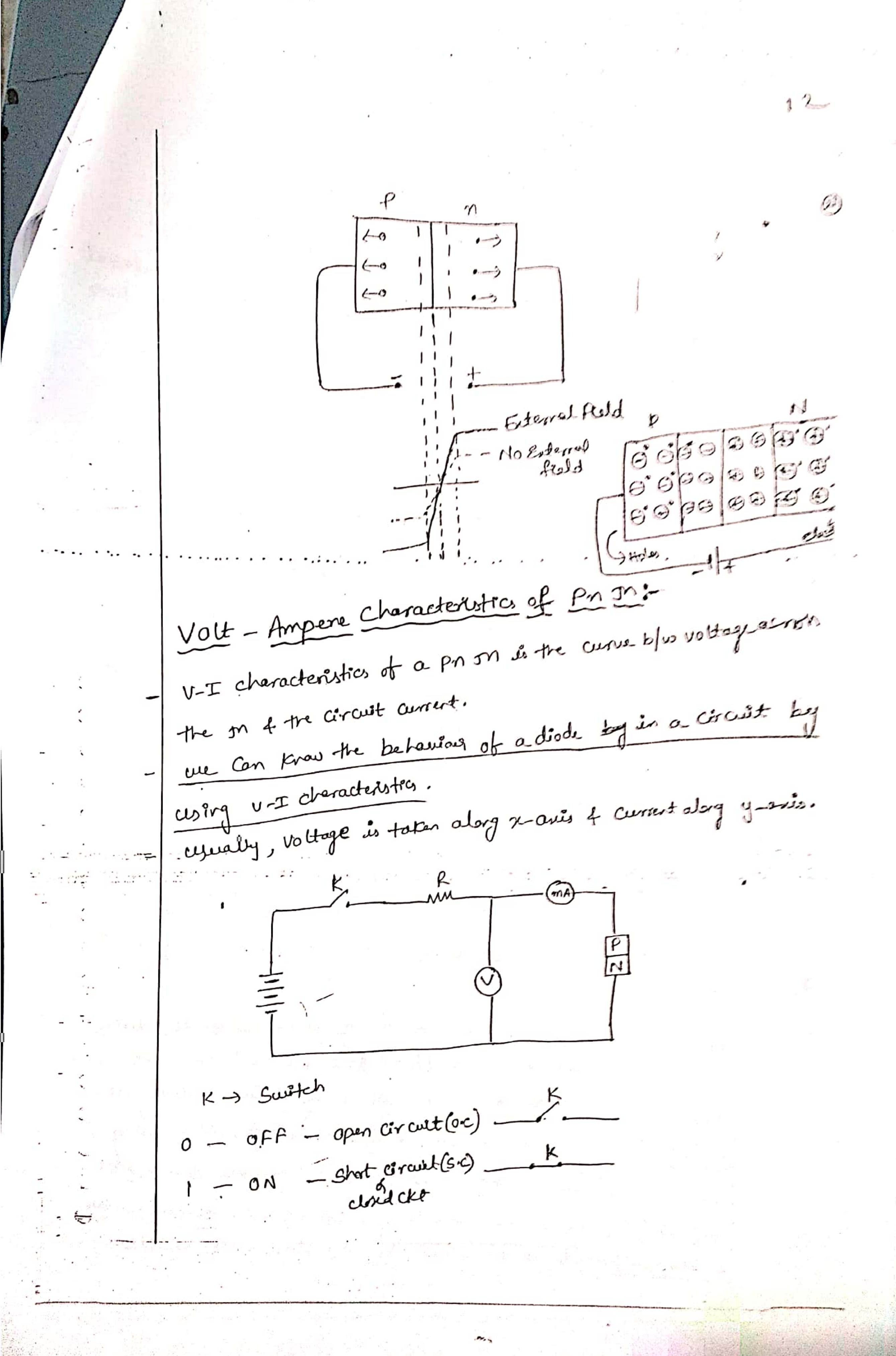
(b) Circuit Symbol

- when the positive terminal of DC source & battery is connected to N type S.C & negative terminal of battery is connected to P type S.C of a PN Jn as shown in fig. then the Jn is said to be Reverse Biased.

Operation:-

- when the PN Jn is reverse biased the holes in P-side are attracted towards -ve terminal of the battery.
- Electrons on the N-side are attracted towards +ve terminal of the battery.
- This action increases the depletion region and barrier potential as shown in figure.
- The Increase in barrier potential prevents the flow of Majority Carriers.

However, there are some electrons (Minority Carriers) on the P-side & holes (Minority Carriers) on the N-side, The barrier potential helps these Minority Carriers to cross the Jn. & a small magnitude of reverse current I_o flows across the Jn. This Current is called reverse Saturation Current.



External field

No External field

Holes.

Volt - Ampere Characteristics of Pn Jn :-

- V-I characteristics of a Pn Jn is the curve b/w voltage across the Jn & the circuit current.
- We can know the behaviour of a diode in a circuit by using V-I characteristics.
- Usually, voltage is taken along x-axis & current along y-axis.

K → Switch

0 — OFF — open circuit (O.C)

1 — ON — Short circuit (S.C) or closed ckt

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under steady state :- Diffusion current = Drift current

Net current = 0 in case of open circuited PN on diode.

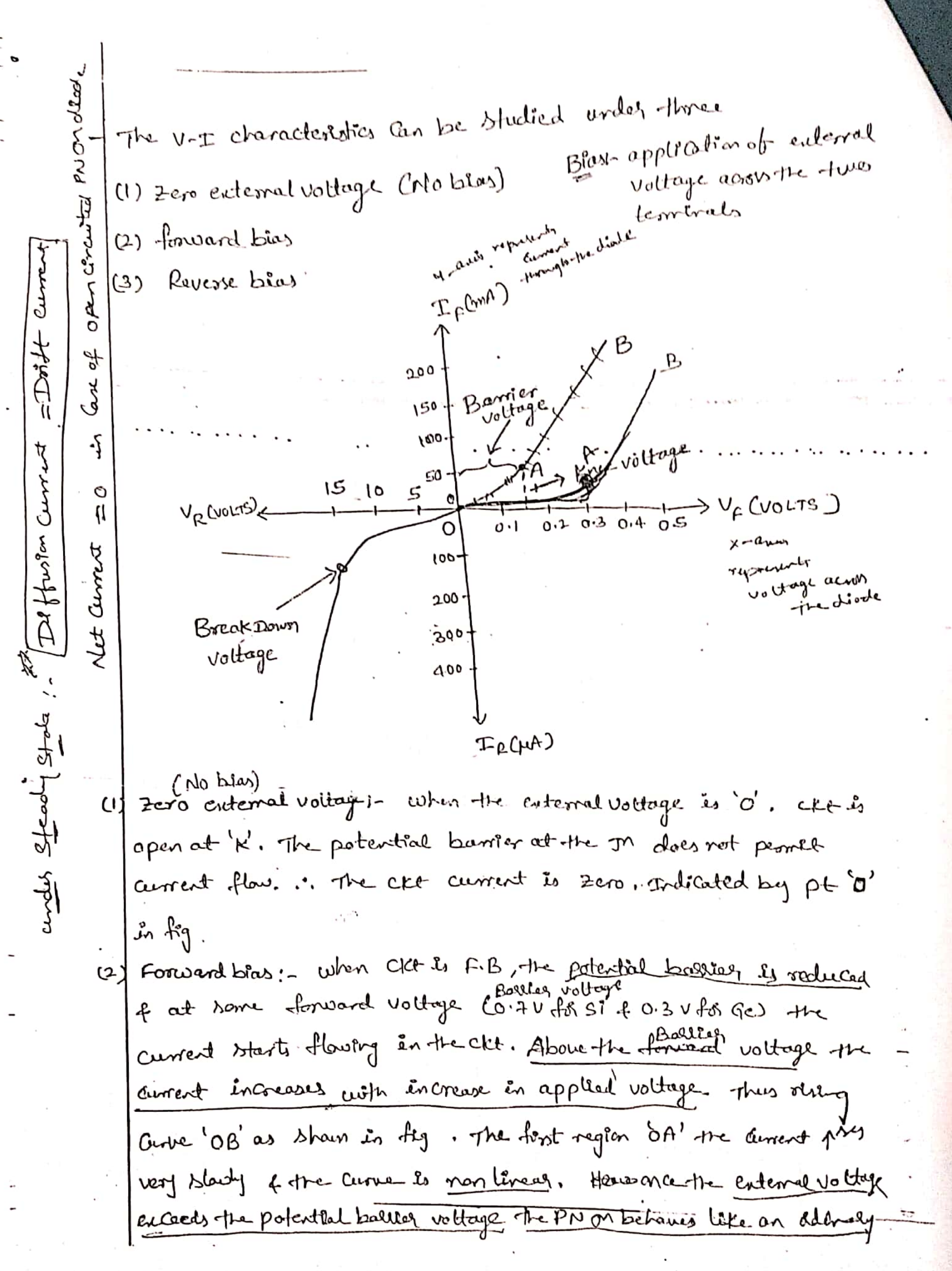
The V-I characteristics can be studied under three

(1) Zero external voltage (No bias)

(2) forward bias

(3) Reverse bias

Bias - application of external voltage across the two terminals



(1) Zero external voltage (No bias) :- when the external voltage is '0', ckt is open at 'K'. The potential barrier at the JN does not permit current flow. ∴ The ckt current is zero, indicated by pt 'O' in fig.

(2) Forward bias :- when ckt is F.B, the potential barrier is reduced & at some forward voltage (0.7 V for Si & 0.3 V for Ge) the current starts flowing in the ckt. Above the ~~forward~~ Barrier voltage the current increases with increase in applied voltage. Thus rising curve 'OB' as shown in fig. The first region 'OA' the current rises very slowly & the curve is non linear. Hence once the external voltage exceeds the potential barrier voltage the PN JN behaves like an ordinary

(24)

- The majority (hole) current I_{pp} is given by

$$I_{pp}(x) = I - I_{np}(x)$$

Quantitative Theory of PN Diode Currents

- when a forward bias is applied to a diode, holes are injected from the P-side into the N-side.

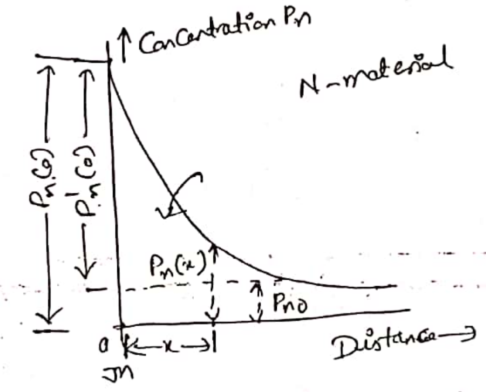
- The hole concentration in N-material is given by

$$P_n(x) = P_{no} + P_n'(0)\, e^{-x/L_p} \quad \text{—— (3)}$$

where P_{no} = Thermal equilibrium concentration

L_p = diffusion length of holes in N-material

x = distance from the junction where concentration is considered



Hole Concentration Components in N-material

the excess of hole concentration at $x=0$, i.e, $P_n'(0)$ is given by

$$P_n'(0) = P_n(0) - P_{no} \quad \text{—— (4)}$$

$\because J = \frac{I}{A} \Rightarrow I = JA$

we know that $J_p = -q D_p \frac{dp}{dx}$ (Refer Diffusion current)

$$I = -q D_p \frac{d P_n(x)}{dx} \cdot A \qquad \because P_n(x) = P_{no} + P_n'(0) e^{-x/L_p}$$

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$$P_n(x) = P_{n0} + P'_n(0)\, e^{-x/L_p}$$

$$\frac{d P_n(x)}{dx} = 0 + P'_n(0)\, e^{-x/L_p} \cdot \frac{-1}{L_p}$$

∴ Diffusion hole current in N side is given by

$$I_{Pn(x)} = + \frac{Aq D_p P'_n(0) \cdot e^{-x/L_p}}{L_p}$$

$e^0 = 1$

At Jn, i.e, $x = 0$

$$I_{Pn(0)} = \frac{Aq D_p P'_n(0)}{L_p} \rightarrow (5)$$

where A = Area of material

q = Magnitude of charge on hole

D_p = diffusion Constant for holes

L_p = diffusion Length of holes in N-material

$P'_n(0)$ = excess of hole Concentration at Jn.

Substituting the Value of $P'_n(0)$ from ④ in (5), we get

$$I_{Pn(0)} = \frac{Aq D_p}{L_p} [P_n(0) - P_{n0}] \rightarrow (6)$$

from Boltzmann relationship of Kinetic energy

$$P_n(0) = P_{n0}\, e^{V/V_T} \rightarrow (7)$$

This is known as Law of Jn.

Here V = applied voltage &

V_T = volt equivalent of temp $= \frac{KT}{q} = \frac{T}{11,600}$

where K is Boltzmann Const

Total diode current:- The total diode current I at x=0 is given by—

$$I = I_{pn}(0) + I_{np}(0), \longrightarrow (8)$$

(hole current at x=0) (electron current at x=0)

where $I_{pn}(0)$ = current caused by holes entering N-region

$I_{np}(0)$ = " electrons " P-region

The value of $I_{pn}(0)$ can be calculated by using eqs. (6) & (7). The

$$I_{pn}(0) = \frac{A q D_p}{L_p}\left[P_{no} e^{V/V_T} - P_{no}\right]$$

$$I_{pn}(0) = \frac{A q D_p P_{no}}{L_p}\left[e^{V/V_T} - 1\right] \longrightarrow (9)$$

$$\text{IIIly } I_{np}(0) = \frac{A q D_n n_{po}}{L_n}\left[e^{V/V_T} - 1\right] \longrightarrow (10)$$

Substituting the values of $I_{pn}(0)$ & $I_{np}(0)$ from eqs (9) & (10) in eq(8)
we get

$$I = \left(\frac{A q D_p P_{no}}{L_p} + \frac{A q D_n n_{po}}{L_n}\right)\left(e^{V/V_T} - 1\right) \longrightarrow (11)$$

or $I = I_o\left(e^{V/V_T} - 1\right)$

where

$$I_o = \left[\frac{A q D_p P_{no}}{L_p} + \frac{A q D_n n_{po}}{L_n}\right] \longrightarrow (12)$$

↓ Reverse Saturation Current

I_o depends on temp but independent of v/g

The reverse Saturation Current :-

We know that $P_{no} = \frac{n_i^2}{N_D}$ → (13) and $n_{po} = \frac{n_i^2}{N_A}$ → (14)

Sub (13) & (14) in (12)

$$I_0 = \left[\frac{A_q D_p \left(\frac{n_i^2}{N_D}\right)}{L_p} + \frac{A_q D_n \left(\frac{n_i^2}{N_A}\right)}{L_n} \right]$$

$$I_0 = A_q \left[\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A} \right] n_i^2$$

N_D = Concentration of donor atoms

N_A = Acceptor

where $n_i^2 = A_0 T^3 e^{\frac{-E_{Go}}{KT}}$.

$$n_i^2 = A_0 T^3 e^{\frac{-V_{Go}}{V_T}}$$

where V_{Go} = Voltage numerically equal to the forbidden gap Energy E_{Go} in electron volt

V_T = Voltage equivalent of temp $= \frac{T}{11,600}$

Limiting values of PN Jn diode :- PN Jn will perform satisfactorily only if it is operated within certain limiting values.

(i) Maximum forward current :- The highest current under F.B condition that can flow through the junction.

(ii) Peak Inverse voltage (PIV) :- Max reverse voltage that can be applied to the PN Jn. If V/g across Jn exceeds PIV under R.B, Jn gets damaged.

(iii) Max. Power Rating :- It is the max. power that can be dissipated at the Jn without damaging the Jn. Power dissipation is the product of voltage across the Jn ~~& current through the Jn~~.

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Applications of PN Jn diode:-

An ideal PN Jn diode has zero resistance when it is

& Infinite resistance when it is

Due to this characteristic the diode finds a number of applications as follows.

(1) rectifiers in dc power supplies
(2) Switch in digital Logic circuits used in Computers
(3) clamping network used as dc restorer in TV receiver and voltage multipliers
(4) clipping Circuits used as wave shaping circuits used in Computers, radars, radio & TV receivers.
(5) demodulation (detector) Circuits
(6) The Same PN Junction with different doping Concentra finds Special applications as follows:
(1) detector (APD, PIN photo diode) in optical Communication Circuits
(2) Zener diodes in voltage regulators
(3) Varactor diodes in tuning Sections of radio & TV recei
(4) Light emitting diodes in digital displays
(5) LASER diodes in optical Communications
(6) Tunnel diodes as a relaxation oscillator at micro wave fre

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Temperature Dependence of V-I characteristics of Diodes:-

The Boltzmann's equation of diode current is expressed as

$$I = I_0\left[e^{V/\eta V_T} - 1\right] \quad I = I_0 \exp.\left\{\left(\frac{V}{\eta V_T}\right) - 1\right\}$$

where, I = diode current (positive when F.B & negative when R.B)

I_0 = diode reverse current at temp T.

V = diode voltage (Positive for F.B & negative for R.B)

η = 1 for Ge & 2 for Si

$V_T = \frac{T}{11,600}$, a quantity in volts dependent upon temp.

T = temp of diode in (°K)

At room temp say 22°c, T = 295°K

& V_T = 0.025 Volt. Thus

$$I = I_0\left(e^{40V} - 1\right), \text{ for Ge}$$

& $$I = I_0\left(e^{20V} - 1\right), \text{ for Si}$$

where I_0 is the reverse saturation current at room temp. It can be shown that it

I_0 is temp dependent. It can be shown that it increases 7% per °c for both Ge & Si. And it doubles for every 10°c rise in temp.

Note:- Ge is more temp dependent than Si because its reverse current is approximately 1000 times larger.

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Ideal vs Practical - Resistance levels (Static and Dynamic)

- In Ideal Case, forward resistance should be zero & Reverse resistance should be infinite.

- In actual practice, no diode is an ideal diode because, neither it acts as a perfect conductor when F.B nor it acts as an insulator when it R.B.

- So we can say that, in F.B, it offers very small resistance (not exactly zero) and is called a forward resistance, whereas it offers a very high resistance (not exactly infinite) in reverse biased condition. This high resistance is known as reverse resistance.

Static or D.C Forward Resistance:-

In F.B, the opposition offered by the diode to the direct current flow is known as Static or D.C forward resistance. The ratio of D.C voltage across the diode to the D.C current flowing through it gives the value of D.C forward resistance. That is,

$$\text{Static resistance} = \frac{\text{Forward DC Voltage}}{\text{Forward DC Current}}$$

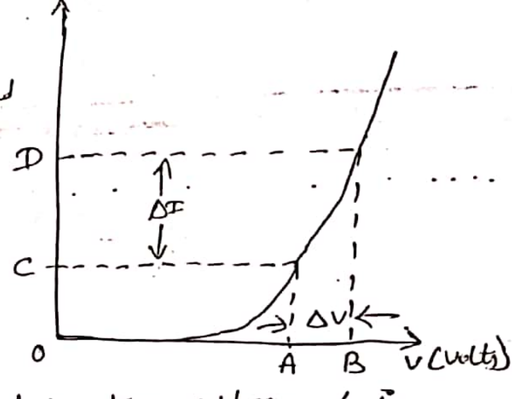
For any operating point, let the forward voltage be OA and the corresponding forward current is OB. ∴ the D.C forward resistance or static resistance is given by

$$R_f = \frac{OA}{OB} = \frac{V}{I}$$

I_F (mA) — Forward Current; B; O; Forward voltage A; V (volts)

Since the Shape of the diode characteristics is non linear, hence the value of R_F depends upon the exact location of the operating point on the curve.

Dynamic or A.C Forward Resistance



- Dynamic resistance of a PN-Jn diode may be defined as the resistance offered by the diode to the A.C signal is called dynamic or A.C resistance.
- Dynamic resistance of a diode is equal to the slope of forward V-I characteristics of the diode beyond the knee voltage & is given by,

$$\boxed{r_f = \frac{\text{change in voltage}}{\text{change in current}} = \frac{\Delta V}{\Delta I}}$$

From the fig, we observe that

change in forward voltage = AB
change in forward current = CD

$$\therefore \text{ Dynamic or A.C forward resistance } (r_f) = \frac{OB - OA}{OD - OC} = \frac{\Delta V}{\Delta I}$$

Expression of Dynamic Forward Resistance

we have diode current equation given as,

$$I = I_0 \left[e^{V/\eta V_T} - 1 \right] \quad \text{--- (1)}$$

Differentiating eq. (1) w.r.t. to voltage (V), we get,

$$\frac{dI}{dV} = I_0 \left[e^{V/\eta V_T} \right] \times \left(\frac{1}{\eta V_T} \right)$$

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$$\Rightarrow g = \frac{I_0 \cdot e^{V/\eta V_T}}{\eta V_T} \rightarrow (2)$$ $\left(\because \text{Conductance } (g) = \frac{dI}{dV}\right)$

from eq. (1), we get,

$$I_0 e^{V/\eta V_T} = I + I_0 \rightarrow (3)$$

using Eq. (3) in Eq. (2), we have,

$$g = \frac{I + I_0}{\eta V_T}$$

$$\Rightarrow r_f = \frac{1}{g} = \frac{\eta V_T}{I + I_0}$$

Since in F.B Cond'n, current, contributed by minority carriers is negligible i.e., $I >> I_0$. Thus,

$$\boxed{r_f = \frac{\eta V_T}{I}} \rightarrow (4)$$

For Ge & Si diodes the dynamic resistance at room temp (27°C) can be calculated by using the equation,

$$\boxed{r_f = \frac{26\,mV \cdot \eta}{I_F(mA)}} \rightarrow (5)$$ $(\because \text{At room temp } V_T = 26\,mV)$

For Ge diode : $r_f = \frac{26\,mV}{I_F(mA)}$ $(\because \eta = 1) \rightarrow (6)$

For Si diode : $r_f = \frac{52\,mV}{I_F(mA)}$ $(\because \eta = 2) \rightarrow (7)$

From eq. (4), it is clear that for F.B, $r_f \propto \frac{1}{I_F}$

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Reverse Resistance:-

It is the resistance offered by the PN jn diode under reverse bias condition. It is very large compared to the forward resistance, which is in the range of several MΩ.

Problem: Determine the forward resistance of a PN jn diode, when the forward current is 5mA at T = 300°K. Assume Silicon diode.

Sol:- Forward resistance of a PN jn diode, $r_f = \frac{\eta V_T}{I}$

$V_T = \frac{T}{11,600} = \frac{300}{11,600}$

$r_f = \frac{2 \times 300}{11,600 \times 5 \times 10^{-3}}$

$= 10.34\,\Omega$

$\frac{2 \times 26 = 52 \times 10^{-3}}{5 \times 10^{-3}}$

(31)

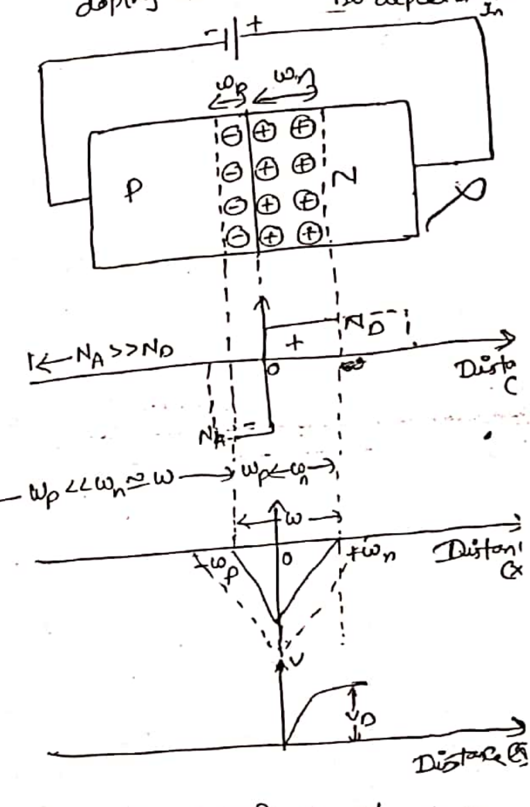
Transition and Diffusion Capacitance :-

There are basically two types of Capacitances associated with a P-N junction.

(1) Space charge or Transition Capacitance (C_T) :- Depletion capaci
This Comes in focus when the P-N Jn is reverse biased.

(2) Diffusion or Storage Capacitance (C_D) :-
This Comes into focus when the diode is forward biased.

Transition Capacitance :-



Consider a reverse biased PN Jn, the majority carriers move away from the Jn and the thickness of the depletion layer increases. The width of the depletion layer increases with increase in reverse bias voltage.

Now, the depletion region acts like an insulator or dielectric medium and P and N-regions on either side have low resistance and act as the conducting as shown in fig.

Since capacitor is a dielectric material (insulation) in b/w two conducting surfaces.

In this way, a P-N Jn may be regarded as a parallel plate capacitor.

The junction capacitance is called the space charge or transition capacitance. This is denoted by (C_T) and is defined as

$$C_T = \left|\frac{dQ}{dV}\right|$$

where dQ is the increase in charge resulting from a change dV in voltage.

- Capacitance is nothing but ability to store charge for an applied potential.
- PN Jn is able to store charge in depletion region which is immobile in nature for a given applied potential this we are considering it as a capacitance effect.
- In general capacitance $C = \frac{Q}{V}$
- But we are intrested in, for the charge in the potential how much is the charge stored in the device

$$C = \frac{\Delta Q}{\Delta V}$$

So, incremental capacitance C_T by

$$C_T = \left|\frac{dQ}{dV}\right|$$

dQ → increase in charge caused by a change dV.

$$C_T = \frac{i\,dt}{dV} \quad (\because i = \frac{dQ}{dt})$$

$$\Rightarrow i = C_T \frac{dV}{dt} \qquad i = \frac{dQ}{dt}$$

Current is rate of flow of charge per time

$$i = C_T \frac{dV}{dt}$$

C_T is transition region capacitance
space charge "
~~barrier~~ "
depletion region "

Capacitance is not a constant, but depends upon the magnitude of the reverse voltage.

So C_T is defined as, $C_T = \left|\frac{dQ}{dV}\right|$

An Alloy Junction :- & Step graded Jn — n type – Pentavalent PAI; p type Trivalent BAG

Consider a Jn in which there is an abrupt change from acceptor ions on one side to donor ions on the other side.

Such a Jn is formed experimentally.

For example, by placing indium, which is trivalent, against n-type Ge & heating the combination to a high temp. for a short time.

Some of the indium dissolves into the Ge to change the Ge from n to p type at the Jn. Such a Jn is called Alloy & fusion Jn.

It is not necessary the $N_A = N_D$

it is often advantageous to have an unsymmetrical Jn.

- acceptor impurity density is assumed to be much smaller than the donor concentration. $N_A << N_D$
- Since net charge must be zero, then

$$e N_A W_p = e N_D W_n$$

In N-side doping concentration is more, so width of depletion in N side is less

In P-side is less, in P side is more

we know that $C_T = \frac{dQ}{dV} \rightarrow (1)$

Now let us consider poisson's equation

$$\frac{d^2V}{dx^2} = \frac{qN_A}{\varepsilon} \rightarrow (2)$$

where ε is the permittivity of the S.C

Integrating above equation twice,

$$\iint d^2V = \iint \frac{qN_A}{\varepsilon} dx^2$$

$$\iint \frac{d^2V}{dx^2} = \iint \frac{qN_A}{\varepsilon} dx^2$$

$$V = \frac{qN_A}{\varepsilon} \iint 1\, dx^2 = \frac{qN_A}{\varepsilon} \int \left(\int 1\, dx\right) dx = \frac{qN_A}{\varepsilon} \int x\, dx = \frac{qN_A}{\varepsilon} \frac{x^2}{2}$$

$$V = \frac{qN_A x^2}{2\varepsilon} \rightarrow (3) \quad \left(\because \iint dx^2 = \frac{x^2}{2}\right)$$

At the ..., $x = \omega$, $V = V_B$

$$V_B = \frac{qN_A}{\varepsilon} \frac{\omega^2}{2} \rightarrow (4)$$

differentiate eq. (4) w.r.to V. we get

$$\frac{d(V_B)}{dV} = \frac{d}{dV}\left[\frac{qN_A}{\varepsilon} \cdot \frac{\omega^2}{2}\right] \qquad \boxed{V_B \propto \omega^2}$$

$\because \omega$ is the function of V,

$$1 = \frac{qN_A}{\varepsilon} \frac{d}{dV}\left[\frac{\omega^2}{2}\right]$$

$\frac{d}{dV}(\omega^2) = 2\omega \cdot \frac{d\omega}{dV}$

$\frac{d}{d\omega}(\omega^2) = 2\omega$

$$1 = \frac{qN_A}{\varepsilon} \cdot \frac{1}{2} \cdot 2\omega \frac{d\omega}{dV}$$

$$1 = \frac{qN_A \omega}{\varepsilon} \frac{d\omega}{dV}$$

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$$\frac{dw}{dV} = \frac{\varepsilon}{q N_A w} \rightarrow (5)$$

$\because Q = nqAL$ (for Conductor)

for $n = N_A$, $L = w$ (Junction width)

$$\therefore Q = N_A q A w \rightarrow (6)$$

differentiate w.r.to V

$$\frac{dQ}{dV} = N_A q A \cdot \frac{dw}{dV} \rightarrow (7)$$

$$\because \frac{dw}{dV} = \frac{\varepsilon}{q N_A w}$$

$$= N_A q A \cdot \frac{\varepsilon}{q N_A w}$$

$$\frac{dQ}{dV} = \frac{\varepsilon A}{w}$$

But $\frac{dQ}{dV}$ is the transition Capacitance C_T hence

$$\boxed{C_T = \frac{\varepsilon A}{w}}$$

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Diffusion Capacitance (C_D):-

when a PN jn is F.B, a capacitance which is much larger than the transition capacitance comes into picture. This type of capacitance is called the diffusion capacitance (C_D).

$$C_D = \frac{dQ}{dV}$$

we have $I = \frac{Q}{\tau}$ ($\because t = \tau \rightarrow$ mean life time of charge carriers)

$\Rightarrow Q = I\tau \longrightarrow (1)$

from Diode equation for F.B,

$$I = I_0 e^{V/\eta V_T} \longrightarrow (2)$$

Sub (2) in (1)

$$Q = \tau (I_0 e^{V/\eta V_T}) \longrightarrow (3)$$

differentiate eq.(3) w.r.to V, we get

$$\frac{dQ}{dV} = \tau \cdot I_0 \frac{d}{dV} (e^{V/\eta V_T})$$

$(\because C_D = \frac{dQ}{dV})$ $\therefore C_D = \tau I_0 \cdot \frac{e^{V/\eta V_T}}{\eta V_T}$

$$= \frac{\tau I}{\eta V_T}$$ $(\because I = I_0 \cdot e^{V/\eta V_T})$

$$\therefore \boxed{C_D = \frac{\tau I}{\eta V_T}}$$

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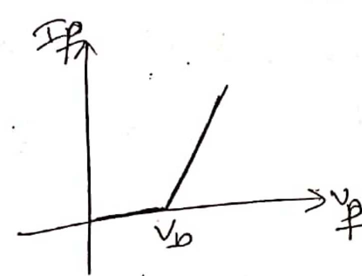
3

Diode Equivalent Circuits

- An Equivalent circuit is a Combination of Elements (like R, L, C etc) properly chosen to best represent the actual characteristics of device in a particular operating region.
- we Canot use circuit analysis techniques like Norton, theveren to find out parameters like voltage, Current & resistance with the actual device.
- we Can replace actual device with equivalent circuits.

3 types
Piece wise linear equivalent ckt
(1) Constant voltage drop or Simplified equivalent ckt.
(2) Ideal equivalent circuit
(3) Piece -wise Linear Equivalent circuit

Assumption
→ linear even with small non-linearity
→ After conducting (ie, after V_b) it Can be represented in linear form



$$slope = \tan\theta$$

$$\tan\theta = \frac{Perpendicular}{Base}$$

$$m = \frac{y}{x} = \frac{I_f}{V_f}$$ (m = slope)

$slope(m) = \frac{I_f}{V_f}$; from ohm's law $\frac{1}{slope(m)} = \frac{V_f}{I_f} = r_f$

$$r_f = \frac{1}{slope}$$

→ If the V-I characteristics is assumed as linear then forward resistance is Constant.
→ Hence due to this Concept we can replace nonlinear curve by straight line. This type of ckt is known as piece wise linear model.

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V_f + − I_f ≡ V_b r_d

V_f + − I_f ≡ + V_f r_d V_b r_d

V_f ↳ represent the direction of current

V_b → barrier potential will oppose the flow of current

r_d → diode resistance

Equivalent circuit of Piece wise linear model

Example:-

I_D 10mA 0.8V V_b V_D

V_b

Si → 0.7V

Ge → 0.3V

$$r_d = \frac{(0.8 - 0.7)}{(10 - 0) \times 10^{-3}}$$

(Si; at 0.8V, at 0.7V)

$r_d = 10\Omega$

2) Constant voltage drop | Simplified model

In electrical circuits, resistance of diode is very small as compared to other elements. So, it can be neglected.

Assumptions:-

(1) linear curve instead of small non_linearity

(2) $r_d = 0$

$$\frac{1}{slope} = 0 \Rightarrow slope = \infty$$

$\tan\theta = \infty$

$\theta = \tan^{-1}(\infty) \Rightarrow \boxed{\theta = 90^\circ}$ in this model

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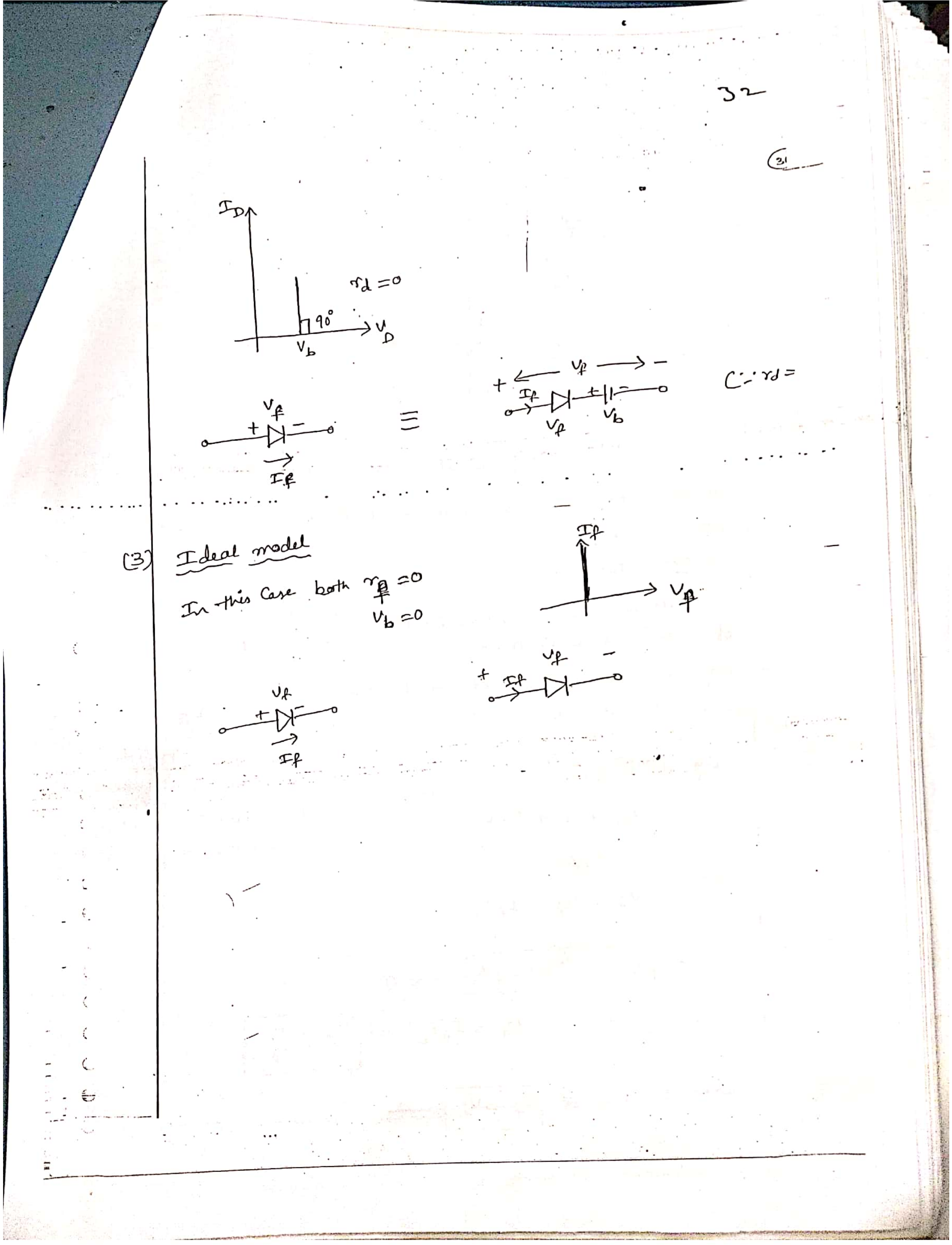

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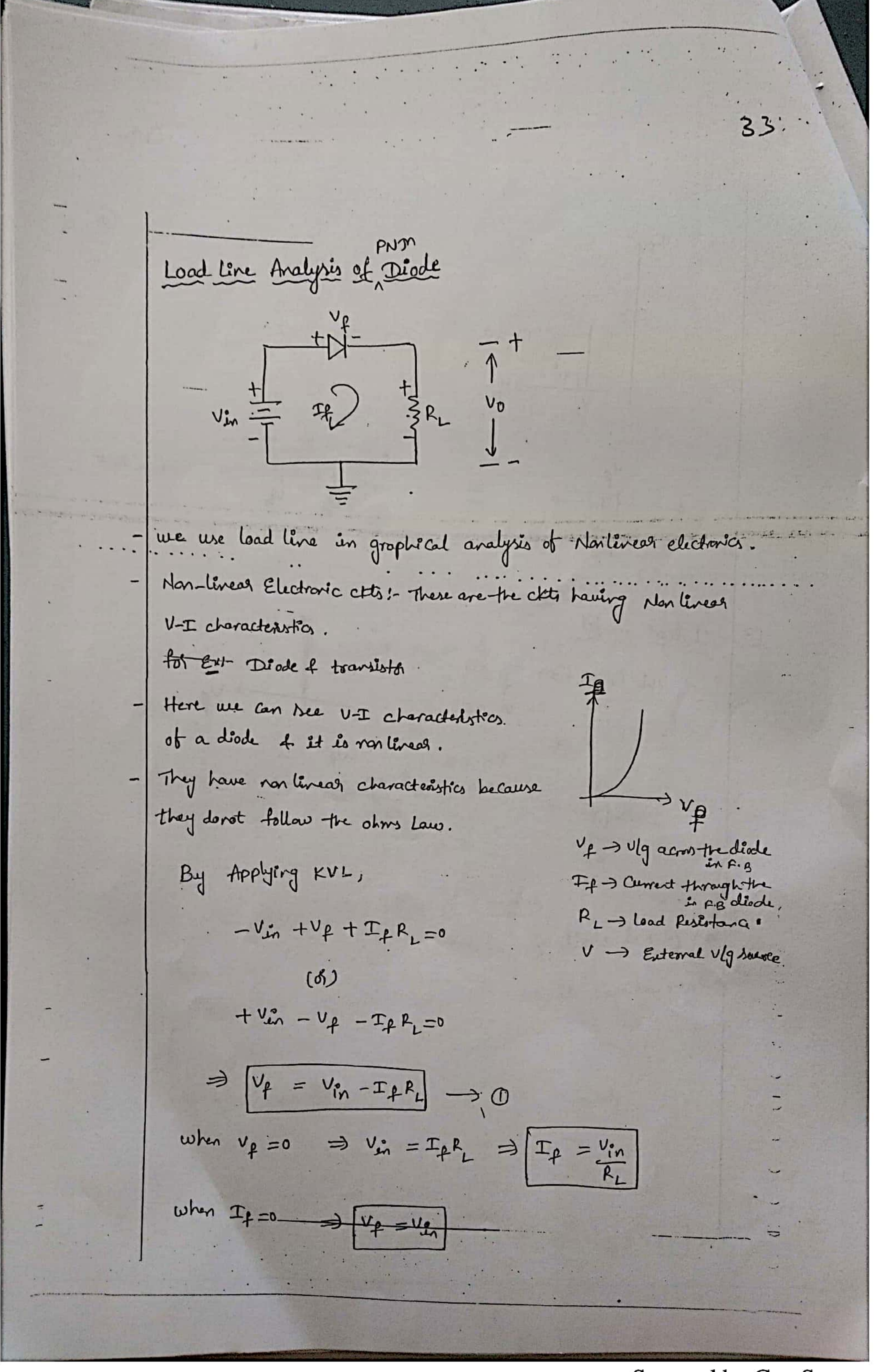

Load Line Analysis of PN Diode

- we use load line in graphical analysis of Nonlinear electronics.
- Non-linear Electronic ckts :- These are the ckts having Non linear V-I characteristics.

  ~~for Ex~~- Diode & transistor.

- Here we can see V-I characteristics of a diode & it is non linear.
- They have non linear characteristics because they donot follow the ohms Law.

$V_f \rightarrow$ v/g across the diode in F.B

$I_f \rightarrow$ Current through the diode in F.B

$R_L \rightarrow$ Load Resistance.

$V \rightarrow$ External v/g source.

By Applying KVL,

$$-V_{in} + V_f + I_f R_L = 0$$

(or)

$$+V_{in} - V_f - I_f R_L = 0$$

$$\Rightarrow \boxed{V_f = V_{in} - I_f R_L} \rightarrow (1)$$

when $V_f = 0 \Rightarrow V_{in} = I_f R_L \Rightarrow \boxed{I_f = \frac{V_{in}}{R_L}}$

when $I_f = 0$ ~~$\Rightarrow \boxed{V_f = V_{in}}$~~

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Slope of the Load Line

$V_{in} = I_f R_L + V_f$

divide B.S by R_L

$$\frac{V_{in}}{R_L} = I_f + \frac{V_f}{R_L}$$

(or) $I_f = \frac{-V_f}{R_L} + \frac{V_{in}}{R_L}$

$y = mx + c$ $x = V_f$, $y = I_f$

$c = \frac{V_{in}}{R_L}$, $m = -\frac{1}{R_L}$

I_f (mA)

$\frac{V_{in}}{R_L}$ $(\frac{V_{in}}{R_L}, 0)$

Load Line

Q-pt

I_fQ

V_fQ V_{in} (0, V) V_f

Q-pt or Quiescent pt

(or) operating pt $\equiv (I_{fQ})$

By changing R_L, Q pt will also change

If $\uparrow R_L$, Q pt will change, Load line will change

Break down Mechanisms in Diode

- In reverse biased Condition as long as the reverse voltage is less than breakdown voltage, the diode current is small and almost Constant at I_0.
- But when reverse voltage increases beyond certain value; large diode current flows. This is Called breakdown of diode and Corresponding voltage is Called reverse breakdown voltage (V_{BR}) of diode.
- There are two mechanisms due to which the breakdown may occur in the diode.

These are (1) Avalanche Break down

(2) Zener Break down

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Zener Diode:-

- when the reverse voltage reaches breakdown voltage in normal PN Jn diode, the Current through the Jn and the power dissipated at the Jn will be high. Such an operation is destructive & the diode gets damaged.
- whereas diodes Can be designed with adequate power dissipation Capabilities to operate in the breakdown region. are Such a diode is known as Zener diode. Zener diode is heavily doped than the ordinary diode.
- operation of Zener diode is same as that of ordinary PN diode under F.B Condition.
- where as under R.B Condition, breakdown of the Jn occurs.
- the breakdown voltage depends upon the amount of doping.

I_F (mA)

V_F

V_R

I_R (μA)

If the diode is heavily doped, depletion layer will be thin & Consequently, breakdown occurs at Lower reverse voltage and further, the breakdown voltage is sharp. whereas a lightly doped diode has a Higher breakdown voltage.

- Thus breakdown voltage Can be Selected with the amount of doping.

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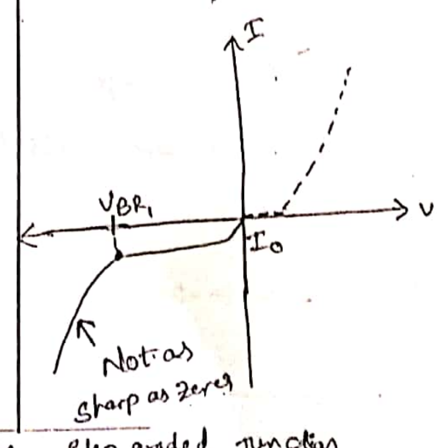
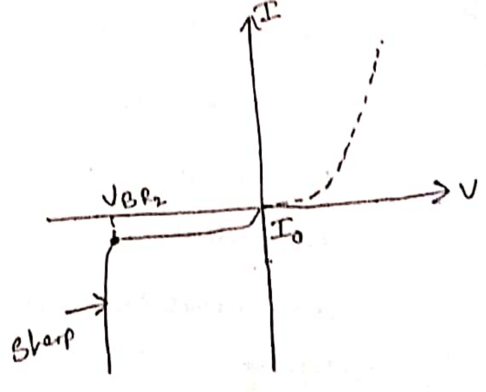
	Avalanche Breakdown	Zener Breakdown
1.	Breaking of Covalent bonds is due to Collision of accelerated charge Carriers having large velocities and Kinetic energy with adjacent atoms. The process is called Carrier multiplication.	Breaking of Covalent bonds is due to intense electric field across the narrow depletion region. This generates large no. of free electron to Cause breakdown.
2.	This occurs of Zener diode with V_{BR} greater than 6V.	This occurs for Zener diodes with V_{BR} less than 6V.
3.	The temperature Coefficient is positive.	The temperature Coefficient is negative.
4.	The breakdown voltage increases as the junction temperature increases.	The breakdown voltage decreases as junction temperature increases
5.	The occurs for lightly doped diodes.	occurs for heavily doped diode
6.	The V-I characteristics is not as sharp as Zener breakdown in breakdown region.	The V-I characteristics is very sharp in breakdown regime.





7.	Step graded junction	Linear Graded Junction

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Applications :-

- from the Zener characteristics, under the R.B condition, the voltage across the diode remains almost constant although the current through the diode increases. Thus, the voltage across the Zener diode serves as a reference voltage. Hence, the diode can be used as a voltage regulator.

R, I_L, I_Z, V_Z, R_L, V_{in}, V_0, +, −

Symbol

as a voltage regulator

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Zener Diode:

Zener diode is a reverse biased heavily-doped Silicon P-N junction diode which is operated in the break-down region.

The Symbol of zener diode is shown in fig().

This is similar to a normal diode except the line representing the cathode is bent at both ends i.e., like the letter z for zener.

fig(): Symbol of zener diode

V-I characteristics:

The V-I characteristics of zener diode under forward bias and Reverse bias is shown in fig:().

When a zener is Forward biased its characteristics are just as those of ordinary diode.

The fig() shows that when reverse applied voltage increased, at V_Z current increases greatly. This voltage is called as zener voltage (V_Z) (or) breakdown voltage.

fig:() V-I characteristics of zener diode.

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Breakdown Mechanism :

There are two mechanism of the breakdown.

(i) Zener breakdown :

Zener breakdown takes place in very thin junction when both sides of junctions are heavily doped then the depletion layer becomes narrow. When a small reverse bias voltage is applied, a very strong electric field is set up across the thin depletion layer. This field is enough to break the covalent bonds. Now very large number of electrons and holes are produced, which constitute the reverse current (Zener current).

(ii) Avalanche breakdown :

This type of breakdown takes place when both sides of jn are lightly doped and the depletion layer is large.

- If applied reverse biase increases, the field across the jn increases. Thermally generated carriers (minority) acquire a large amount of energy from the this field and starts distrupt covalent bond by colliding with immobile ions and creates new electron-hole pairs. These new carriers again acquire sufficient energy from the field and collide with other immobile ions and generating further electron-hole-pairs. This process is cumulative in nature and results in generation of avalanche (flood) of charge carriers within a short time.

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.'. mechanism of carrier generation is known as avalanche multiplication.

Application of zener diode:

→ Used as a voltage regulator.

→ Used as peak clipper

Tunnel Diode:

Tunnel diode, is a Extremely heavily doped, thin junction diode. Also called Esaki diode.

An ordinary PN junction diode is doped by impurity atoms in the concentration 1 part in 10^8. With this amount of doping, the width of depletion layer is wide and exists a potential barrier across the junction. Due to this potential barrier majority charge carriers can't cross the junction.

If the concentration of impurity atoms is greatly increased in a PN Junction i.e., 1 part in 10^3, the device characteristics are completely changed. Under this condition, a very thin depletion layer forms, and the carriers cross the junction even if they do not have enough energy to overcome the potential barrier (0.3-Ge & 0.7-Si). This is known as tunneling phenomenon

Symbol: A —▷|— K

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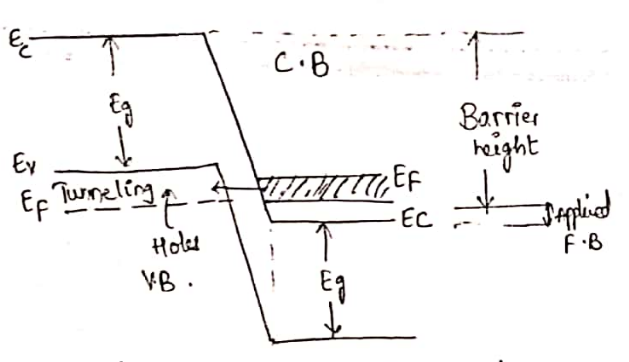
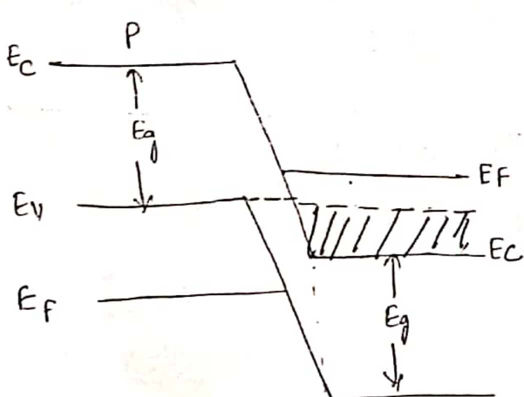
V-I characteristics:

V-I characteristics of Tunnel diode can be explained well using Energy band structure of a heavily doped P-N diode. Energy band diagram & V-I characteristics are as shown in fig:( ),( ) respectively.



(a) when small forward biased

(b) Full tunnelling



(c) After Peak voltage

(d) After Valley Voltage

→ Consider now that a forward bias is applied to the diode, so that the potential barrier is decreased below E_0. Hence the n-side levels must be shift upward with respect to those on the p-side, and the energy-band picture for this situation is indicated in fig:( )a.

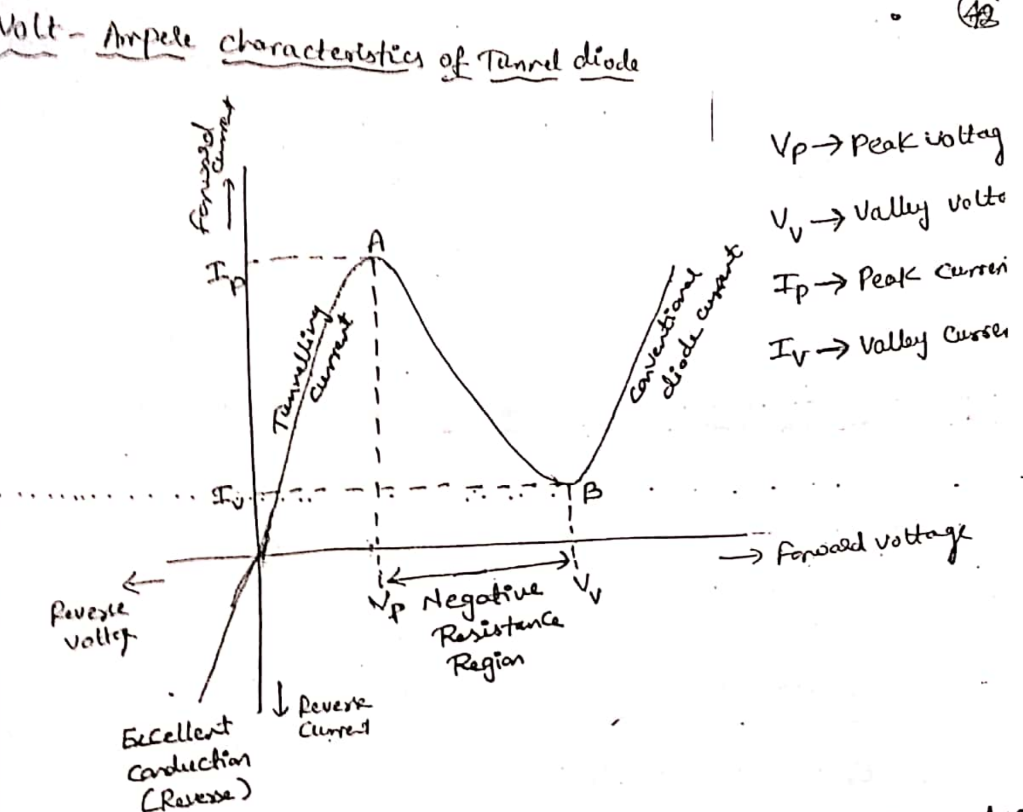
It shows that energy levels of electrons occupied in the conduction band of the n-material (the heavily shaded level) are same as allowed empty states (holes) in the valance band of the p-side. Hence electrons will tunnel from the n- to the p-material, giving rise to the forward current, as shown in V-I char. fig( )

→ As the forward bias is increased further, the condition shown in fig( )b. is reached. Now maximum number of electrons can leave right side of the Jn, and tunnel through the barrier to the left side, giving rise to the peak current I_P in fig( ), and the voltage is peak voltage V_P.

→ If still more forward bias is applied, the situation in fig( )c. is obtained and the tunnelling current decreases. Finally, at even large forward bias, fig( )d. is obtained, there are no equal energy levels in both side, so tunnelling stops. The point is known as valley point (V_V, I_V), After this point if forward bias increased, it ~~actes~~ acts as a ordinary diode.

(42)

Volt - Ampere characteristics of Tunnel diode



→ As soon as the F.B is applied significant current is produc

→ The current quickly reaches its peak value I_p. when forward voltage reaches a value V_p. It is denoted by point A.

→ when foward voltage is further increased (i.e, $> V_p$), the current starts decreasing to I_V corresponding to valley voltage (V_V). This is denoted by point B.

→ Thus from point A to B, the current decreases as voltage increases, this results in a negative resistance.

→ The position AB constitutes the most useful property of the diode. That is instead of absorbing power, a -ve resistance produc power.

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→ For voltage greater than V_V current starts increasing as in case of a conventional diode.

Application of Tunnel diode:-

(1) ultra high speed switching device

(2) High frequency oscillator (Microwave oscillator)

(3) Digital design

Comparision of Zener and tunnel diodes

Feature	Zener	Tunnel
Construction	Made up of Si with two layers (P-N)	Made up of germenium or gallium arsenide with two layers (P-N), gallium arsenide is prefered
Doping	Heavily doped	Heavily doped
operation	Acting as breakdown device at reverse bias	Exhibits negative resistance at F.B
Applications	Constant voltage source Voltage regulator	Microwave oscillator ultra high speed switching device

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Varactor diode :-

- It is also termed as voltage variable Capacitance diode, or VariCap,
- we know that the depletion region in a P-N Jn forms a barrier which seperates the +ve & -ve charges on each side of the Jn and the depletion region acting like a dielectric.

Thus a PN Jn possesses Junction Capacitance.

- when a reverse bias is applied, the junction Capacitance decreases because the depletion region width increases. $\because C_T = \frac{\varepsilon A}{W}$

* A varactor diode is specially manufactured P-N Junction with suitable impurity Concentration and operated under R.B conditions so as to yield a variable Junction Capacitance.

Symbol — Equivalent circuit

working :-

The circuit of R.B varactor diode is shown in fig

when R.B voltage is increased, the depletion layer becomes widened. This increases the dielectric thickness. As a result the capacitance is reduced. on the other hand, when reverse bias voltage is decreased the depletion layer becomes narrower. This decreases the dielectric thickness. In this case the Capacitance is increased.

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Fig. shows the variation of diode-Capacitance as a function of applied R.B voltage. From the fig. the variation of Capacitance is maximum when R.B voltage is zero & it reduces non-linearly as the R.B voltage increases.

Diode Capacitance

0

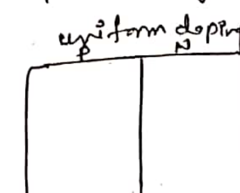
Reverse Voltage

fig:- Reverse voltage verses diode Capacitan

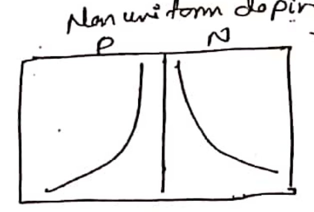
Types of Varactor diode:-

There are two types of varactor diode profile:

(i) Abrupt doping profile



(ii) Hyper abrupt profile



→ In abrupt doping profile, the doping is uniform on both sides of the junction and the tuning range of Capacitance is 4:1

→ In Hyper abrupt profile, the doping level increases towards the junction as shown in fig.(ii). In this Case due to smaller depletion layer, a large Capacitance occurs at the junction. So, a small change in reverse bias voltage makes a larger variation in Capacitance. Due to this reason, tuning range is 10:1.

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Applications:-

1. varactor diode is used in automatic frequency control.
2. It is used in tuning circuits.
3. used in adjustable band pass filters.

** SCR (Silicon Controlled Rectifier)

Anode A, P, N, P, N, J_1, J_2, J_3, G (Gate), K Cathode

A, G, K

→ It is a four layer semiconductor device being alternate of P-type & N-type Silicon.

→ It Consists of 3 Junctions J_1, J_2, J_3 & 3 terminals Anode (A), Cathode (K) & Gate (G).

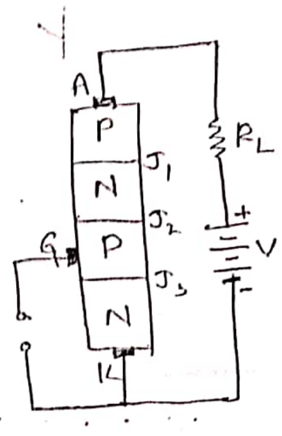
→ SCR is a unidirectional device. (J_1 & J_3 operates in F.B & J_2 in R.B)

Operation:-

The operation of SCR can be studied (i) when the gate is open

(ii) when the gate is +ve w.r.to Cathodes

(i) when the gate is open:-



It is shown in the fig, no voltage is applied at the gate. From the fig. J_1 & J_3 are F.B while the junction J_2 is R.B. Due to R.B J_2, no current flows through R_L and hence SCR is cut-off. However when the anode (F.B) voltage is increased a certain critical value (Breakover voltage) is reached then the junction J_2 breaks down. SCR now starts conducting heavily and is said to be in ON state.

(ii) when the gate is positive w.r.to cathode:-

As shown in fig: J_3 is F.B, so at very small gate voltage gate current starts flowing. Due to the gate current, anode current increases. In an extremely small time, junction J_2 breaksdown & SCR conducts heavily.

once SCR starts conducting, the gate loses all controls. That is to turn OFF SCR, supply voltage is reduced to zero.

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Points to remember:-

→ If the anode is made '-'ve w.r.to Cathode i.e, J_1 & J_3 R.B. SCR is blocked & no current flows. If '-'ve voltage increases breakdown occurs & SCR is destroyed. It shows that SCR is unidirectional device.

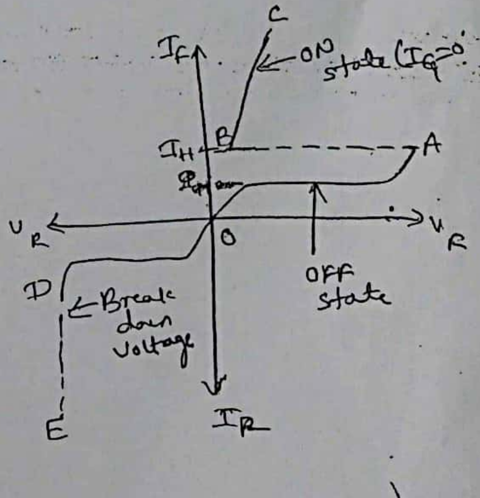
→ SCR can turn ON either by keeping the gate open & making the supply voltage equal to breakover voltage or by applying small voltage (typically 1.5V) to the gate & making the supply voltage less than breakover voltage.

→ Either SCR does not conduct or conducts heavily. Thus SCR behaves like a switch.

→ To turn off SCR, supply voltage is reduced to zero.

V-I characteristics of SCR:-

→ V-I characteristics of SCR for $I_G=0$ (i.e gate is open) is shown in fig.



Forward Characteristics:-

→ When the anode is '+'ve w.r.to Cathode, the characteristics is known as forward characteristics. It is shown in fig1 by OABC curve.

- When the supply voltage is increased from zero, a point A is reached then SCR starts conducting. The voltage at point A is called as forward breakover voltage.
- At this voltage junction J_2 breaks down & SCR switches suddenly to high conducting state.
- Breakover voltage is defined as the minimum forward voltage at which SCR starts conducting heavily.
- At this movement, the voltage across SCR suddenly drops as shown by dotted curve AB.
- At point B current is called as holding current I_H.

* The holding current is the maximum anode current at which SCR is turned off from ON condition.

* There is a maximum value of anode current which an SCR is capable of passing without destruction. This is known as forward current rating and is expressed by I_F (about 30 A to 100 A).

→ Reverse biased characteristics:-

→ When anode is -ve w.r.to cathode, the characteristics is called as reverse characteristics.

→ When the anode (applied) voltage is gradually increased, at first the anode current remains small (i.e, leakage current)

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UNIT-II

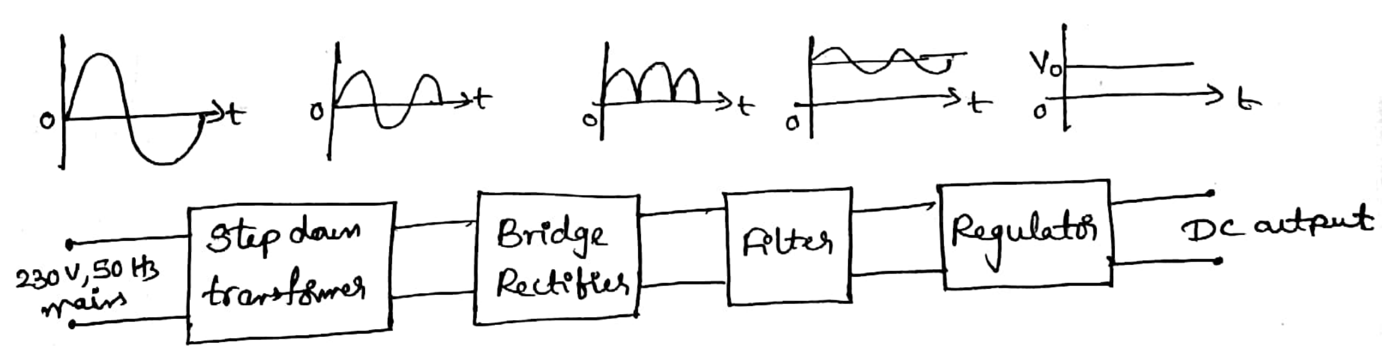
Rectifiers and Filters

INTRODUCTION:-

All electronic circuits need dc power supply either from battery & power pack units. It may not be economical & convenient to depend upon battery power supply. Hence, many electronic equipment contain circuits which convert the ac supply voltage into dc voltage at the required level.

1. Linear mode power supply (LMPS) :- ac to dc
2. Switched mode power supply (SMPS) :- dc to dc, dc to ac - Inverter

- ac (230V, 50 Hz)



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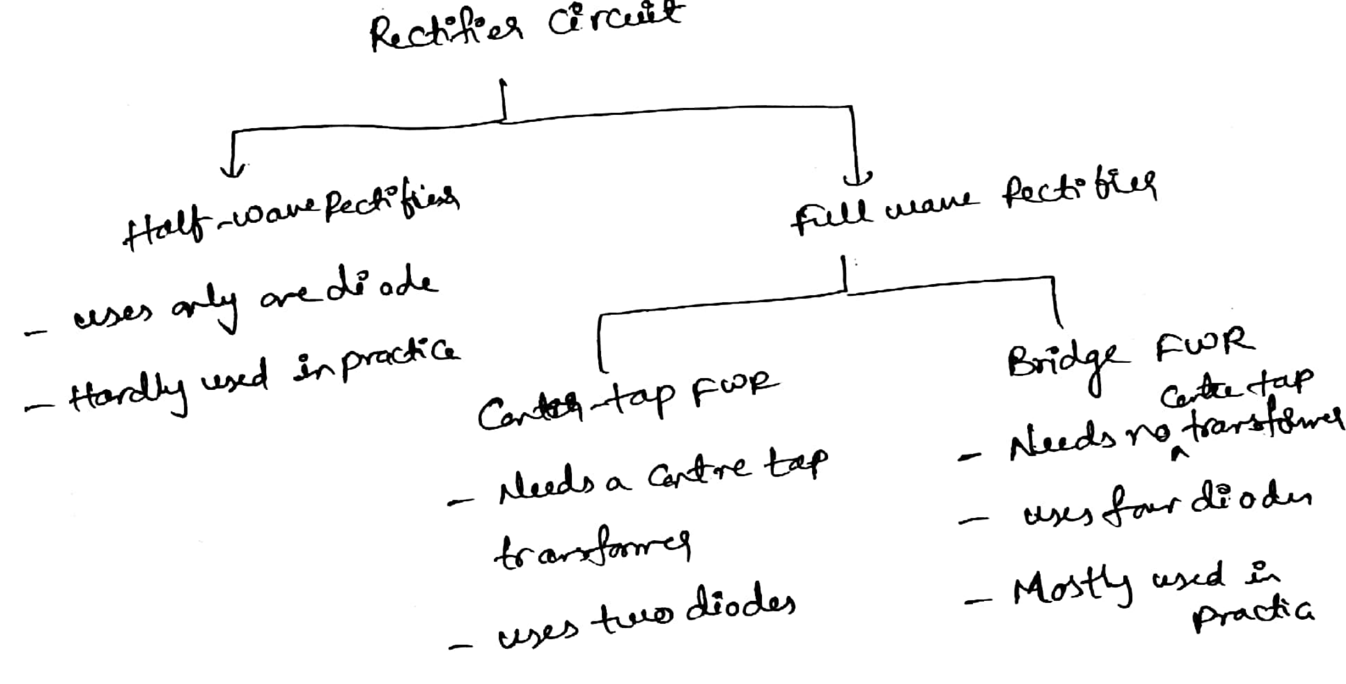
Rectifier:-

Rectifier is defined as an electronic device used for Converting ac voltage into unidirectional dc voltage.

- A Rectifier utilizes unidirectional Conduction device like a vacuum diode & PN junction diode.
- Rectifiers are classified depending upon the period of Conduction as Half-wave rectifier and Full-wave rectifier.



- Centre tap transformer is expensive, so we are going for Bridge FWR.

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UNIT-II

Rectifiers and Filters

The P-N junction diode as rectifier:-

In diode readily conducts under F.B

F.B → diode conducts

R.B → diode doesnot conduct

If an alternating v/g is applied across the diode terminals,

diode is F.B → during +ive half-cycles

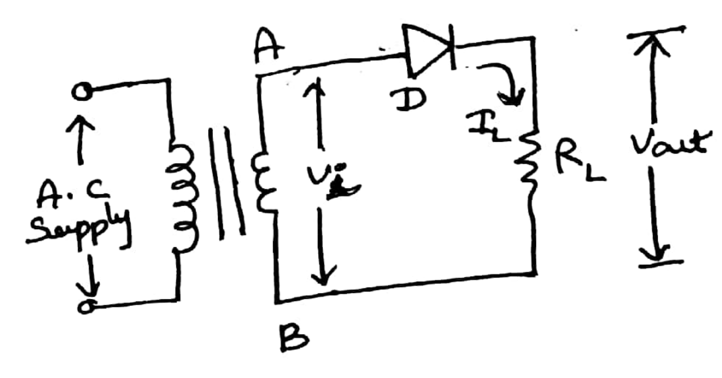
R.B → -ive half-cycles

Hence if a single diode is used for rectification, conduction occurs only during +ive half-cycles. This is half-wave rectification

If we are using two or four diodes, conduction occurs during both positive & negative half-cycles. This is full-wave rectification

Half-wave rectification:-

A diode D and load resistor R_L are connected in series, and the alternating voltage to be rectified is applied directly across the series combination, if no transformer used.



However, if a transformer is used, let it be assumed that end A of the secondary winding is +ive during a positive half-cycle of V_s, the diode D is F.B & hence it conducts.

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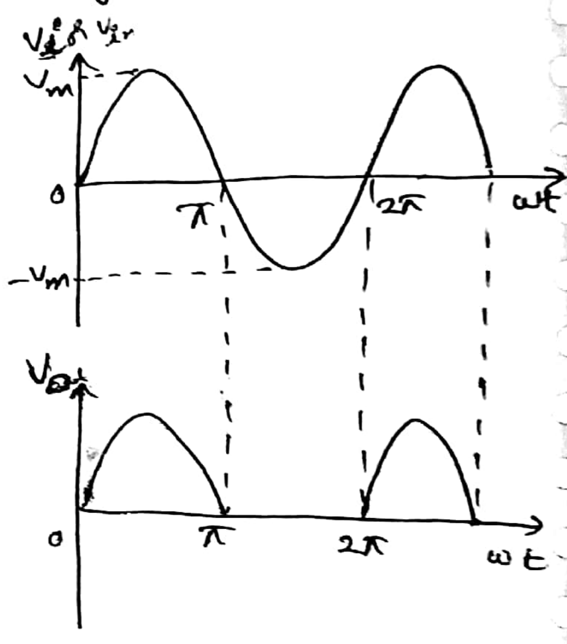
A current flows through the load resistor R_L.

- During the -ve half cycle of V_s, end A becomes negative. (end B would be positive then) and the diode gets reverse biased. It does not conduct and hence there is no output current through R_L.
- The diode conducts again during the subsequent +ve half cycle and there is flow of current through R_L.



- It is seen that there is conduction only during +ve half cycles of the applied signal. The o/p voltage i.e, the voltage which develops across R_L.

  all the negative half cycles of the i/p v/g are suppressed.

- The rectified o/p. i.e, current I_L is unidirectional, but it is not pure d.c., nor is it continuous. It is termed as pulsating d.c.

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$V_i = V_m \sin \omega t$

$V_m \rightarrow$ peak value

$$V_o = \begin{cases} V_m \sin \omega t & \text{for } 0 \le \omega t \le \pi \\ 0 & \text{for } \pi \le \omega t \le 2\pi \end{cases}$$

where $V_m = I_m R_L$

(1) dc voltage & Current:-

$$V_{avg} \text{ (or) } V_{dc} = \frac{\text{Area under the curve}}{\text{base}}$$

$$= \frac{\int_0^{2\pi} V_o \, d(\omega t)}{2\pi}$$

$$= \frac{1}{2\pi} \int_0^{2\pi} V_o \, d(\omega t)$$

$$= \frac{1}{2\pi} \int_0^{\pi} V_m \sin \omega t \, d\omega t \quad (\because V_o = 0 \text{ for } \pi \text{ to } 2\pi)$$

$$= \frac{V_m}{2\pi} \left[-\cos \omega t \right]_0^{\pi}$$

$$= \frac{V_m}{2\pi} \left[-\cos \pi + \cos 0 \right]$$

$\cos \pi = -1$

$\cos 0 = 1$

$$= \frac{V_m}{2\pi} [1 + 1] = \frac{V_m}{\pi}$$

$$\therefore \boxed{V_{dc} = \frac{V_m}{\pi}}$$

$$I_{dc} = \frac{V_{dc}}{R_L}$$

$$= \frac{V_m}{\pi R_L} = \frac{I_m R_L}{\pi R_L} \quad (\because V_m = I_m R_L)$$

$$\boxed{I_{dc} = \frac{I_m}{\pi}}$$

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(2) r.m.s Value of o/p voltage & Current:-

$$V_{r.m.s} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} V_0^2 \, d\omega t}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{2\pi} V_m^2 \sin^2 \omega t \, d\omega t} \quad \left(\because \sin^2\theta = \frac{1-\cos 2\theta}{2}\right)$$

$\therefore \int \cos 2x = \frac{\sin 2x}{2}$

$$= \sqrt{\frac{V_m^2}{2\pi}\int_0^{\pi} \frac{[1-\cos 2\omega t]}{2} \, d\omega t}$$

$$\int_0^{\pi/2} (1-\cos 2x)\,dx$$

$$\left[x - \frac{\sin 2x}{2}\right]_0^{\pi/2}$$

$$= \sqrt{\frac{V_m^2}{4\pi}\left[(\omega t)_0^{\pi} - \left[\frac{\sin 2\omega t}{2}\right]_0^{\pi}\right]}$$

$\int \cos\theta = \frac{\sin\theta}{2}$

$$= \sqrt{\frac{V_m^2}{4\pi}\left[(\pi - 0) - \left[\frac{\sin 2\pi}{2} - \frac{0}{2}\right]\right]} \quad (\because \sin 2\pi = 0)$$

$$= \sqrt{\frac{V_m^2}{4\pi}\cdot \pi} = \frac{V_m}{2}$$

$$\boxed{V_{r.m.s} = \frac{V_m}{2}}$$

$$I_{rms} = \frac{V_{rms}}{R_L} = \frac{V_m}{2R_L} = \frac{I_m R_L}{2R_L} = \frac{I_m}{2}$$

$$\therefore \boxed{I_{rms} = \frac{I_m}{2}}$$

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(3) **Rectifier efficiency:-**

The Rectifier efficiency is defined as the ratio of d.c output power to the a.c input power.

$$\eta = \frac{\text{d.c Power delivered to the load}}{\text{a.c input power from transfrmr}}$$

$$= \frac{P_{dc}}{P_{ac}} = \frac{V_{dc}\, I_{dc}}{V_{rms}\, I_{rms}}$$

$$= \frac{V_{dc} \cdot \frac{V_{dc}}{R_L}}{V_{rms} \cdot \frac{V_{rms}}{R_L}}$$

$$= \frac{V^2_{dc}}{V^2_{r.m.s}} = \frac{V_m^2/\pi^2}{V_m^2/2^2} = \frac{4}{\pi^2} = 0.406$$

$$= 40.6\%$$

(4) **Ripple factor (γ):-** The ratio of rms value of ac Component to the dc Component in the output is known as ripple factor.

$$\gamma = \frac{\text{rms value of ac Component}}{\text{dc value of Component}}$$

$V_r = V_{ac}$

$V_r \rightarrow$ ripple voltage

$$\gamma = \frac{(V_r)_{rms}}{V_{dc}} \qquad \frac{(V_{ac})_{rms}}{V_{dc}}$$

ac $\rightarrow$ ripple

where $(V_r)_{rms} = \sqrt{V^2_{rms} - V^2_{dc}}$

$$\gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

$$= \sqrt{\frac{V_m^2/4}{V_m^2/\pi^2} - 1}$$

$$= \sqrt{\frac{\pi^2}{4} - 1} = 1.21 \text{ for H.W.R}$$

$\boxed{\gamma = 1.21}$ for H.W.R

(5) **Regulation**:- The regulation is defined as the variation of d.c output voltage with change in d.c load current.

voltage regulation / load regulation

$$\% \text{ Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%.$$

(6) **Transformer utilisation factor**:- The d.c. Power to be delivered to the load in a rectifier circuit decides the rating of the transformer used in the circuit. So,

$$TUF = \frac{\text{d.c Power to be delivered to the load}}{\text{a.c rating of the transformer secondary}}$$

$$= \frac{P_{d.c}}{P_{a.c}(\text{rated})}$$

In the half-wave rectifying circuit, the rated voltage of the transformer secondary is $V_m/\sqrt{2}$, & the actual r.m.s current flowing through it according to the principle will be $\frac{I_m}{2}$

$$\therefore TUF = \frac{V_{dc} \cdot I_{dc}}{V_{ac}(\text{rated}) \cdot I_{ac}(\text{rated})}$$

$$= \frac{V_m/\pi \cdot I_m/\pi}{V_m/\sqrt{2} \cdot I_m/2} = \frac{2\sqrt{2}}{\pi^2} = 0.287$$

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This means that if the transformer rating is 1KVA (1000VA) then the half wave rectifier can deliver 1000 × 0.287 = 287 watts to load resistance.

(7) **Peak Inverse Voltage (PIV):-**

It is defined as the maximum voltage across the diode in the reverse direction without destroying the junction, i.e, V_m. Peak of a negative half cycle is V_m

(8) **Form Factor (F):-** The form factor F is defined as

$$F = \frac{\text{rms value}}{\text{average value}} = \frac{V_m/2}{V_m/\pi} = \frac{\pi}{2} = 1.57$$

(9) **Peak factor:-** It is defined as the ratio of peak value to r.m.s value

$$\therefore \text{Peak factor} = \frac{\text{Peak value}}{\text{rms value}} = \frac{V_m}{V_m/2} = 2$$

Problems:-

(1) A half-wave rectifier, having a resistive load of 1000 Ω. rectifies an alternating voltage of 325 V peak value and the diode has a forward resistance of 100 Ω. Calculate (a) peak, average and rms value of current (b) dc power output (c) ac input power (d) efficiency of the rectifier.

Sol:- (a) Peak value of current, $I_m = \frac{V_m}{r_f + R_L} = \frac{325}{100+1000} = 295.45$ mA

Average Current, $I_{dc} = \frac{I_m}{\pi} = \frac{295.45}{3.14} = 94.046 \text{ mA}$

RMS value of Current, $I_{rms} = \frac{I_m}{2} = \frac{295.45}{2} = 147.725 \text{ mA}$

(b) DC power output, $P_{dc} = I_{dc}^2 \times R_L$

$= (94.046 \times 10^{-3})^2 \times 1000$

$= 8.845 W$

(c) AC input power, $P_{ac} = (I_{rms})^2 \times (r_f + R_L)$

$= (147.725 \times 10^{-3})^2 \times (1100) = 24 W$

(d) Efficiency of rectification, $\eta = \frac{P_{dc}}{P_{ac}} = \frac{8.845}{24} = 36.85\%$

(2) A HWR has a load of 3.5 KΩ. If the diode resistance and Secondary Coil resistance together have a resistance of 800 Ω and the input voltage has a Signal voltage of peak value 240V. Calculate

(i) Peak, average and rms value of Current flowing.

(ii) dc power output

(iii) ac power input

(iv) efficiency of the rectifier.

Sol:- Load resistance in a HWR, $R_L = 3.5 K\Omega$

Diode and Secondary Coil resistance, $r_f + r_s = 800 \Omega$

peak value of input voltage $= 240V$

(i) Peak value of Current, $I_m = \frac{V_m}{r_s + r_f + R_L} = \frac{240}{4300} = 55.81 mA$

Average value of Current, $I_{dc} = \frac{I_m}{\pi} = \frac{55.81 \times 10^{-3}}{\pi} = 17.77 mA$

RMS value of Current, $I_{rms} = \frac{I_m}{2} = \frac{55.81 \times 10^{-3}}{2} = 27.905 mA$

(ii) DC power output is

$$P_{dc} = (I_{dc})^2 R_L = (17.77 \times 10^{-3})^2 \times 3500 = 1.105W$$

(iii) AC power input is

$$P_{ac} = (I_{rms})^2 \times (r_f + R_L + r_s) = (27.905 \times 10^{-3})^2 \times 4300 = 3.348W$$

~~$= (0.15)^2 \times 896 \Omega = 18 W$~~

(iv) Efficiency of the rectifier is

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{1.105}{3.348} \times 100 = 33\%$$

(3) A half-wave rectifier is used to supply 24 vdc to a resistive load of 500 Ω & the diode has a forward resistance of 50 Ω. Calculate the maximum value of the ac voltage required at the input.

Ans: Average value of load Current, $I_{dc} = \frac{V_{dc}}{R_L} = \frac{24}{500} = 48 mA$

Maximum value of load Current, $I_m = \pi \times I_{dc} = \pi \times 48 mA = 150.8 mA$

∴ maximum ac voltage required at the input,

$$V_m = I_m \times (r_f + R_L)$$
$$= 150.8 \times 10^{-3} \times 550$$
$$= 82.94V$$

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(4) An ac supply of 230V is applied to a half-wave rectifier circuit through transformer of turns ratio $n_2 : n_1$ 5:1. Assume the diode is an ideal one. The load resistance is 300 Ω. Find (a) dc output voltage (b) PIV (c) maximum and (d) average values of Power delivered to the load.

Ans:- (a) The transformer secondary voltage $= \frac{230}{5} = 46\,V$

Rated voltage of the transformer secondary is $\frac{V_m}{\sqrt{2}}$

Maximum value of secondary voltage, $V_m = \sqrt{2} \times 46 = 65V$

$\therefore$ dc o/p voltage, $V_{dc} = \frac{V_m}{\pi} = \frac{65}{\pi} = 20.7\,V$

(b) PIV of a diode $= V_m = 65V$

(c) Maximum value of load current, $I_m = \frac{V_m}{R_L} = \frac{65}{300}$

$= 0.217A$

$\therefore$ max value of Power delivered to the load,

$\rightarrow P_m = I_m^2 \times R_L = (0.217)^2 \times 300 = 14.1W$

(d) The average value of load current, $I_{dc} = \frac{V_{dc}}{R_L} = \frac{20.7}{300}$

$= 0.069\,A$

$\therefore$ avg value of Power delivered to the load

$\rightarrow P_{dc} = I_{dc}^2 \times R_L = (0.069)^2 \times 300 = 1.43W.$

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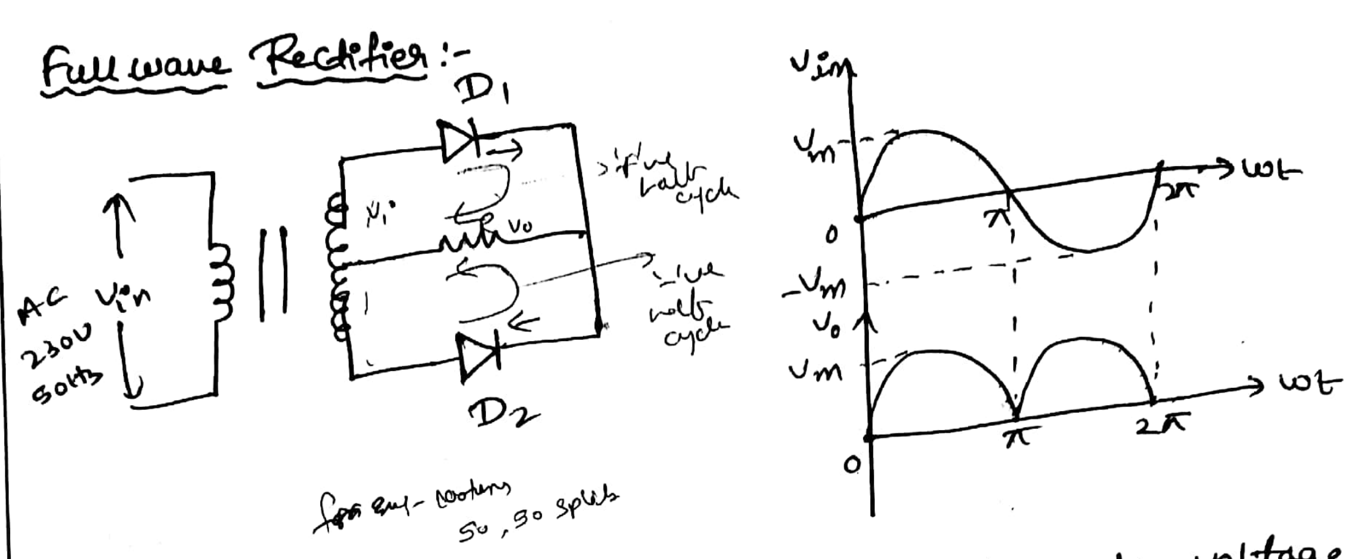
Full wave Rectifier :-



- It Converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. It uses two diodes of which are conducts during one half-cycle while the other diode conducts during the other half-cycle of the applied ac voltage.

- During positive half cycle ⇒ D_1 becomes positive & (F.B)
  D_2 becomes negative (R.B)

  ⇒ D_1 Conducts
  D_2 does not Conduct

The load current flows through D_1 and the voltage drop across R_L will be equal to the input voltage.

- During negative half cycle of the input ⇒ D_1 becomes negative (R.B)
  ⇒ D_2 becomes F.B
  D_1 does not Conduct
  D_2 Conducts

The load current flows through D_2 and the voltage drop across R_L will be equal to the input voltage.

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$$V_o = \begin{cases} V_m \sin\omega t & 0 \le \omega t \le \pi \\ V_m \sin\omega t & \pi \le \omega t \le 2\pi \end{cases}$$ where $V_m = I_m R_L$

(Sketch: V_o against ωt, with humps between 0, π, 2π, 3π; the first hump is shaded.)

(1) dc Voltage & Current

$$V_{avg} \text{ (or) } V_{dc} = \frac{\text{Area under the curve over full cycle}}{\text{period of the cycle}}$$

period $= \pi - 0 = \pi$

$$= \frac{\int_0^\pi V_o \, d(\omega t)}{\pi}$$

$$= \frac{1}{\pi}\int_0^\pi V_m \sin\omega t \, d\omega t$$

$$= \frac{V_m}{\pi}\left[-\cos\omega t\right]_0^\pi = \frac{V_m}{\pi}\left[-\cos\pi + \cos 0\right]$$

$$= \frac{V_m}{\pi}\left[-(-1)+1\right] = \frac{2V_m}{\pi}$$

$$\boxed{V_{dc} = \frac{2V_m}{\pi}}$$

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{2V_m}{\pi R_L} = \frac{2 I_m R_L}{\pi R_L}$$

$$\boxed{I_{dc} = \frac{2I_m}{\pi}}$$

(2) r.m.s value of o/p voltage & Current

$$V_{r.m.s} = \sqrt{\frac{\int_0^\pi V_o^2 \, d(\omega t)}{\pi}}$$

$$= \sqrt{\frac{1}{\pi}\int_0^\pi V_m^2 \sin^2\omega t \, d(\omega t)}$$

$$= \sqrt{\frac{V_m^2}{\pi}\int_0^\pi \left(\frac{1-\cos 2\omega t}{2}\right) d\omega t}$$

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$$= \sqrt{\frac{V_m^2}{2\pi}\left[(\omega t)_0^\pi - \left(\frac{\sin 2\omega t}{2}\right)_0^\pi\right]}$$

$$= \sqrt{\frac{V_m^2}{2\pi}\left[(\pi - 0) - \left[\frac{\sin 2\pi}{2} - \frac{\sin 2(0)}{2}\right]\right]}$$

$$= \sqrt{\frac{V_m^2}{2\pi}\left[\pi - 0 - 0\right]}$$

$$= \sqrt{\frac{V_m^2}{2\pi}\cdot\pi} = \sqrt{\frac{V_m^2}{2}} = \frac{V_m}{\sqrt{2}}$$

$$\boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}$$

$$I_{rms} = \frac{V_{rms}}{R_L} = \frac{V_m}{\sqrt{2}R_L} = \frac{I_m R_L}{\sqrt{2}R_L}$$

$$\boxed{I_{rms} = \frac{I_m}{\sqrt{2}}}$$

(3) Rectifier efficiency:-

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{V_{dc}\cdot I_{dc}}{V_{rms}\cdot I_{rms}} = \frac{V_{dc}\cdot\frac{V_{dc}}{R_L}}{V_{rms}\cdot\frac{V_{rms}}{R_L}}$$

$$= \frac{V_{dc}^2}{R_L}\cdot\frac{R_L}{V_{rms}^2} = \frac{V_{dc}^2}{V_{rms}^2} = \frac{\left(\frac{2V_m}{\pi}\right)^2}{\left(\frac{V_m}{\sqrt{2}}\right)^2}$$

$$= \frac{4V_m^2}{\pi^2}\times\frac{2}{V_m^2} = \frac{8}{\pi^2} = 0.812$$

$$\boxed{\eta_{FWR} = 81.2\%}$$

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(4) **Ripple Factor:-**

$$\gamma = \frac{(V_r)_{rms}}{V_{dc}}$$

$$(V_r)_{rms} = \sqrt{V_{rms}^2 - V_{dc}^2}$$

$$\gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{V_m^2}{(\sqrt{2})^2} \cdot \frac{\pi^2}{4V_m^2}\right) - 1}$$

$$= \sqrt{\frac{\pi^2}{8} - 1} = 0.482$$

$$\boxed{\gamma = 0.482} \text{ for F.W.R}$$

(5) **Regulation:-**

$$\text{Load regulation\%} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%$$

$$\text{Line regulation\%} = \frac{V_{FL} - V_{NL}}{V_{NL}} \times 100\%$$

(6) **Transformer utilisation factor**

$$TUF = \frac{P_{d.c}}{P_{a.c(rated)}} = \frac{V_{dc}\, I_{dc}}{V_{ac(rated)} \cdot I_{ac(rated)}}$$

at secondary winding

$$= \frac{\frac{2V_m}{\pi} \cdot \frac{2I_m}{\pi}}{\frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{\sqrt{2}}} = \frac{\sqrt{2}\sqrt{2} \times 4}{\pi^2}$$

$$= \frac{8}{\pi^2} = 0.812 = 81.2\%$$

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As we know, a full wave rectifier, Consists of two half-wave rectifiers.

~~∴ TUF of primary winding = 2 × TUF of HWR~~

~~= 2 × 0.287~~

~~Primary TUF = 0.574~~

~~The average TUF = (TUF (Primary) + TUF (Secondary)) / 2~~

$$avg\ TUF = \frac{TUF_{(P)} + TUF_{(S_1)} + TUF_{(S_2)}}{3}$$

~~$= \frac{0.574 + 0.812}{2}$~~

$$= \frac{0.812 + (0.287 + 0.287)}{2}$$

$= 0.693$

TUF $= 0.693 = 69.3\%$

TUF = 69.3% for F.W.R

(7) **Peak Inverse voltage (PIV) :-**

PIV for FWR $= 2V_m$

(8) **Form Factor :-**

$$F = \frac{rms\ Value}{avg\ Value} = \frac{\frac{V_m}{\sqrt{2}}}{\frac{2V_m}{\pi}} = \frac{V_m}{\sqrt{2}} \cdot \frac{\pi}{2V_m} = \frac{\pi}{2\sqrt{2}} = 1.11$$

$F = 1.11$

(9) **Peak Factor :-**

$$= \frac{Peak\ value}{rms\ Value} = \frac{V_m}{V_m/\sqrt{2}}$$

$= \sqrt{2}$

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Transformer transforms (changes) high v/g to low v/g or low v/g to high v/g

Step down transformer (Voltage has been stepped -down)

(1) n_1 n_2 5:1

230V — 46V

$n_1 > n_2$ → step down

1:5 ratio = $n_2 > n_1$ → step up for same example

$$\frac{\text{Primary turns}}{\text{Secondary turns}} = \frac{\text{Primary Voltage}}{\text{Secondary Voltage}}$$

$$\frac{5}{1} = \frac{230V}{Sec. v/g}$$

$$sec. v/g = \frac{230}{5} = 46 V$$

(2) Primary voltage = 220

Secondary " = 110

Ratio is 2:1

$$\frac{\text{Primary turns}}{1} = \frac{220}{110} = 2$$

(3) 19:1

230 — 12

$$\frac{\text{Pri turns}}{1} = \frac{230}{12}$$

(4) $\frac{480}{120} = 4:1$

(5) $\frac{240}{120} = 2:1$

(6) $\frac{300}{180} = 2:1$

(7) N_p : N_s

355 : 4500
n_1 n_2

Primary v/g = 35 (V_p)

$$\frac{N_p}{N_s} = \frac{V_p}{V_s}$$

$$\frac{355}{4500} = \frac{35}{V_s}$$

$$V_s = \frac{35 \times 4500}{355}$$

$$= 443.66$$

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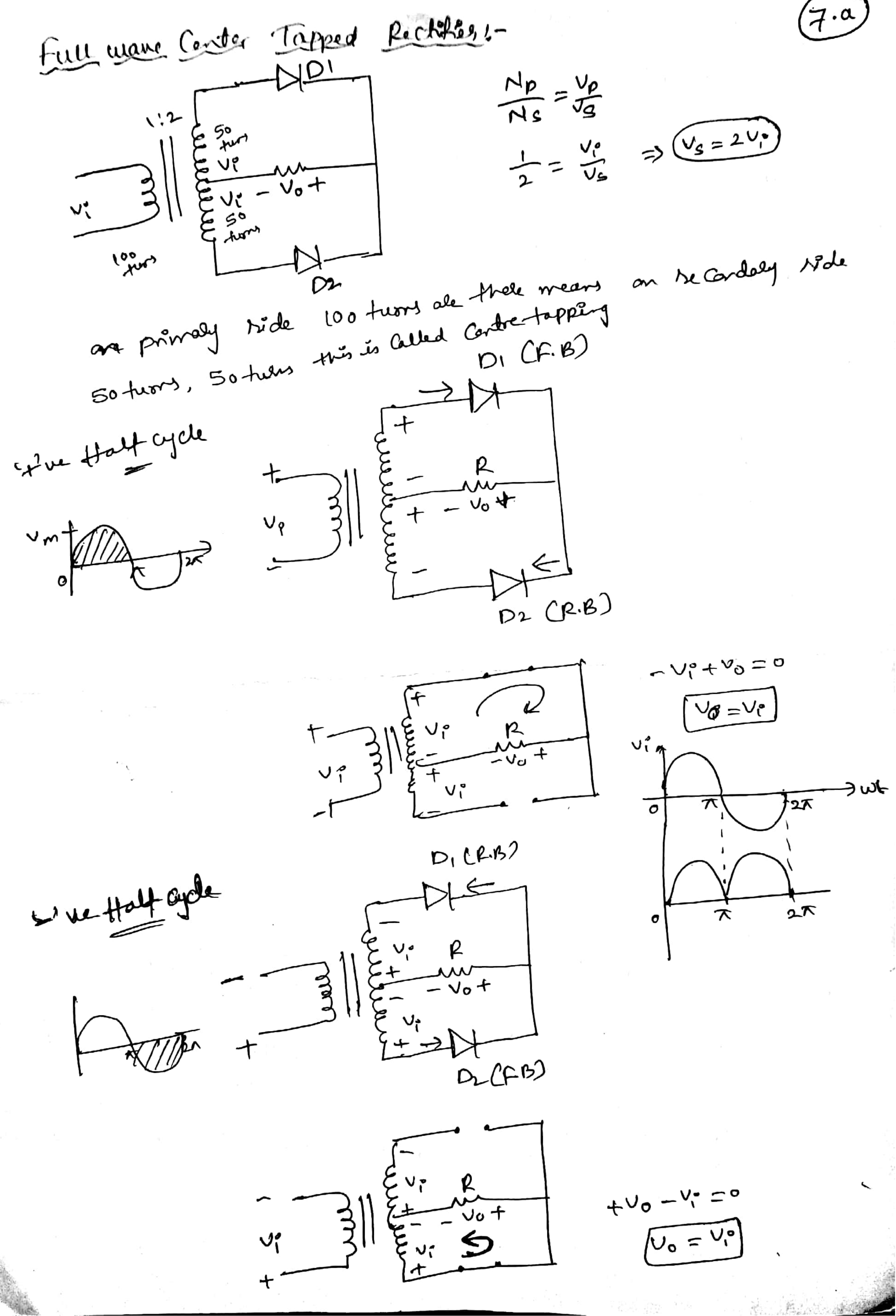
Comparision of Rectifiers

	Half-wave	Full-wave	Bridge
No. of diodes	1	2	4
η (efficiency)	40.6%	81.2%	81.2%
V_{dc}	V_m/π	$2V_m/\pi$	$2V_m/\pi$
V_{rms}	$V_m/2$	$V_m/\sqrt{2}$	$V_m/\sqrt{2}$
Ripple factor (γ)	1.21	0.48	0.48
PIV	V_m	$2V_m$	V_m
Form Factor	1.57	1.11	1.11
Peak Factor	2	$\sqrt{2}$	$\sqrt{2}$
TUF	0.287	0.46	0.81

disadv of FWR :- usage of centre tapped transformer, costly, bulky, $2V_m$



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Advantages of Half wave Rectifier:-

- Simple Circuit
- Low Cost

Disadvantages of Half wave Rectifier:-

- Low rectifier efficiency
- Higher ripple factor
- Low TUF

Advantages of Full wave Rectifier:-

- Equal currents flow through the two halves of the Centre tapped Secondary of the power transformer in opposite directions. Hence dc saturation of the core is avoided.
- Higher ripple frequency & Lower ripple factor permits use of cheaper Smoothing filter.
- Higher o/p voltage, higher o/p power & higher TUF.
- Higher rectifier efficiency.

Drawbacks of Full wave Rectifier:-

- More circuit elements
- Higher Cost.

Merits of Bridge Rectifier:-

- currents in both the Primary & the Secondary of the power transformer flow for the entire a.c. cycle & hence for a given power output, power transformer of a small size may be used in Comparision with that in a full wave Rectifier.
- No Centre tap is needed in the transformer secondary.
- Since two diodes are present in Series in each Conduction path, PIV rating of each diode is only Vm. Hence bridge Rectifier is highly Suited for high Voltage application.

Disadvantages of Bridge Rectifier

- Four diodes are needed
- Load resistor & the Source have no Common point which may be earthed.
- During each half cycle, two diodes are present in Series in each Conduction path, PIV rating of each diode is only Vm. Hence bridge Rectifier is highly Suited for high voltage applications.

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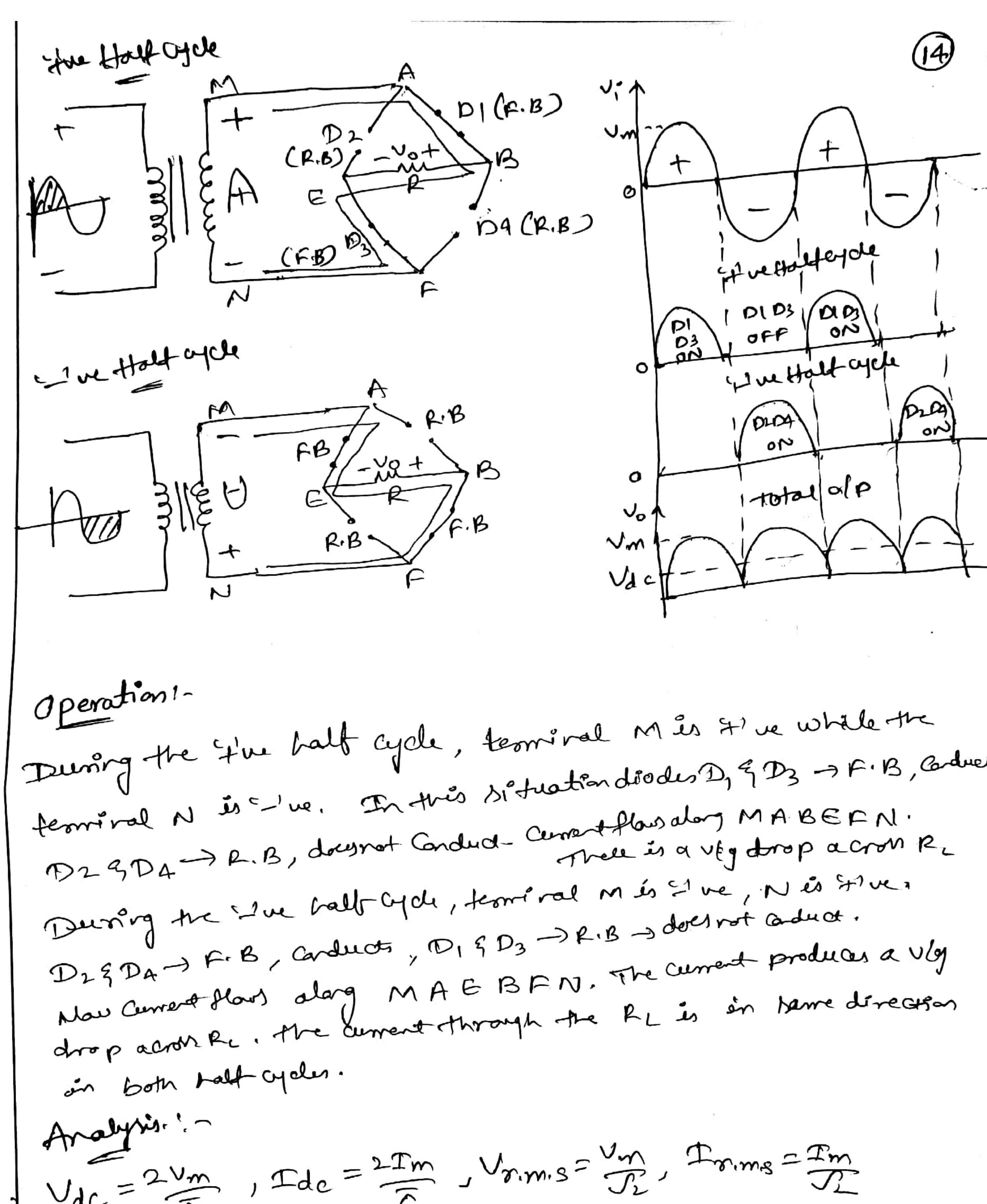

Operation:-

During the +ve half cycle, terminal M is +ve while the terminal N is -ve. In this situation diodes D_1 & D_3 → F.B, conducts. D_2 & D_4 → R.B, does not conduct. Current flows along MABEFN. There is a vtg drop across R_L.

During the -ve half cycle, terminal M is -ve, N is +ve. D_1 & D_3 → R.B → does not conduct. D_2 & D_4 → F.B, conducts. Now current flows along MAEBFN. The current produces a vtg drop across R_L. The current through the R_L is in same direction in both half cycles.

Analysis:-

→ $V_{dc} = \frac{2V_m}{\pi}$, $I_{dc} = \frac{2I_m}{\pi}$, $V_{r.m.s} = \frac{V_m}{\sqrt{2}}$, $I_{r.m.s} = \frac{I_m}{\sqrt{2}}$

→ $\eta = 0.812$ (or) 81.2%, $\gamma = 0.48$

→ $TUF = \frac{(TUF)_p + (TUF)_s}{2} = \frac{0.812 + 0.812}{2} = 0.812$

→ PIV:- It is V_m for each diode

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UNIT- III
TRANSISTOR CHARACTERISTICS

BJT: Junction transistor, transistor current components, transistor equation, transistor configurations, transistor as an amplifier, characteristics of transistor in Common Base, Common Emitter and Common Collector configurations, Ebers-Moll model of a transistor, punch through/ reach through, Photo transistor, typical transistor junction voltage values.**FET:** FET types, construction, operation, characteristics, parameters, MOSFET-types, construction, operation, characteristics, comparison between JFET and MOSFET.

Transistors

Unipolar Junction Transistor (UJT) ⇓ The current conduction is only due to one type of carriers ie majority carriers.

Bipolar Junction Transistor (BJT) ⇓ The current conduction in bipolar transistor is due to both minority and majority carriers.

Bipolar Junction Transistor (BJT)

Construction :

* It's a 3 terminal device → Emitter (E), Base (B) & collector (C)
* Two Basic types
  - npn ⇓ 2 layers of n-type material sandwitching a thin p-type layer is called npn Transistor
  - pnp ⇒ 2 layer of p-type material sandwitching a thin n-type layer is called pnp Transistor.
* The Emitter terminal is heavily doped while the base & collector are lightly doped.
* The Thickness of the base layer is ~0.001 of that of the emitter (or) collector layer.

Symbols :

B, C, E — npn ⇒ Emitter — n | p | n — collector; Base; 2 pn Junction

B, C, E — pnp ⇒ Emitter — p | n | p — collector; Base; 2 pn Junction

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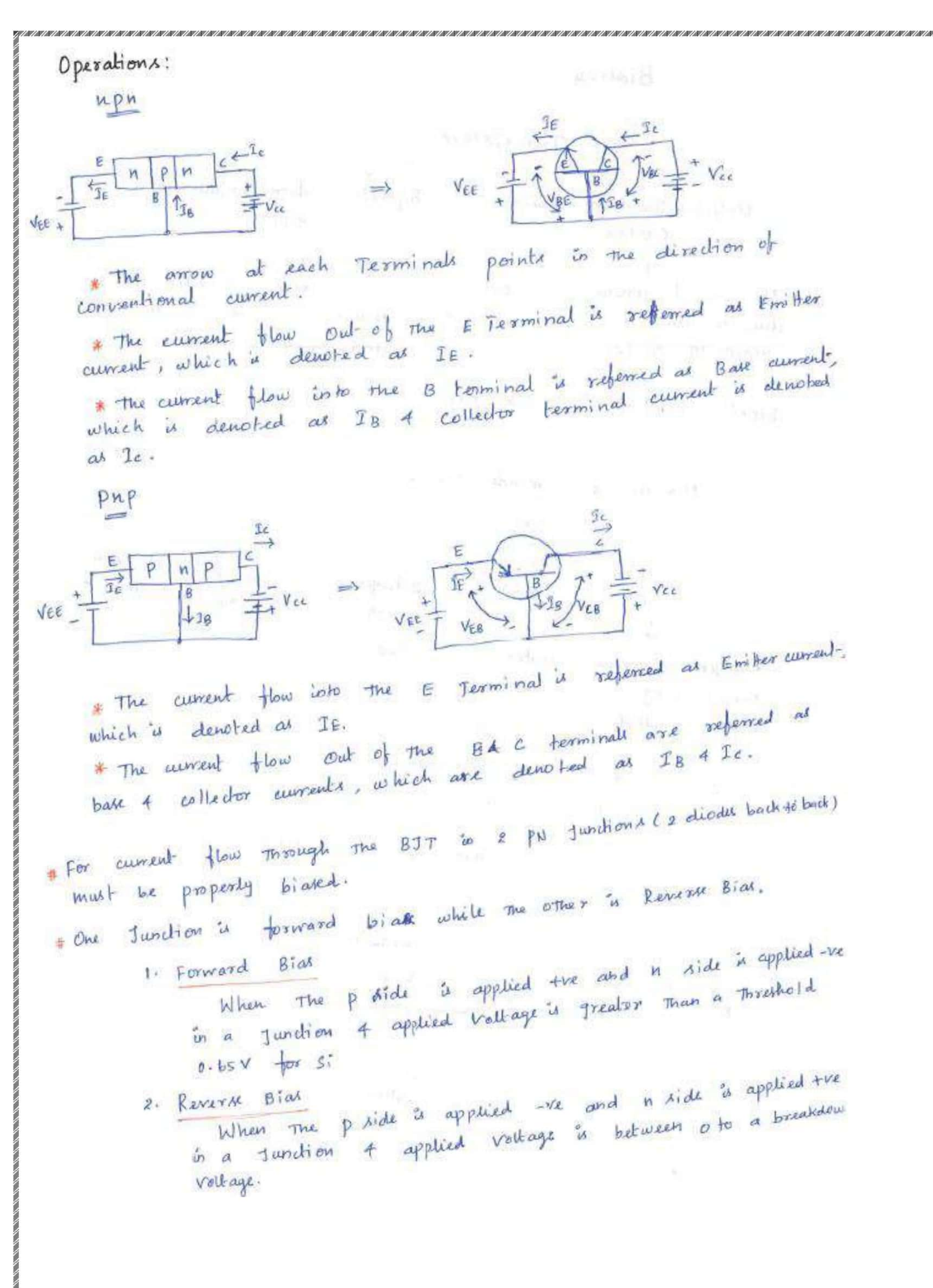

Operations:

npn

* The arrow at each Terminals points in the direction of conventional current.

* The current flow out of the E Terminal is referred as Emitter current, which is denoted as I_E.

* The current flow into the B terminal is referred as Base current, which is denoted as I_B & Collector terminal current is denoted as I_C.

pnp

* The current flow into the E Terminal is referenced as Emitter current, which is denoted as I_E.

* The current flow out of the B & C terminals are referred as base & collector currents, which are denoted as I_B & I_C.

* For current flow through the BJT is 2 PN Junctions (2 diodes back to back) must be properly biased.

* One Junction is forward bias while the other is Reverse Bias.

1. Forward Bias

   When the p side is applied +ve and n side is applied -ve in a Junction & applied voltage is greater than a Threshold 0.65 V for Si

2. Reverse Bias

   When the p side is applied -ve and n side is applied +ve in a Junction & applied voltage is between 0 to a breakdown voltage.

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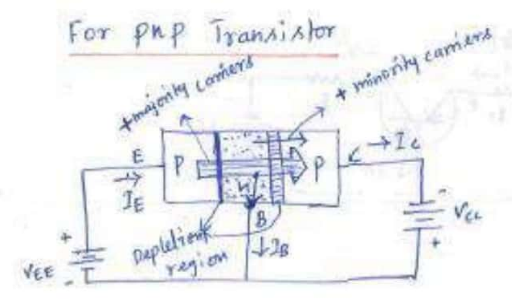
For pnp Transistor



* The Emitter - Base Junction is forward biased While the collector - Base Junction is Reverse biased.

* The majority carriers will flow from E to B across forward bias Junction.

* Because the Base layer is very thin & has a high resistance, most of these carriers will diffuse across the reverse bias junction into the collector in the same direction of the minority charges & only tiny amount of current will flow out of the Base Terminal.

* Typically collector currents are of the order of mA While Base currents are μA.

* Applying Kirchhoff's current law:

$$I_E = I_C + I_B$$

* The collector current is comprised of 2 components → majority & minority carriers.

* The minority current component is called leakage current, I_{CO} (I_C with Emitter terminal open).

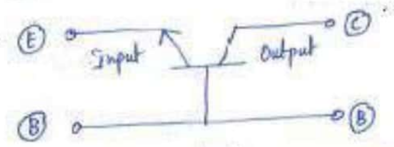
* So the collector current is

$$I_C = I_{C_{majority}} + I_{CO_{minority}}$$

Transistor Configurations:

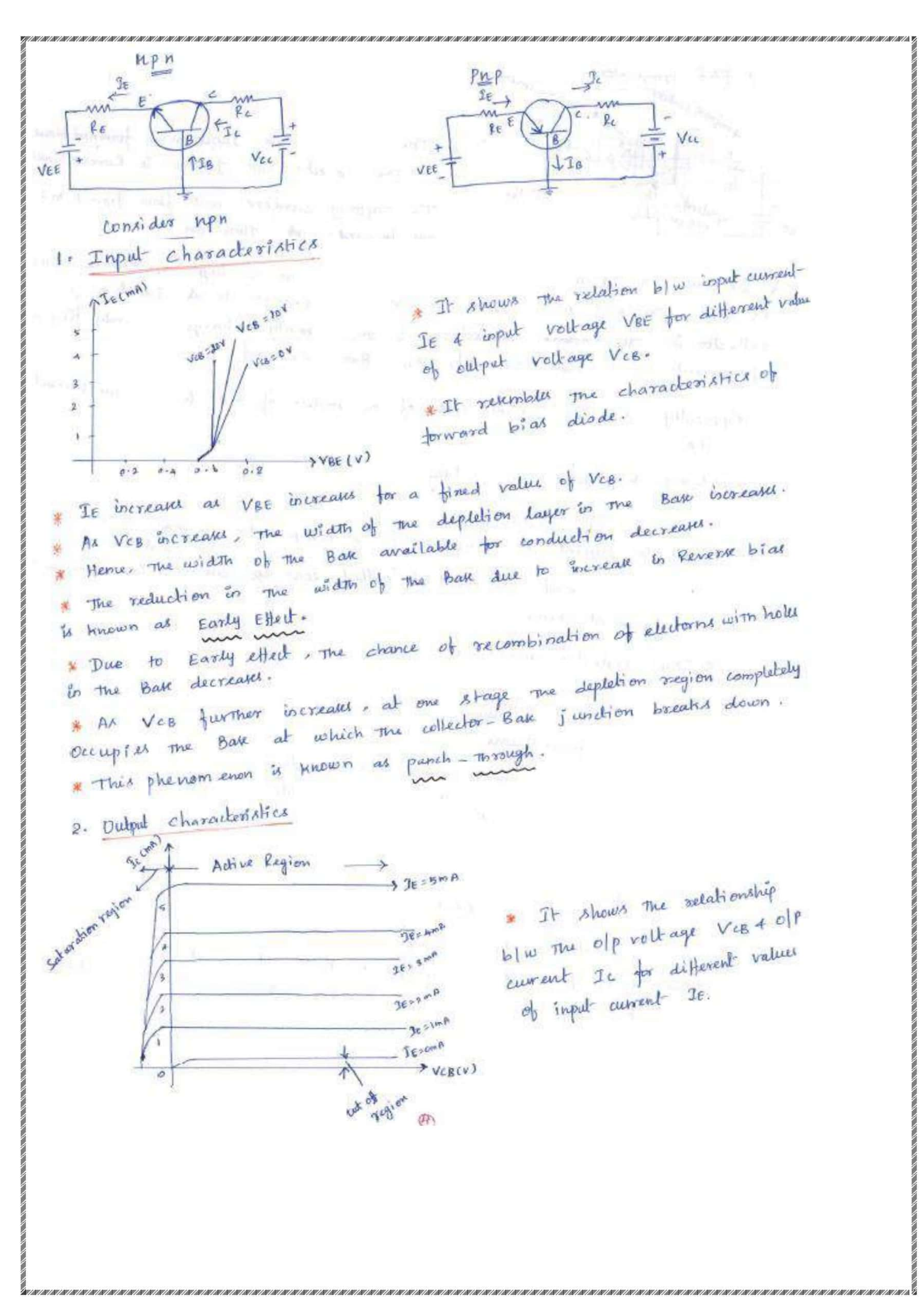
1. Common Base (CB) configuration
2. Common Emitter (CE) configuration
3. Common collector (CC) configuration

1. Common Base configuration



* The Base terminal is common to both i/p & o/p.

* The i/p is applied b/w the Emitter & the base & o/p is taken from collector & Base.



npn

I_E, E, C, R_E, R_C, I_C, B, I_B, V_{EE}, V_{CC}

pnp

I_E, I_C, R_E, E, C, R_C, B, I_B, V_{EE}, V_{CC}

Consider npn

1. Input characteristics

I_E(mA), $V_{CB}=10V$, $V_{CB}=20V$, $V_{CB}=0V$, V_{BE}(V), 0.2, 0.4, 0.6, 0.8

* It shows the relation b/w input current I_E & input voltage V_{BE} for different value of output voltage V_{CB}.
* It resembles the characteristics of forward bias diode.

* I_E increases as V_{BE} increases for a fixed value of V_{CB}.
* As V_{CB} increases, the width of the depletion layer in the Base increases.
* Hence, the width of the Base available for conduction decreases.
* The reduction in the width of the Base due to increase in Reverse bias is known as Early Effect.
* Due to Early effect, the chance of recombination of electrons with holes in the Base decreases.
* As V_{CB} further increases, at one stage the depletion region completely occupies the Base at which the collector-Base junction breaks down.
* This phenomenon is known as punch-through.

2. Output characteristics

I_C(mA), Active Region, Saturation region, $I_E=5mA$, $I_E=4mA$, $I_E=3mA$, $I_E=2mA$, $I_E=1mA$, $I_E=0mA$, V_{CB}(V), cut off region

* It shows the relationship b/w the o/p voltage V_{CB} & o/p current I_C for different values of input current I_E.

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i) Cut-off Region

* Both the junctions are reverse biased.
* When the emitter-base junction is reverse biased, the current due to majority carrier ie I_E is zero.
* When the collector-base junction is reverse biased, the current due to minority carriers flows from the collector to the base is represented as I_{CBO}.

ii) Active Region

* The Emitter-base junction is forward biased & the collector-base junct is reverse biased.
* Once the V_{CB} reaches a value large enough to ensure a large portion of electrons enter the collector, I_C remains constant as shown by horizontal lines.
* As I_E increases, I_C increases.

iii) Saturation Region

* Both junctions are forward biased.
* When V_{CB} is -ve, the collector-base junction is actually forward biase
* Thus, graphs are drawn on the -ve side of V_{CB}.

Current Amplification factor (α)

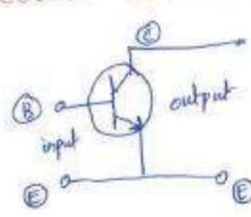
* It's the ratio of change in collector current to the change in Emitter current at constant collector-base voltage V_{CB}.

$$\alpha_{AC} = \frac{\Delta I_C}{\Delta I_E} \Big|_{V_{CB} = \text{constant}}$$

* If only DC values are considered

$$\alpha_{DC} = \frac{I_C}{I_E}$$

2. Common-Emitter Configuration



* Input is applied b/w base & Emitter and output is taken b/w collector & the emitter.

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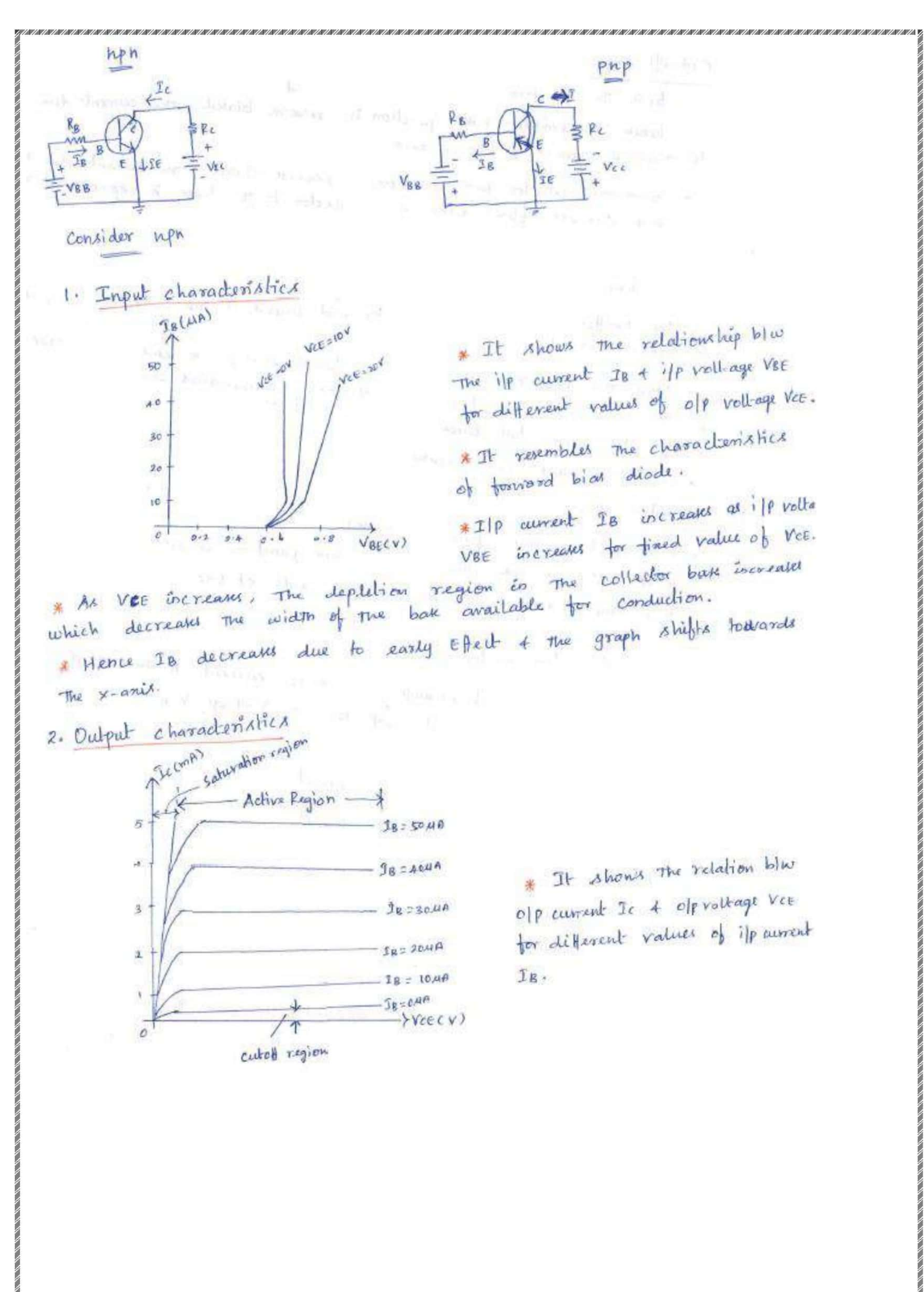

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i) Cut-off Region

* Both the junctions are reverse biased.
* When the emitter-base junction is reverse biased, the current due to majority carriers ie I_B is zero.
* When the collector-base junction is reverse biased. The current due to minority carriers flows from the collector to emitter which is represented as I_{CEO}.

ii) Active Region

* The Emitter-base junction is forward biased & the collector-base junction is reverse biased.
* As I_B is maintained constant, current I_C increases as reverse-bias voltage V_{CE} increases.

iii) Saturation Region

* Both junctions are forward biased.
* When V_{CE} is reduced to a small value such as 0.2 V, the collector base junction is actually forward biased.
* In this region, there is a large change in I_C with small change in V_{CE}

Current Amplification factor (β)

* It's defined as the change in collector current to the change in base current at constant collector-Emitter voltage V_{CE}.

$$\beta_{AC} = \frac{\Delta I_C}{\Delta I_B} \Bigg|_{V_{CE} = \text{constant}}$$

* If only DC values are considered

$$\beta_{DC} = \frac{I_C}{I_B}$$

Relation between α and β

$$I_E = I_C + I_B \quad \text{--- (1)}$$

Also,

$$\beta_{DC} = \frac{I_C}{I_B} \quad \text{--- (2)}$$

From (1) $\quad I_B = I_E - I_C \quad$ --- (3)

sub (3) in (2) $\quad \beta_{DC} = \dfrac{I_C}{I_E - I_C} \quad$ --- (4)

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* Divide eqn (4) by I_E both Numerator & Denominator

$$(4) \Rightarrow \beta_{DC} = \frac{I_C / I_E}{\frac{I_E}{I_E} - \frac{I_C}{I_E}} = \frac{I_C / I_E}{1 - \frac{I_C}{I_E}} \quad \text{— (5)}$$

W.K.T $\alpha_{DC} = \frac{I_C}{I_E}$

Sub α_{DC} in eqn (5)

$$(5) \Rightarrow \beta_{DC} = \frac{\alpha_{DC}}{1 - \alpha_{DC}}$$

* If subscript DC is ignored

$$\beta = \frac{\alpha}{1-\alpha}$$

Collector Current (I_C):

* Apply KCL to the transistor

$$I_E = I_B + I_C \quad \text{— (A)}$$

* The collector current has 2 components

$$I_C = I_{C\,majority} + I_{C\,minority}$$

$$I_C = \alpha I_E + I_{CO} \quad \text{— (B)}$$

* For general purpose Transistors → I_C is measured in mA & I_{CO} is measured in μA (or) nA.

sub eq (A) in (B)

$$I_C = \alpha(I_B + I_C) + I_{CO}$$

$$= \alpha I_B + \alpha I_C + I_{CO}$$

$$I_C - \alpha I_C = \alpha I_B + I_{CO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CO} \qquad \because \beta = \frac{\alpha}{1-\alpha}$$

$$= \beta I_B + \frac{1}{1-\alpha} I_{CO}$$

sub $\frac{1}{1-\alpha} = (\beta+1)$ so we get

$$I_C = \beta I_B + (\beta+1) I_{CO}$$

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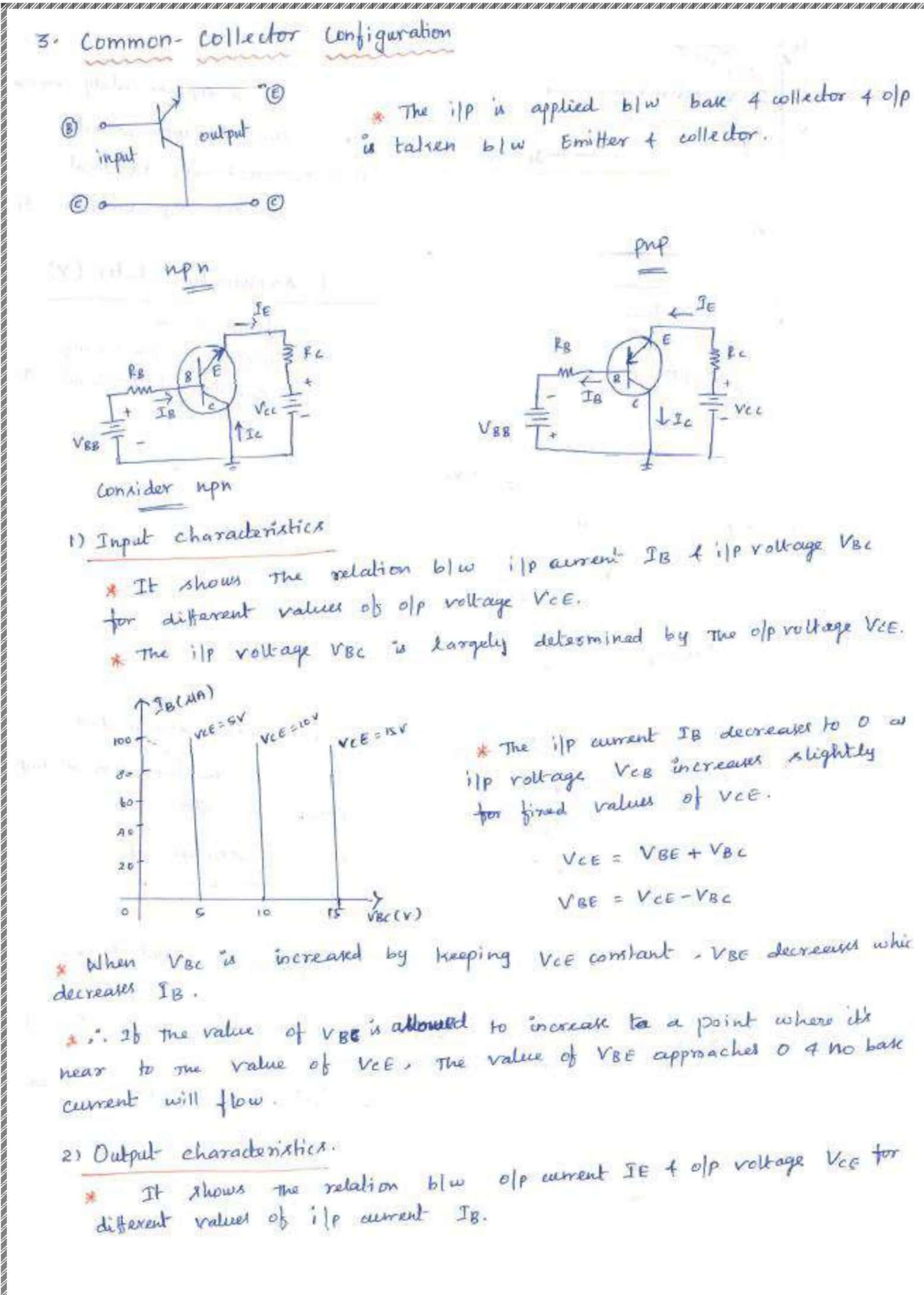

3. Common- Collector Configuration

* The i/p is applied b/w base & collector & o/p is taken b/w Emitter & collector.

Consider npn

1) Input characteristics

* It shows the relation b/w i/p current I_B & i/p voltage V_{BC} for different values of o/p voltage V_{CE}.

* The i/p voltage V_{BC} is largely determined by the o/p voltage V_{CE}.

* The i/p current I_B decreases to 0 as i/p voltage V_{CB} increases slightly for fixed values of V_{CE}.

$$V_{CE} = V_{BE} + V_{BC}$$

$$V_{BE} = V_{CE} - V_{BC}$$

* When V_{BC} is increased by keeping V_{CE} constant, V_{BE} decreases whic decreases I_B.

* ∴ If the value of V_{BE} is allowed to increase to a point where it's near to the value of V_{CE}, the value of V_{BE} approaches 0 & no base current will flow.

2) Output characteristics.

* It shows the relation b/w o/p current I_E & o/p voltage V_{CE} for different values of i/p current I_B.

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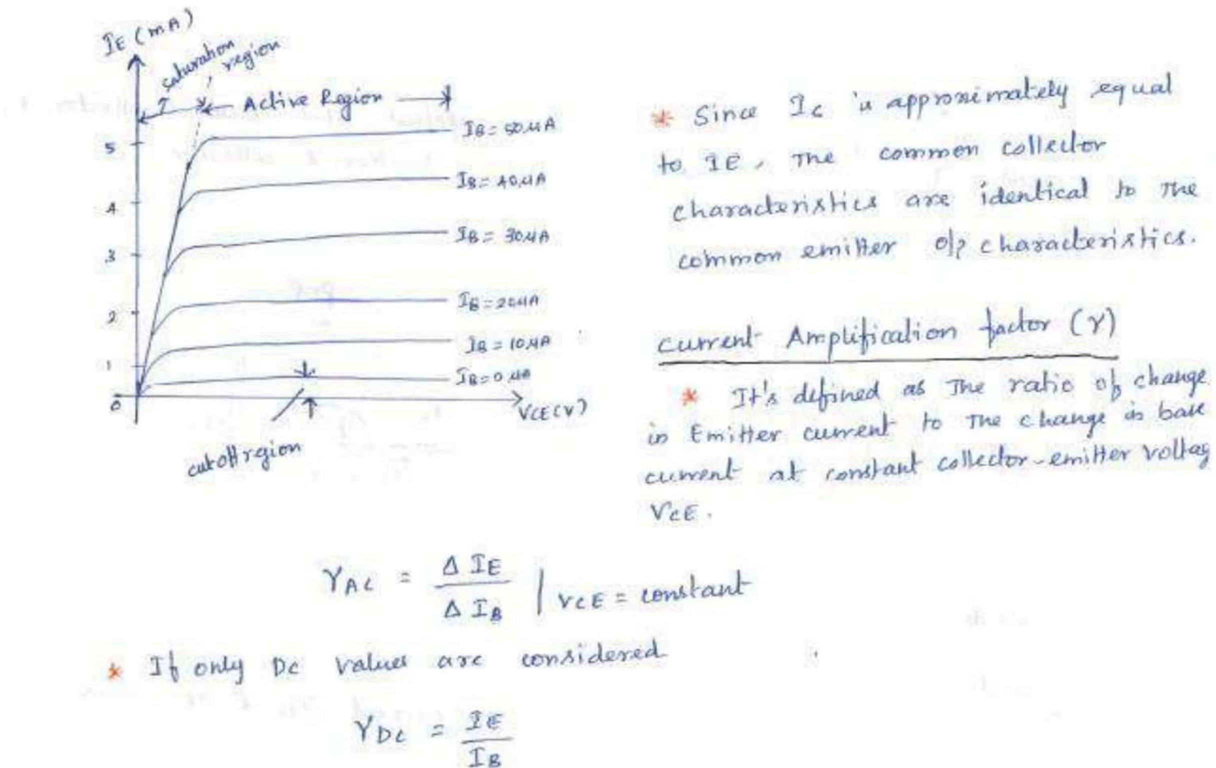

* Since I_C is approximately equal to I_E, the common collector characteristics are identical to the common emitter o/p characteristics.

Current Amplification factor (γ)

* It's defined as the ratio of change in Emitter current to the change in base current at constant collector-emitter voltage V_{CE}.

$$\gamma_{AC} = \frac{\Delta I_E}{\Delta I_B} \Big|_{V_{CE} = \text{constant}}$$

* If only DC values are considered

$$\gamma_{DC} = \frac{I_E}{I_B}$$

Current components in a transistor:

The figure below shows the various current components which flow across the forward-biased emitter junction and reverse-biased collector junction in P-N-P transistor.

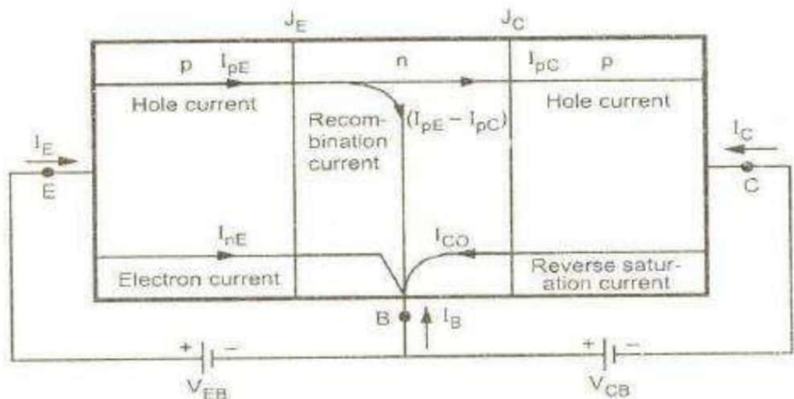

Figure. Current components in a transistor with forward-biased emitter and reverse-biased collector junctions.

The emitter current consists of the following two parts:

3. Hole current I_{pE} constituted by holes (holes crossing from emitter into base).
4. Electron current I_{nE} constituted by electrons (electrons crossing from base into the emitter).

Therefore, Total emitter current $I_E = I_{pE}$ (majority) + I_{nE} (Minority)

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The holes crossing the emitter base junction J_E and reaching the collector base junction J_C constitutes collector current I_{pC}.

Not all the holes crossing the emitter base junction J_E reach collector base junction J_C because some of them combine with the electrons in the n-type base.

Since base width is very small, most of the holes cross the collector base junction J_C and very few recombine, constituting the base current $(I_{pE} - I_{pC})$.

When the emitter is open-circuited, $I_E=0$, and hence $I_{pC}=0$. Under this condition, the base and collector together current I_C equals the reverse saturation current I_{CO}, which consists of the following two parts: I_{PCO} caused by holes moving across I_C from N-region to P-region.

I_{nCO} caused by electrons moving across I_C from P-region to N-region. $I_{CO} = I_{nCO} + I_{pCO}$

In general, $I_C = I_{nC} + I_{pC}$

Thus for a P-N-P transistor, $\mathbf{I_E = I_B + I_C}$

Ebers-

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FIELD EFFECT TRANSISTOR:

FET is a device in which the flow of current through the conducting region is controlled by an electric field. Hence the name Field Effect Transistor (FET). As current conduction is only by majority carriers, FET is said to be a unipolar device.

Based on the construction, the FET can be classified into two types as Junction FET (JFET) and Metal Oxide Semiconductor FET(MOSFET).

Depending upon the majority carriers, JFET has been classified into two types named as (1) N-channel JFET with electrons as the majority carriers and (2) P-channel JFET with holes as the majority carriers.

Construction of N-Channel JFET :

It consists of an N-type bar which is made of silicon. Ohmic contacts, (terminals) made at the two ends of the bar, are called Source and Drain.

Source (S) This terminal is connected to the negative pole of the battery. Electrons which are the majority carriers in the N-type bar enter the bar through this terminal.

Drain (D) This terminal is connected to the positive pole of the battery. The majority carriers leave the bar through this terminal.

Gate (G) Heavily doped P-type silicon is diffused on both sides of the N-type silicon bar by which PN junctions are formed. These layers are joined together and called Gate G.

Channel The region BC of the N-type bar in the depletion region is called the channel. Majority carriers move from the source to drain when a potential difference V_{DS} is applied between the source and drain.

Operation of N-channel JFET:

When $V_{GS} = 0$ and $V_{DS} = 0$ When no voltage is applied between drain and source, and gate and source, the thickness of the depletion regions around the PN junction is uniform as shown in figure.

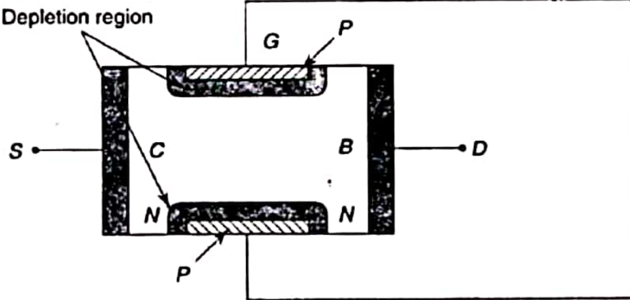

Figure 3.3: Construction of JFET

When $V_{DS} = 0$ and V_{GS} is decreased from zero. In this case PN junctions are reverse biased and hence the thickness of the depletion region increases. As V_{GS} is decreased from zero, the reverse bias voltage across the PN junction is increased and hence the thickness of the depletion region in the channel increases until the two depletion regions make contact with each other. In this condition, the channel is said to be cutoff. The value of V_{GS} which is required to cutoff the channel is called the cutoff voltage V_C.

When $V_{GS} = 0$ and V_{DS} is increased from zero. Drain is positive with respect to the source with $V_{GS} = 0$. Now the majority carriers (electrons) flow through the N-channel from source to drain. Therefore the

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conventional current I_D flows from drain to source. The magnitude of the current will depend upon the following factors:-

1. The number of the majority carriers (electrons) available in the channel, i.e. the conductivity of the channel.
2. The length *l* of the channel.
3. The cross sectional area *A* of the channel at *B*.
4. The magnitude of the applied voltage V_{DS}. Thus the channel acts as a resistor of resistance R given by

$$R = \frac{\rho l}{A} \quad ....(1)$$

$$I_D = \frac{V_{DS}}{R} = \frac{A\,V_{DS}}{\rho l} \quad ....(2)$$

where ρ is the resistivity of the channel. Because of the resistance of the channel and the applied voltage V_{DS}, there is a gradual increase of positive potential along the channel from source to drain. Thus the reverse voltage across the PN junctions increases and hence the thickness of the depletion regions also increases. Therefore the channel is wedge shaped, as shown in figure.

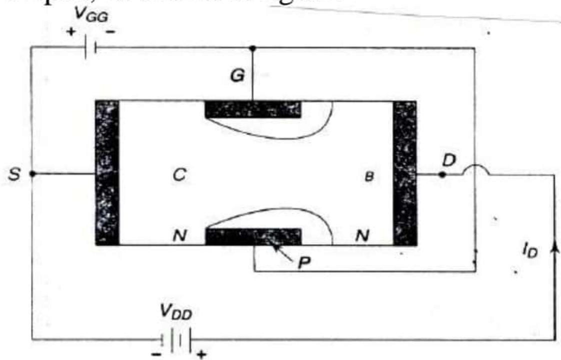

Figure 3.4: JFET under applied bias

As V_{DS} is increased, the cross-sectional area of the channel will be reduced. At a certain value V_P of V_{DS}, the cross-sectional area at B becomes minimum. At this voltage, the channel is said to be pinched off and the drain voltage V_P is called the pinch-off voltage.

As a result of the decreasing cross-section of the channel with the increase of V_{DS}, the following results are obtained.

(i) As V_{DS} is increased from zero, I_D increases along OP, and the rate of increase of I_D with V_{DS} decreases as shown in figure.

(ii) When $V_{DS} = V_P$, I_D becomes maximum. When V_{DS} is increased beyond V_P, the length of the pinch-off region increases. Hence there is no further increase of I_D.

(iii) At a certain voltage corresponding to the point B, I_D suddenly increases. This effect is due to the avalanche multiplication of electrons caused by breaking of covalent bonds of silicon atoms in the depletion region between the gate and the drain. The drain voltage at which the breakdown occurs is denoted by BV_{DGO}. The variation of I_D with V_{DS} when $V_{GS} = 0$ is shown in figure by the curve OPBC.

When V_{GS} is negative and V_{DS} is increased. When the gate is maintained at a negative voltage less than the negative cutoff voltage, the reverse voltage across the junction is further increased. Hence for a negative value of V_{GS}, the curve of I_D versus V_{DS} is similar to that for $V_{GS} = 0$, but the values of V_P and BV_{DGO} are lower, as shown in figure.

From the curves, it is seen that above the pinch-off voltage, at a constant value of V_{DS}. I_D increases with an increase of V_{GS}. Hence a JFET is suitable for use as a voltage amplifier, similar to a transistor amplifier.

It can be seen from the curve that for the voltage $V_{DS} = V_P$, the drain current is not reduced to zero. If the drain current is to be reduced to zero, the ohmic voltage drop along the channel should also be reduced to zero. Further, the reverse biasing to the gate-source PN junction essential for pinching off the channel would also be absent.

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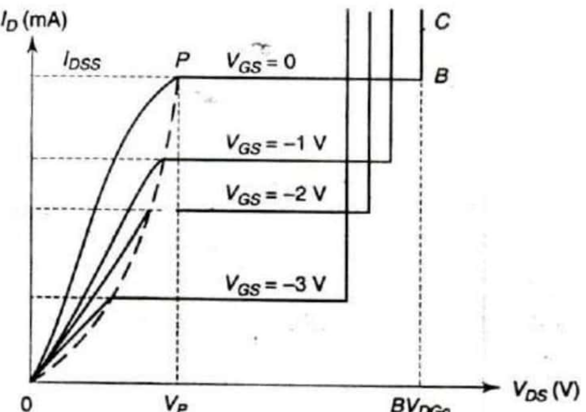

Figure 3.5: JFET Drain characteristics

The drain current I_D is controlled by the electric field that extends into the channel due to reverse biased voltage applied to the gate; hence this device has been given the name "Field Effect Transistor".

In a bar of P-type semiconductor, the gate is formed due to N-type semiconductor. The working of the P-channel JFET will be similar to that of the N-channel JFET with proper alterations in the biasing circuits; in this case holes will be the current carriers instead of electrons. The circuit symbols for N-channel and P-channel JFETs are shown in figure. It should be noted that the direction of the arrow points in the direction of conventional current which would flow into the gate if the PN junction was forward biased.

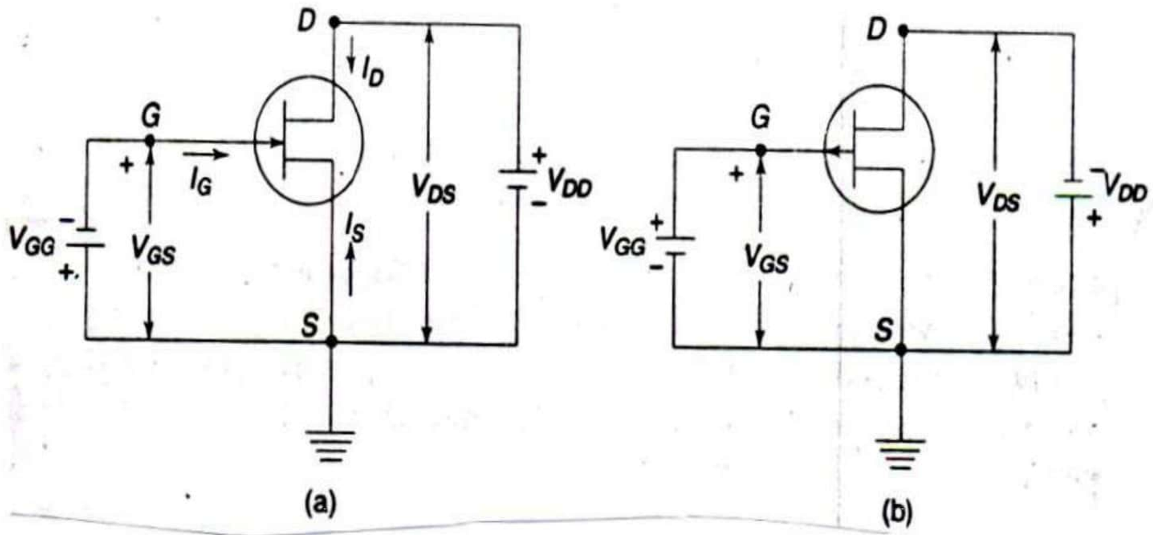

Figure 3.6: Circuit Symbols for N and P Channel JFET

MOSFET:

Metal Oxide Semiconductor Field Effect Transistor (MOSFET):

MOSFET is the common term for the Insulated Gate Field Effect Transistor (IGFET). There are two basic forms of MOSFET: (i) Enhancement MOSFET and (ii) Depletion MOSFET.

Principle:

By applying a transverse electric field across an insulator, deposited on the semiconducting material, the thickness and hence the resistance of a conducting channel of a semiconducting material can be controlled.

Enhancement MOSFET:

Construction: The construction of an N-channel Enhancement MOSFET is shown in figure. Two highly doped N^+ regions are diffused in a lightly doped substrate of P-type silicon substrate. One N^+ region is called the source S and the other one is called the drain D. They are separated by 1 mil (10^{-3} inch). A thin insulating layer of SiO_2 is grown over the surface of the structure and holes are cut into the oxide layers, allowing

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contact with source and drain. Then a thin layer of metal aluminum is formed over the layer of SiO_2. This metal layer covers the entire channel region and it forms the gate G.

The metal area of the gate, in conjunction with the insulating oxide layer of SiO_2 and the semiconductor channel forms a parallel plate capacitor. This device is called the insulated gate FET because of the insulating layer of SiO_2. This layer gives an extremely high input resistance for the MOSFET.

Operation: If the substrate is grounded and a positive voltage is applied at the gate, the positive charge on G induces an equal negative charge on the substrate side between the source and drain regions. Thus an electric field is produced between the source and drain regions. The direction of the electric field is perpendicular to the plates of the capacitor through the oxide. The negative charge of electrons which are minority carriers in the P-type substrate forms an inversion layer. As the positive voltage on the gate increases, the induced negative charge in the semiconductor increases. Hence the conductivity increases and current flows from source to drain through the induced channel. Thus the drain current is enhanced by the positive gate voltage as shown in figure.

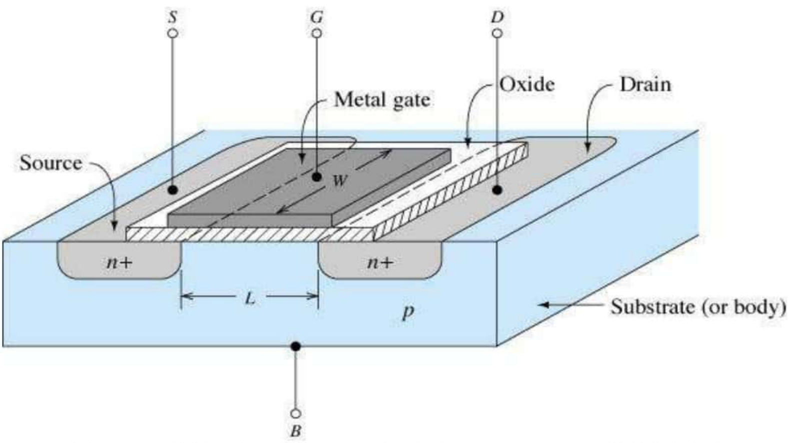

Figure 3.7: N – Channel Enhancement MOSFET

Depletion MOSFET :

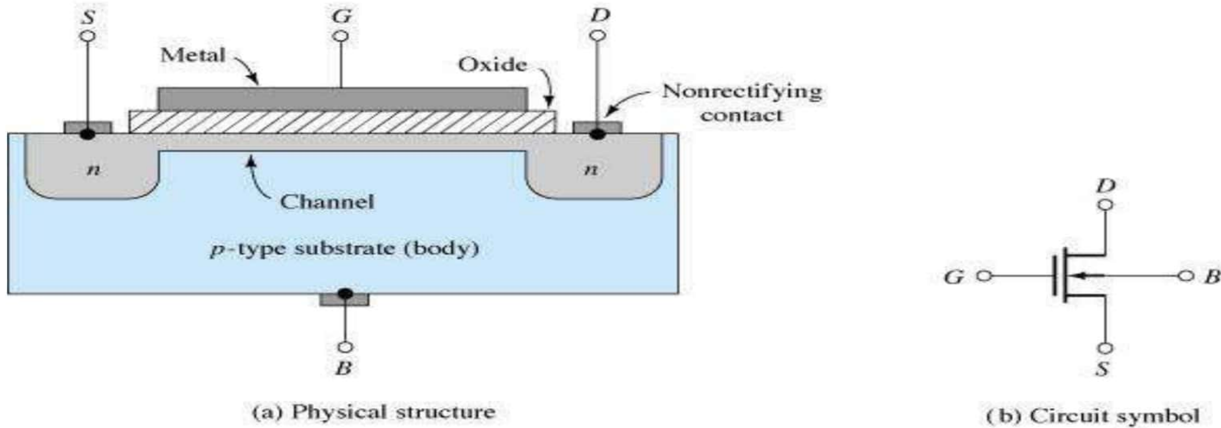

Figure 3.8: N-Channel Depletion MOSFET

The construction of an N-channel depletion MOSFET is shown in figure where an N-channel is diffused between the source and drain to the basic structure of MOSFET.

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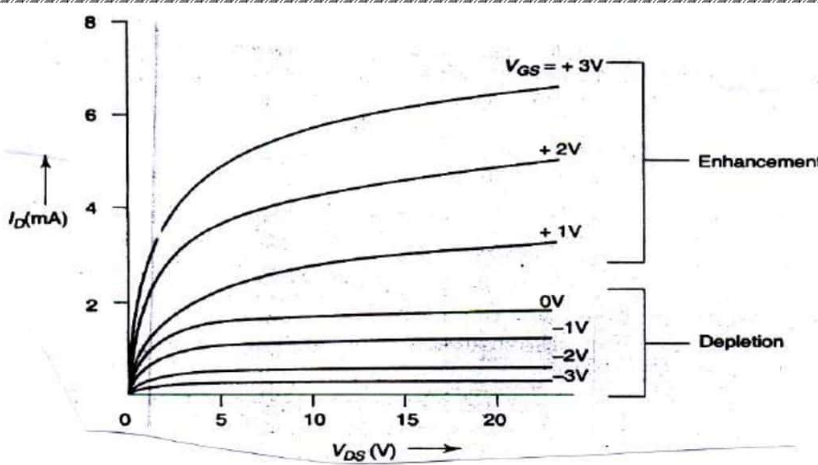

Figure 3.9: Volt-Ampere Characteristics of MOSFET

With $V_{GS} = 0$ and the drain D at a positive potential with respect to the source, the electrons (majority carriers) flow through the N-channel from S to D. Therefore the conventional current I_D flows through the channel D to S. If the gate voltage is made negative, positive charge consisting of holes is induced in the channel through SiO_2 of the gate-channel capacitor. The introduction of the positive charge causes depletion of mobile electrons in the channel. Thus a depletion region is produced in the channel. The shape of the depletion region depends on V_{GS} and V_{DS}. Hence the channel will be wedge shaped as shown in figure. When V_{DS} is increased, I_D increases and it becomes practically constant at a certain value of V_{DS}, called the pinch-off voltage. The drain current I_D almost gets saturated beyond the pinch-off voltage.

Since the current in an FET is due to majority carriers (electrons for an N-type material), the induced positive charges make the channel less conductive, and I_D drops as V_{GS} is made negative.

The depletion MOSFET may also be operated in an enhancement mode. It is only necessary to apply a positive gate voltage so that negative charges are induced into the N-type channel. Hence the conductivity of the channel increases and I_D increases. The volt-ampere characteristics are indicated in figure.

Comparison of JFET vs MOSFET:

JFETs and MOSFETs are quite similar in their operating principles and in their electrical characteristics. However, they differ in some aspects, as detailed below:

1. JFETs can only be operated in the **depletion mode** whereas MOSFETs can be operated in either depletion or in **enhancement mode**. In a JFET, if the gate is forward biased, excess- carrier injunction occurs and the gate current is substantial. Thus channel conductance is enhanced to some degree due to excess carriers but the device is never operated with gate forward biased because gate current is undesirable.
2. MOSFETs have input impedance much higher than that of JFETs. This is due to negligibly small leakage current.
3. JFETs have characteristic curves more flat than those of MOSFETs indicating a higher drain resistance.
4. When JFET is operated with a reverse bias on the junction, the gate current I_G is larger than it would be in a comparable MOSFET. The current caused by minority carrier extraction across a reverse-biased junction is greater, per unit area, than the leakage current that is supported by the oxide layer in a MOSFET. Thus MOSFET devices are more useful in electrometer applications than are the JFETs.

For the above reasons, and also because MOSFETs are somewhat easier to manufacture, they are more widely used than are the JFETs.

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UJT (Unijunction Transistor):

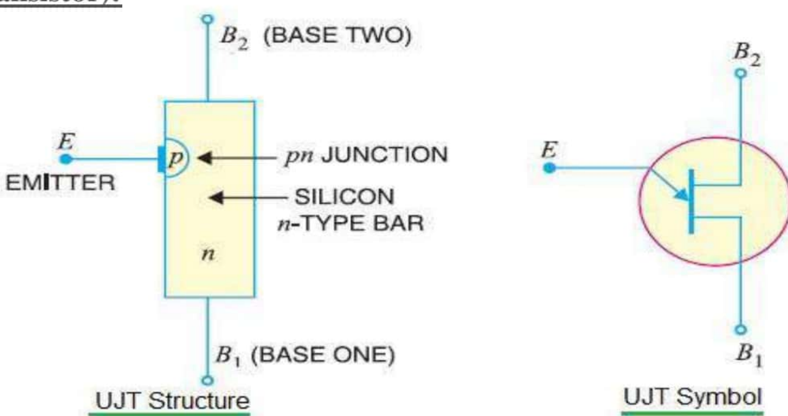

Figure 3.10.: Structure and Symbol of UJT

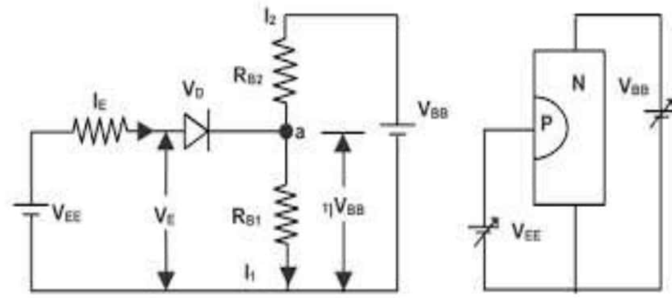

Figure 3.11.: Equivalent circuit of UJT

As shown it is n-type silicon bar with connections on both ends. The leads are referred as "B1" and "B2". Along the bar between the two bases , PN junction is constructed between P-type Emitter and N-type Bar. This lead is referred as "Emitter Lead-E". It is the short form of UnijunctionTransistor. t is 3 terminal switching device made of semiconductor materials. When UJT is triggered, I_E increases re-generatively until it is limited by V_E . Here I_E is emitter current and V_E is emitter power supply. Due to this feature, UJT is used in wide variety of applications such as sawtooth generator, pulse generator, switching etc. Device has only one PN junction and hence the term "UNI" in Unijunction Transistor (UJT). The UJT is also known as "Double Based Diode". This is due to the fact that it has only one PN junction. The two base terminals are derived from one single section of diode(or semiconductor material). In UJT, emitter part is heavily doped and n region is lightly doped. Hence resistance between two base terminals is quite high when emitter terminal is left open. The value of resistance is about 5 to 10 KOhm. UJT is a three terminal semiconductor switching device. As it has only one PN junction and three leads, it is commonly called as Unijunction Transistor.

The basic structure of UJT is shown in figure (a). It consists of a lightly doped silicon bar with a heavily-doped P-type material alloyed to its one side closer to B_2 for producing single PN junction. The circuit symbol of UJT is shown in figure (b).Here the emitter leg is drawn at an angle to the vertical and the arrow indicates the direction of the conventional current.

Characteristics of UJT:

Referring to figure (c), the interbase resistance between B_2 and B_1 of the silicon bar is $R_{BB} = R_{B1} + R_{B2}$. With emitter terminal open, if voltage V_{BB} is applied between the two bases, a voltage gradient is established along the N-type bar. The voltage drop across R_{B1} is given by $V_1 = \eta\ V_{BB}$ where the intrinsic stand-off ratio $\eta = R_{B1}/\ (R_{B1} + R_{B2})$. This voltage V_1 reverse biases the PN junction and emitter current is cut off. But a small leakage current flows from B_2 to emitter due to minority carriers. If a positive voltage V_E is applied to the emitter, the PN junction will remain reverse biased so long as V_E is less than V_1. If V_E exceeds V_1 by the cutin voltage V_r, the diode becomes forward biased. Under this condition, holes are injected into N-type bar. These holes are repelled by the terminal B_2 and are attracted by the terminal B_1. Accumulation

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of holes in E to B_1 region reduces the resistance in this section and hence emitter current I_E is increased and is limited by V_E. The device is now in the 'ON' state.

If a negative voltage is applied to the emitter, PN junction remains reverse biased and the emitter current is cut off. The device is now in the 'OFF' state.

As shown in figure, up to the peak point P, the diode is reverse biased. At P, the diode starts conducting and holes are injected into the N-layer. Hence resistance decreases thereby decreasing V_E for the increase in I_E. So there is a negative resistance region from peak point P to valley point V. After the valley point, the device is driven into saturation and behaves like a conventional forward biased PN junction diode.

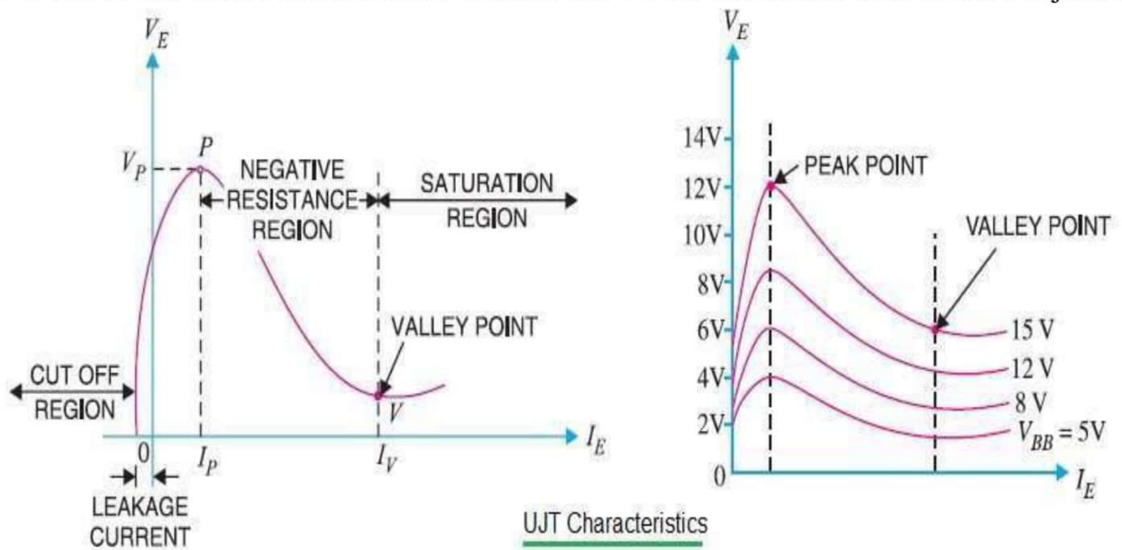

Figure 3.12: Characteristics of UJT

A unique characteristics of UJT is, when it is triggered, the emitter current increases regeneratively until it is limited by emitter power supply. Due to this negative resistance property, UJT can be employed in a variety of applications, viz. sawtooth wave generator, pulse generator, switching, timing and phase control circuits.

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Unit - IV

Analysis of Transistor amplifier ckt using Hybrid Model:

Fig: shows the Hybrid Model for common emitter configuration. Here, we shall derive expressions for current gain, input resistance, voltage gain, O/P resistance & power gain.

CE I_b h_{ie} I_c I_L R_s V_{be} $h_{re}V_{ce}$ $h_{fe}I_b$ h_{oe} V_{ce} R_L V_s

fig: h-parameter equivalent ckt of a CE amp

The hybrid equations for this configuration are given as

$$V_{be} = h_{ie}I_b + h_{re}V_{ce} \quad \text{——(1)}$$

$$I_c = h_{fe}I_b + h_{oe}V_{ce} \quad \text{——(2)}$$

$$V_{ce} = -I_cR_L \quad \text{——(3)}$$

($\because$ from fig $V_{ce} = I_LR_L$ & $I_L = -I_c$)

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(1) Current gain (A_{ie}): It is defined as the ratio of output current to the input current. ~~If the~~

$$A_{ie} = \frac{I_L}{I_b} = -\frac{I_c}{I_b} \quad \text{—— (4)}$$

Sub. the value of V_{ce} from eq.(3) in(2), we get

$$I_c = h_{fe} I_b - h_{oe} I_c R_L$$

$$\Rightarrow I_c [1 + h_{oe} R_L] = h_{fe} I_b$$

$$\Rightarrow \frac{I_c}{I_b} = \frac{h_{fe}}{1 + h_{oe} R_L} \quad \text{—— (5)}$$

Sub (5) in (4), we get

$$A_{ie} = -\frac{I_c}{I_b} = -\left(\frac{h_{fe}}{1 + h_{oe} R_L}\right)$$

$$\therefore \boxed{A_{ie} = -\left(\frac{h_{fe}}{1 + h_{oe} R_L}\right)} \qquad A_{ib} = -\left(\frac{h_{fb}}{1 + h_{ob} R_L}\right)$$

(2) Input resistance (R_{ie}): It is defined as the ratio of input voltage across the input terminals of the ampl (V_{be}) to the current (I_b).

$$R_{ie} = V_{be} / I_b \quad \text{—— (6)}$$

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Sub. the value of I_c from eq.(3) in eq.(2), we get

$$\frac{-V_{ce}}{R_L} = h_{fe} I_b + h_{oe} V_{ce}$$

$$\Rightarrow -V_{ce}\left[h_{oe} + 1/R_L\right] = h_{fe} I_b$$

$$\Rightarrow \frac{V_{ce}}{I_b} = -\frac{h_{fe}}{(h_{oe} + 1/R_L)} \quad \text{——— (7)}$$

from eq.(1), we have

$$\left(\frac{V_{be}}{I_b}\right) = h_{ie} + h_{re}\frac{V_{ce}}{I_b} \quad \text{——— (8)}$$

from equ. (7) & (8), we ~~hav~~ get

$$\boxed{R_{ie} = \frac{V_{be}}{I_b} = h_{ie} - \frac{h_{fe} h_{re}}{h_{oe} + 1/R_L}}$$

(3) Voltage gain (A_v): It is defined as the ratio of o/p voltage to the input voltage.

$$A_{ve} = \frac{V_{ce}}{V_{be}} \quad \text{——— (9)}$$

From eq.(6), $V_{be} = I_b R_{ie}$

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$$A_{ve} = \frac{V_{ce}}{I_b \cdot R_{ie}} = \frac{V_{ce}}{I_b} \cdot \left(\frac{1}{R_{ie}}\right)$$

Sub. the value of $\left(\frac{V_{ce}}{I_b}\right)$ from eq. (7), we get

$$A_{ve} = -\left[\frac{h_{fe}}{h_{oe} + (1/R_L)}\right] \cdot \frac{1}{R_{ie}}$$

(4.) output Resistance (R_{oe}):

By definition, output resistance is obtained by setting I/P as short ckt (i.e $V_{be}=0$) & O/P as open ckt (i.e Removing R_L), and now it is the ratio of O/P voltage to O/P current.

$\therefore R_{oe} = V_{ce} / I_c$ when $V_{be} = 0$

from equ.(2)

$$I_c = h_{fe} I_b + h_{oe} V_{ce}$$

$$\Rightarrow \frac{I_c}{V_{ce}} = h_{fe}\left(\frac{I_b}{V_{ce}}\right) + h_{oe} \quad \text{——— (10)}$$

from equ (1)

$$0 = h_{ie} I_b + h_{re} V_{ce}$$

$$\Rightarrow \frac{I_b}{V_{ce}} = -\frac{h_{re}}{h_{ie}} \quad \text{——— (11)}$$

from eq. (10) & (11), we get

$$\frac{I_c}{V_{ce}} = -\frac{h_{fe} h_{re}}{h_{ie}} + h_{oe}$$

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$$\Rightarrow \frac{I_c}{V_{ce}} = \frac{h_{oe}h_{ie} - h_{re}h_{fe}}{h_{ie}}$$

$$\therefore \boxed{R_{oe} = \frac{V_{ce}}{I_c} = \frac{h_{ie}}{h_{oe}h_{ie} - h_{re}h_{fe}}}$$

(5) <u>Voltage gain</u> <u>with source resistance</u>: The i/p ckt with source resistance is as shown in fig:

Now the overall voltage gain is given by

$$(A_{ve})_s = \frac{V_{ce}}{V_s} = \frac{V_{ce}}{V_{be}} \times \frac{V_{be}}{V_s}$$

$$= (A_{ve}) \cdot \frac{V_{be}}{V_s} \quad \text{—(12)}$$

I_s, R_s, R_{ie}, V_{be}, V_s, +, −

fig:

The current flowing in the ckt

$$I_s = V_s / (R_s + R_{ie})$$

$$\therefore V_{be} = R_{ie} \cdot I_s$$

$$\Rightarrow V_{be} = \frac{R_{ie} V_s}{(R_s + R_{ie})}$$

$$\Rightarrow \frac{V_{be}}{V_s} = \frac{R_{ie}}{(R_{ie} + R_s)} \quad \text{—(13)}$$

from (12) & (13), we get

$$\boxed{(A_{ve})_s = (A_{ve}) \cdot \left(\frac{R_{ie}}{R_{ie} + R_s}\right)}$$

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(6) Current gain with Source resistance:

The overall current gain is given by

$$(A_{ie})_s = \frac{I_{ce}}{I_s} = \frac{I_{ce}}{I_b} \cdot \frac{I_b}{I_s} = (A_{ie})\left(\frac{I_b}{I_s}\right) \quad \text{--- (14)}$$

The modified ckt using Norton's equivalent ckt for the source is shown in fig.

From the fig:, $I_b = \dfrac{I_s R_s}{R_s + R_{ie}}$

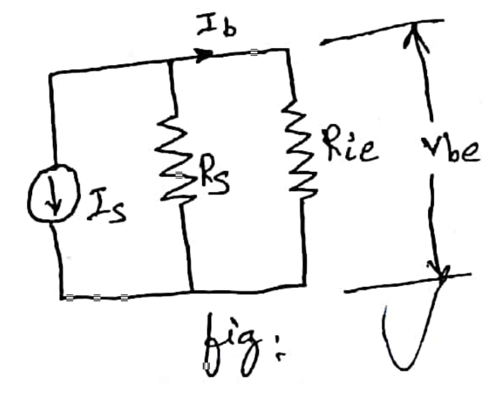

fig:

$$\therefore \frac{I_b}{I_s} = \frac{R_s}{R_s + R_{ie}} \quad \text{--- (15)}$$

Sub. (15) in (14), we get

$$(A_{ie})_s = (A_{ie})\left(\frac{R_s}{R_s + R_{ie}}\right)$$

(7) Power gain: It is the product of Voltage gain & current gain.

$P = VI$

A_{vc} A_{Ic}

$$\therefore \text{Power gain}(A_{pe}) = A_{ve} \cdot A_{ie}$$

(or)

$$\text{Overall Power gain } (A_p)_s = (A_{ve})_s \cdot (A_{ie})_s$$

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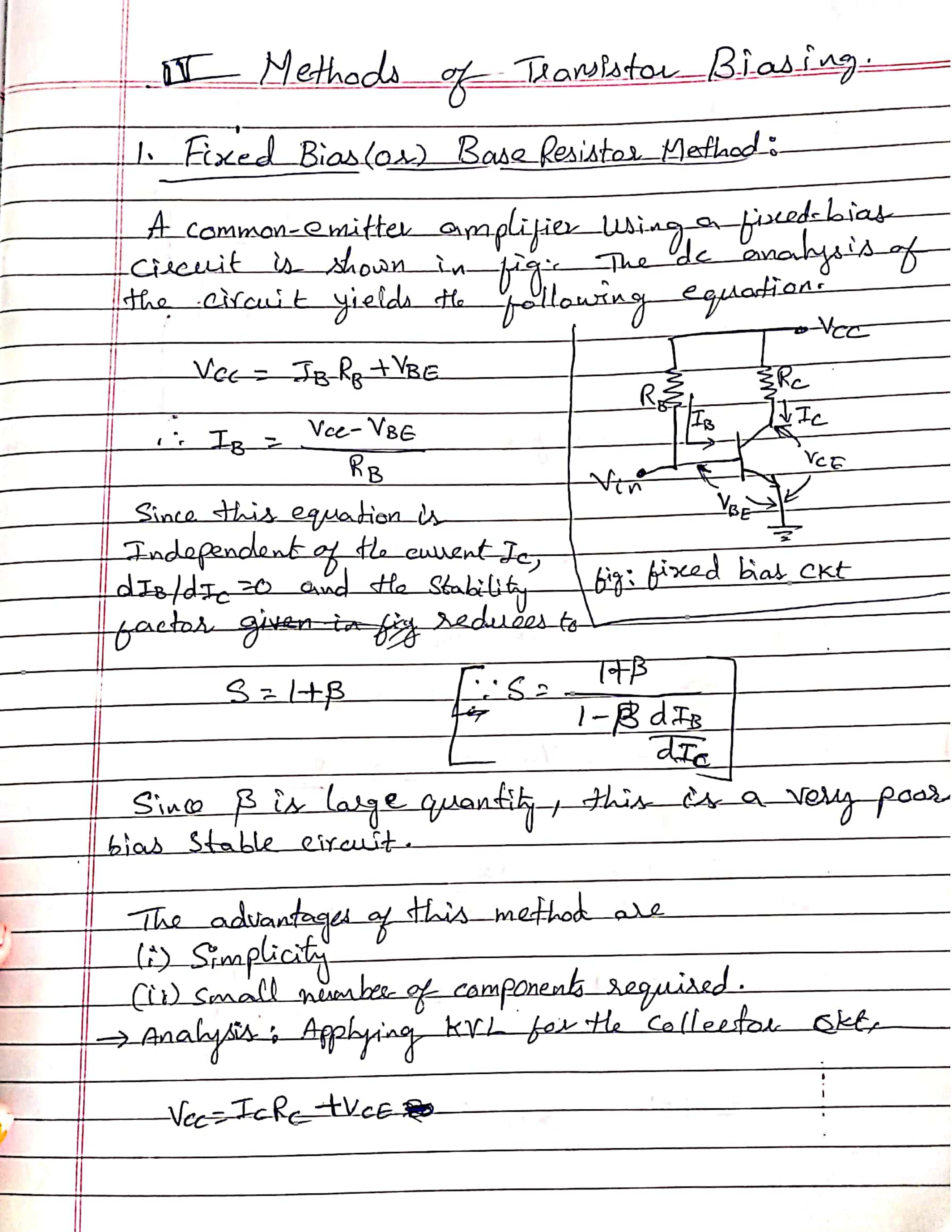

IV Methods of Transistor Biasing.

1. Fixed Bias (or) Base Resistor Method:

A common-emitter amplifier using a fixed-bias circuit is shown in fig. The dc analysis of the circuit yields the following equation.

$$V_{CC} = I_B R_B + V_{BE}$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

fig: fixed bias ckt

Since this equation is Independent of the current I_C, $dI_B/dI_C = 0$ and the Stability factor ~~given in fig~~ reduces to

$$S = 1 + \beta$$

$$\left[\because S = \frac{1+\beta}{1 - \beta \frac{dI_B}{dI_C}} \right.$$

Since β is large quantity, this is a very poor bias Stable circuit.

The advantages of this method are
(i) Simplicity
(ii) small number of components required.

→ Analysis: Applying KVL for the collector ckt,

$$V_{CC} = I_C R_C + V_{CE}$$

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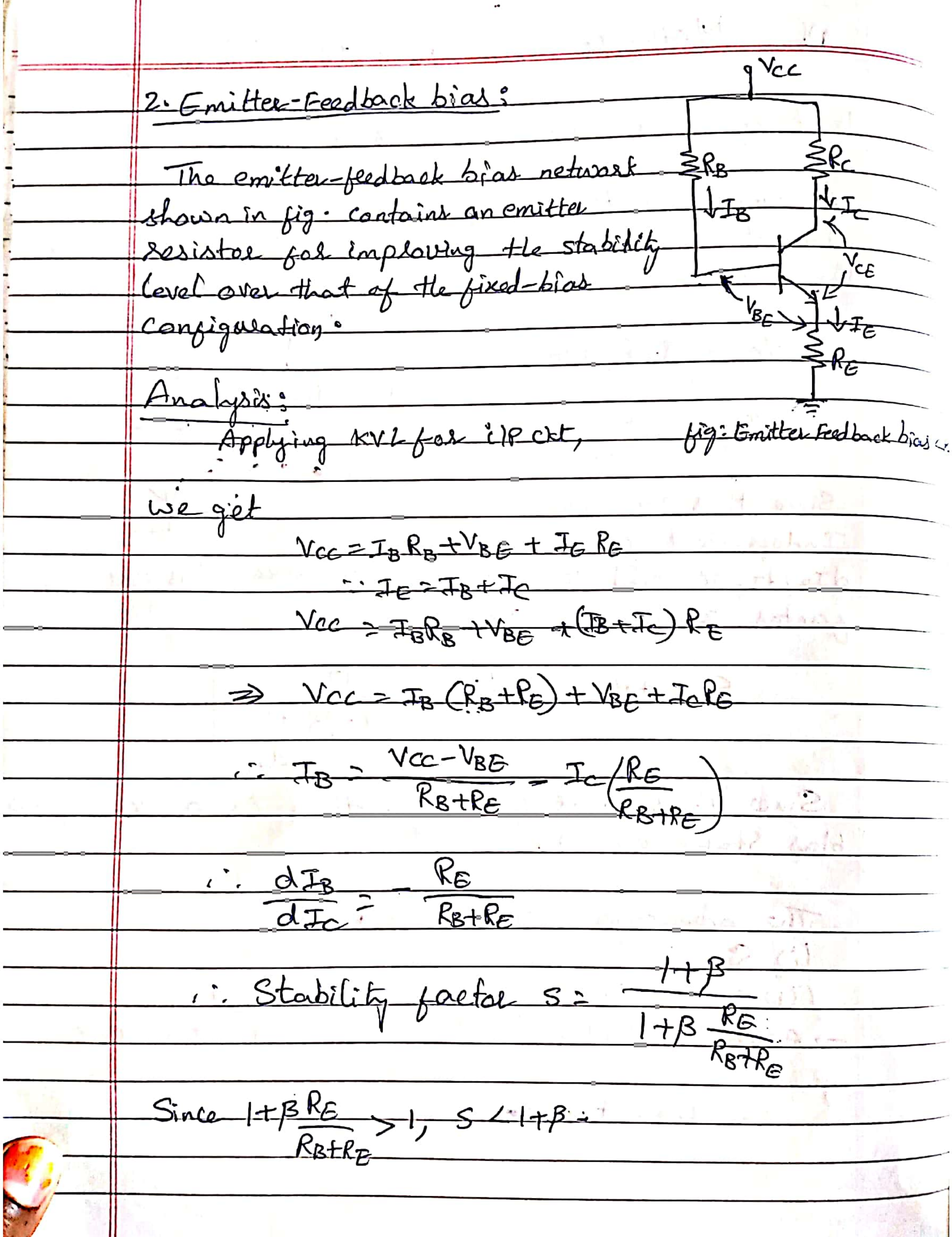

2. Emitter-Feedback bias:

The emitter-feedback bias network shown in fig. contains an emitter resistor for improving the stability level over that of the fixed-bias configuration.

fig: Emitter Feedback bias ckt.

Analysis:

Applying KVL for i/p ckt,

we get

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

$$\because I_E = I_B + I_C$$

$$V_{CC} = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$\Rightarrow V_{CC} = I_B (R_B + R_E) + V_{BE} + I_C R_E$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B + R_E} - I_C \left(\frac{R_E}{R_B + R_E} \right)$$

$$\therefore \frac{dI_B}{dI_C} = -\frac{R_E}{R_B + R_E}$$

$$\therefore \text{Stability factor } S = \frac{1+\beta}{1+\beta \frac{R_E}{R_B + R_E}}$$

Since $1+\beta \frac{R_E}{R_B+R_E} > 1$, $S < 1+\beta$.

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~~It is~~ Note that the value of the stability factor S is always lower in Emitter feedback bias circuit than that of the fixed-bias circuit.

Hence, it is clear that a better thermal stability can be achieved in this bias ckt than fixed bias ckt.

Applying KVL for o/p ckt, we get

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\therefore I_C = \frac{V_{CC} - V_{CE} - I_E R_E}{R_C}$$

&

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

3. Collector to base bias (or) Collector-feedback bias:

A common-emitter amplifier using collector-to-base bias circuit is shown in fig. This ckt is the simplest way to provide some degree of stabilization to the amplifier operating point.

fig: collector to base bias ckt.

The Analysis for i/p & o/p ckt is

$$V_{CC} = (I_B + I_C) R_C + I_B R_B + V_{BE}$$

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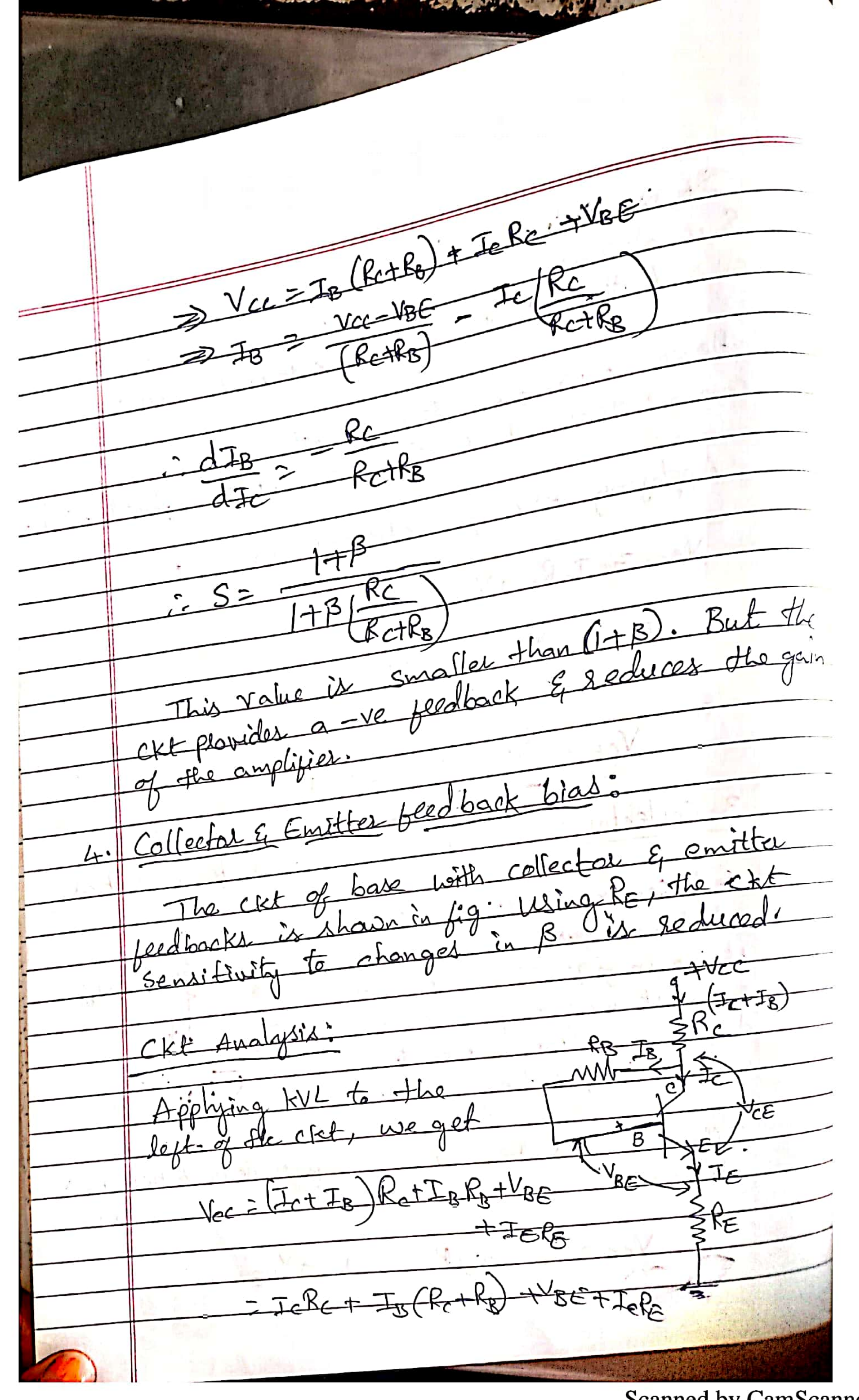

$$\Rightarrow V_{CC} = I_B(R_C+R_B) + I_C R_C + V_{BE}$$

$$\Rightarrow I_B = \frac{V_{CC}-V_{BE}}{(R_C+R_B)} - I_C\left(\frac{R_C}{R_C+R_B}\right)$$

$$\therefore \frac{dI_B}{dI_C} = -\frac{R_C}{R_C+R_B}$$

$$\therefore S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C+R_B}\right)}$$

This value is smaller than $(1+\beta)$. But the ckt provides a -ve feedback & reduces the gain of the amplifier.

4. Collector & Emitter feedback bias:

The ckt of base with collector & emitter feedbacks is shown in fig. Using R_E, the ckt sensitivity to changes in β is reduced.

Ckt Analysis:

Applying KVL to the left of the ckt, we get

$$V_{CC} = (I_C+I_B)R_C + I_B R_B + V_{BE} + I_E R_E$$

$$= I_C R_C + I_B(R_C+R_B) + V_{BE} + I_E R_E$$

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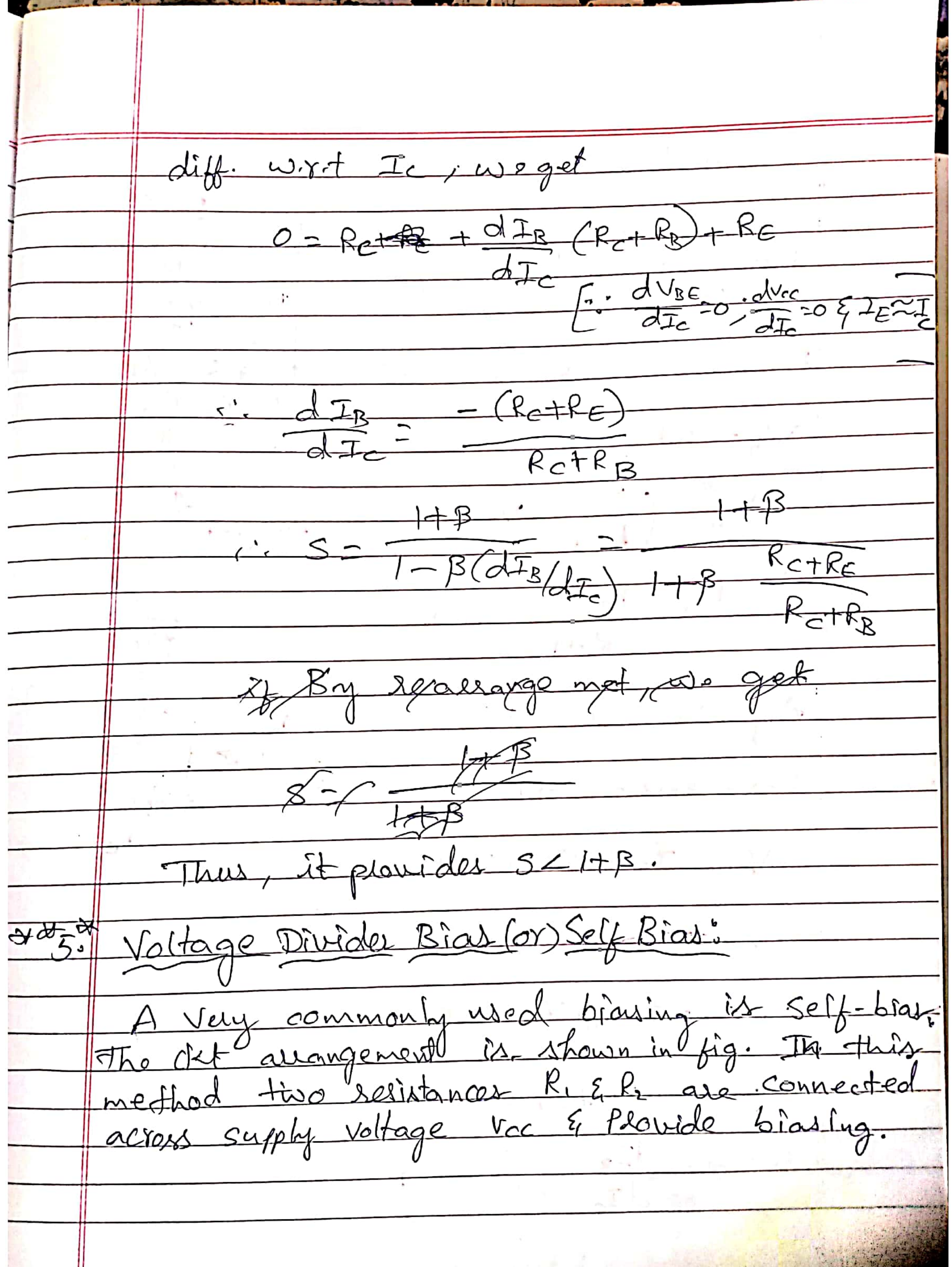

diff. w.r.t I_C, we get

$$0 = R_C + \frac{dI_B}{dI_C}(R_C+R_B) + R_E$$

$$\left[\because \frac{dV_{BE}}{dI_C} = 0,\ \frac{dV_{CC}}{dI_C} = 0 \ \& \ I_E \approx I_C\right]$$

$$\therefore \frac{dI_B}{dI_C} = \frac{-(R_C+R_E)}{R_C+R_B}$$

$$\therefore S = \frac{1+\beta}{1-\beta(dI_B/dI_C)} = \frac{1+\beta}{1+\beta\,\frac{R_C+R_E}{R_C+R_B}}$$

Thus, it provides $S < 1+\beta$.

5. Voltage Divider Bias (or) Self Bias:

A very commonly used biasing is self-bias. The ckt arrangement is shown in fig. In this method two resistances R_1 & R_2 are connected across supply voltage V_{CC} & provide biasing.

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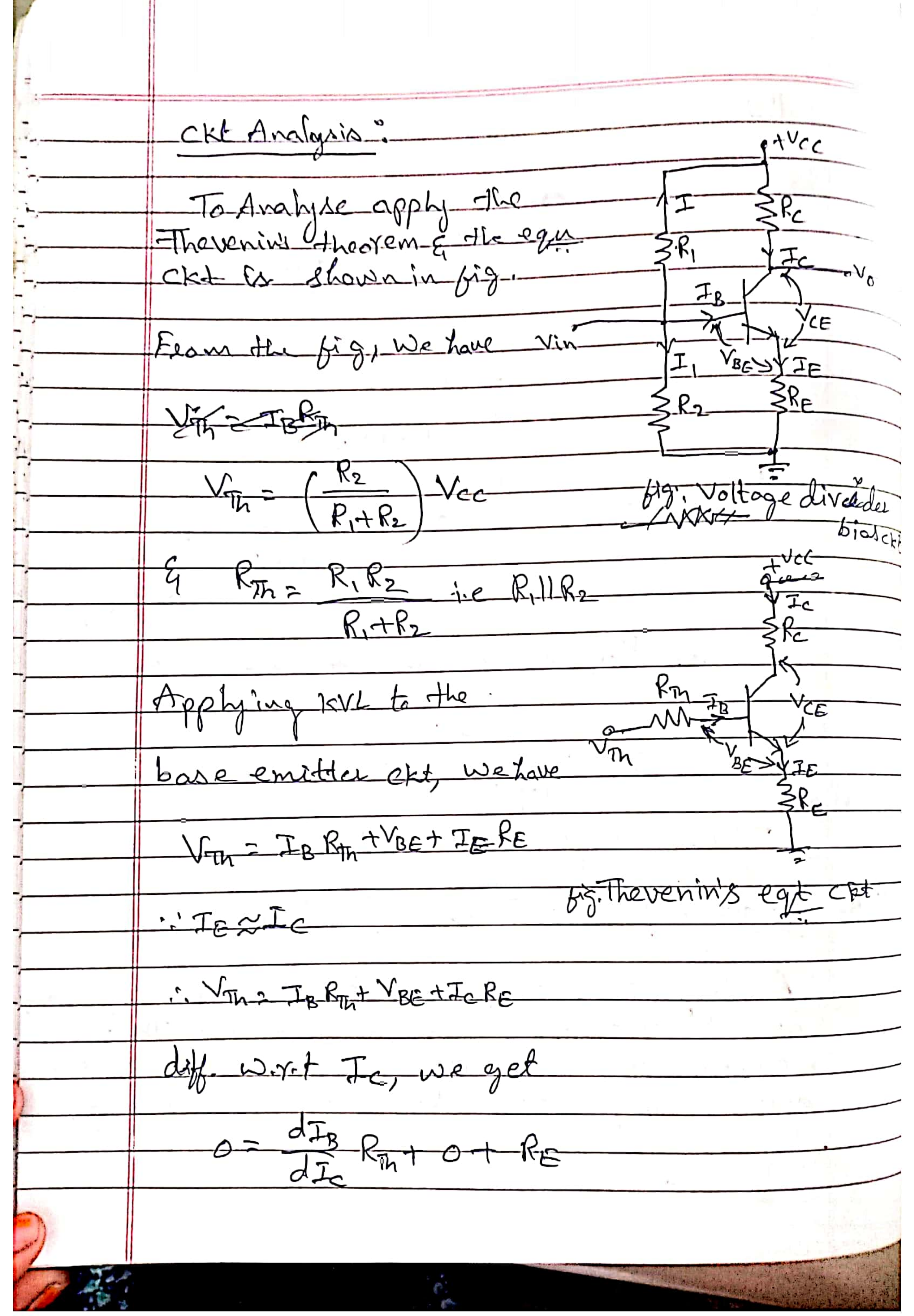

Ckt Analysis :

To Analyse apply the Thevenin's theorem & the eqv ckt is shown in fig.

From the fig, we have

~~$V_{Th} = I_B R_{Th}$~~

$$V_{Th} = \left(\frac{R_2}{R_1+R_2}\right) V_{CC}$$

& $$R_{Th} = \frac{R_1 R_2}{R_1+R_2} \quad \text{i.e } R_1 \| R_2$$

fig. Voltage divider bias ckt

Applying KVL to the base emitter ckt, we have

$$V_{Th} = I_B R_{Th} + V_{BE} + I_E R_E$$

$\because I_E \approx I_C$

$$\therefore V_{Th} = I_B R_{Th} + V_{BE} + I_C R_E$$

diff. w.r.t I_C, we get

$$0 = \frac{dI_B}{dI_C} R_{Th} + 0 + R_E$$

fig. Thevenin's eqt ckt

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$\Rightarrow \frac{dI_B}{dI_C} = -R_E/R_{Th}$

$\therefore$ Stability factor $S = \frac{1+\beta}{1-\beta \frac{dI_B}{dI_C}}$

$= \frac{1+\beta}{1+\beta \frac{R_E}{R_{Th}}}$

If R_E/R_{Th} is very small then S approaches 1 which is best for 'S'.

Ex: **Problem:**

Design a fixed bias ckt using Si transistor with following specifications $V_{CC} = 16V$, $V_{BE} = 0.7V$, $V_{CEQ} = 8V$ & $I_{CQ} = 4mA$ & $\beta = 50$.

Sol: Given data:

For Si transistor $V_{BE} = 0.7V$

$V_{CC} = 16V$

$V_{CEQ} = 8V$

$I_{CQ} = 4mA$ &

To Find R_B & R_C: $\beta = 50$

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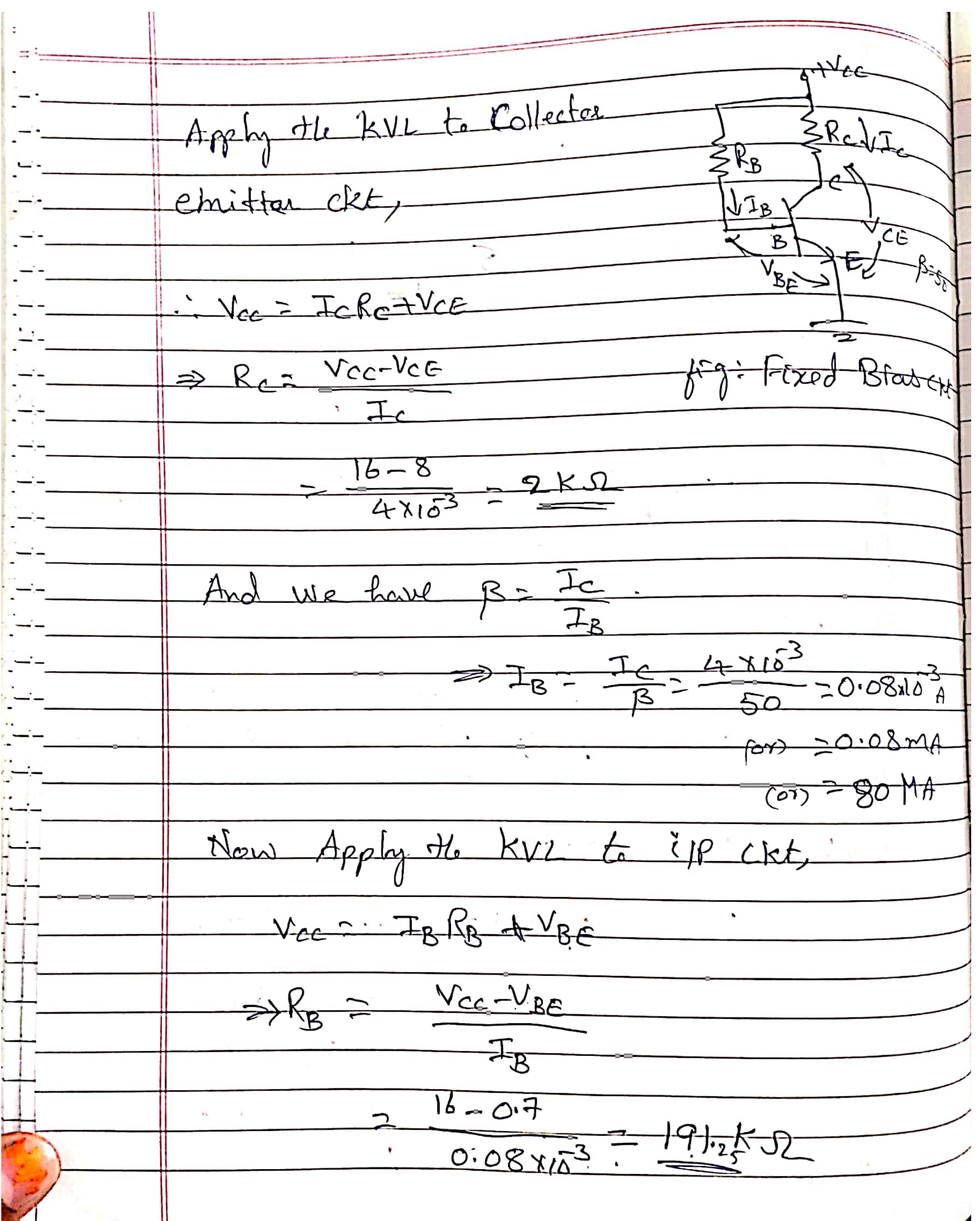

Apply the KVL to Collector emitter ckt,

fig: Fixed Bias ckt

$\therefore V_{CC} = I_C R_C + V_{CE}$

$\Rightarrow R_C = \dfrac{V_{CC} - V_{CE}}{I_C}$

$= \dfrac{16 - 8}{4 \times 10^{-3}} = 2\,K\Omega$

And we have $\beta = \dfrac{I_C}{I_B}$.

$\Rightarrow I_B = \dfrac{I_C}{\beta} = \dfrac{4 \times 10^{-3}}{50} = 0.08 \times 10^{-3}\,A$

(or) $= 0.08\,mA$

(or) $= 80\,\mu A$

Now Apply the KVL to i/p ckt,

$V_{CC} = I_B R_B + V_{BE}$

$\Rightarrow R_B = \dfrac{V_{CC} - V_{BE}}{I_B}$

$= \dfrac{16 - 0.7}{0.08 \times 10^{-3}} = 191.25\,K\Omega$

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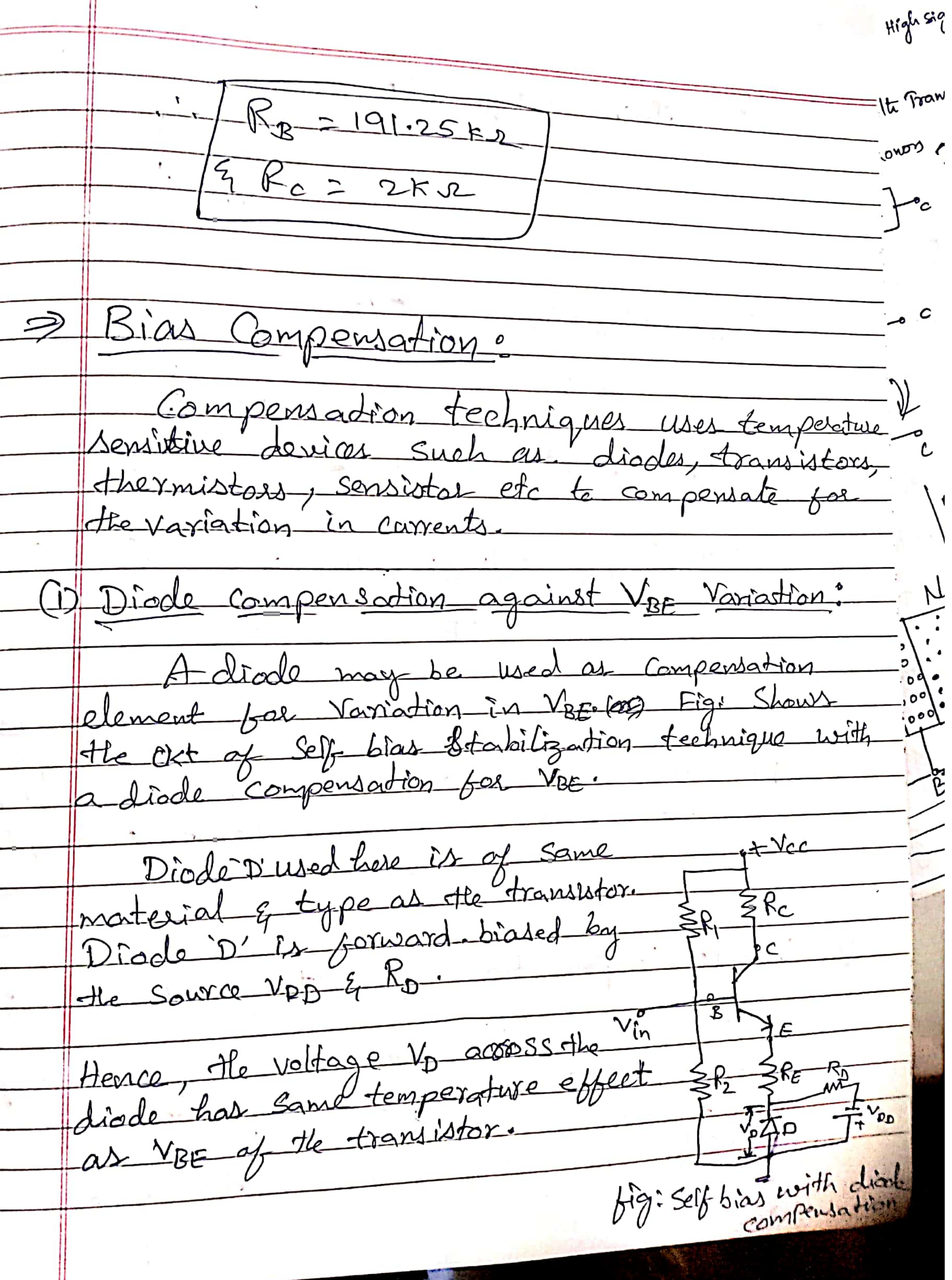

$\therefore$ $R_B = 191.25\,k\Omega$

& $R_C = 2\,k\Omega$

⇒ Bias Compensation:

Compensation techniques uses temperature sensitive devices such as diodes, transistors, thermistors, sensistor etc to compensate for the variation in currents.

(1) Diode compensation against V_{BE} Variation:

A diode may be used as compensation element for variation in V_{BE} (or) Fig: Shows the ckt of Self bias stabilization technique with a diode compensation for V_{BE}.

Diode 'D' used here is of same material & type as the transistor. Diode 'D' is forward biased by the source V_{DD} & R_D.

Hence, the voltage V_D across the diode has same temperature effect as V_{BE} of the transistor.

+Vcc, R_1, R_C, C, B, E, V_{in}, R_2, R_E, R_D, V_{DD}, V_D, D

fig: Self bias with diode compensation

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Using Thevenin's Equ ckt, analysis as follows.

$$V_{Th} = I_B R_{Th} + V_{BE} + I_E R_E - V_D$$

$\because I_E = I_B + I_C$

$\Rightarrow$

$$V_{Th} = I_B R_{Th} + V_{BE} + I_B R_E + I_C R_E - V_D$$

$$\Rightarrow I_C = \frac{V_{Th} - I_B[R_{Th} + R_E] - [V_{BE} - V_D]}{R_E}$$

+Vcc, RC, RTh, VTh, IB, VBE, IE, RE, RD, VD, D, VDD

fig: Thevenin's equ ckt

Since variation in V_{BE} with temperature is the same as the variation in V_D with temperature, hence the quantity $(V_{BE} - V_D)$ remains constant. So, the current I_C remains constant inspite of the variation in V_{BE}.

2. Diode Compensation against I_{CO} Variation:

Fig: Shows the ckt of transistor ampl with diode 'D' used for compensation of variation in I_{CO}.

The diode D & the transistor are of

the same type & same material. So, the reverse saturation current I_0 of the diode will increase with temperature at the same rate as the transistor collector saturation current I_{co}.

Diode D is Reverse biased by V_{BE}. We know that, from fig:

$$I_B = I - I_0$$

& We have $I_C = \beta I_B + (1+\beta) I_{co}$

$$\Rightarrow I_C = \beta(I - I_0) + (1+\beta) I_{co}$$

& $\Rightarrow I_C = \beta I - \beta I_0 + (1+\beta) I_{co}$

fig: Transistor amplifier with Diode compensation for I_{co}

if $\beta >> 1$

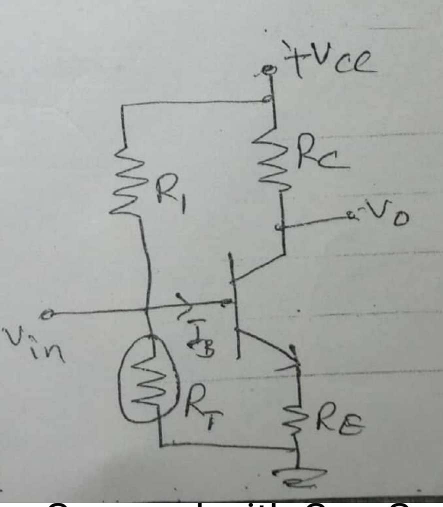
$$\therefore I_C = \beta I - \beta I_0 + \beta I_{co}$$

$$I_C = \beta I + \beta [I_{co} - I_0]$$

In above expression, $(I_{co} - I_0)$ is constant & hence I_C remains same.

(3) Thermistor Compensation:

Fig: Shows the Self bias ckt with thermistor (R_T) across B & Emitter.



Thermistor has a -ve temperature coefficient of resistance. i.e, its

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resistance decreases with increase in temperature.

When temperature increases, R_T decrease & current flow increase through it, hence I_B decreases. So, I_C is ~~controlled~~ constant.

4. Sensistor Compensation:

Fig: show the Sensistor Compensation ckt with R_S.

Sensistor has a +ve temperature coefficient of resistance. i.e., its resistance ~~d~~ Increases with Increase in temperature.

When temperature increases; R_S increases & current flowing through it decreases, So, I_B also decreases, hence I_C remainse same.

fig: Sensistor Compensation ckt.

REQUIREMENTS OF A BIASING CIRCUIT :-

→ The E-B jn must be F.B (0.6V to 0.7V) & C-B jn must be R.B. i.e., the tr must be operated in the middle of the active region or Q-Point should be fixed at the centre of the active region.

→ The ckt design should provide a degree of temperature stability.

→ The Q-Point should be made independent of tr. parameters (such as β).

To maintain the Q-Point stable by keeping I_c, & V_{CE} constant so that the tr. will always work in active region, the following techniques are normally used

(i) Stabilization techniques.

(ii) Compensation techniques.

** Stabilization techniques refer to the use of resistive biasing ckts which allow I_B to vary so as to keep I_c relatively const with variations in I_{co}, β, and V_{BE}.

→ Compensation techniques refer to the use of temp - sensitive devices such as diodes, transistors, thermistors etc. which provide compensating voltages & currents to maintain Q- point stable.

** Stability Factors :-

→ Stabilization techniques give different biasing ckts which are discussed in the following sections. In order to compare the stability provided by these ckts, one term is raised called stability factor, which indicates the degree of change in Q - point due to variation in temperature. Since there are three variables which are temp. dependent, we can define three stability factors as below:

(i) $S = \left.\dfrac{\partial I_c}{\partial I_{co}}\right|_{V_{BE},\, \beta\ const}$ (or) $S = \dfrac{\Delta I_c}{\Delta I_{co}}$

(ii) $S' = \left.\dfrac{\partial I_c}{\partial V_{BE}}\right|_{I_{co},\, \beta\ const}$ (or) $S' = \dfrac{\Delta I_c}{\Delta V_{BE}}$

(iii) $S'' = \left.\dfrac{\partial I_c}{\partial \beta}\right|_{I_{co},\, V_{BE}\ const}$ (or) $S'' = \dfrac{\Delta I_c}{\Delta \beta}$

→ Ideally, stability factor should be perfectly zero to keep Q-Point stable.

→ Practically stability factor should have the value as min. as possible. Thermal stability of a ckt is assessed by deriving a stability factor, S.

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The total change in the I_C due to change in I_{CO}, V_{BE} & β_{dc} is given by,

$$\Delta I_C = S\Delta I_C + S'\Delta V_{BE} + S''\Delta\beta.$$

Mathematical Exp'n for Stability factor :-

The Stability factor is expressed as the rate of change of I_C with respect to reverse saturation current while keeping the CE-current gain 'β' and Base current 'I_B' as const.

Mathematically, the stability factor may be stated as

$$S = \frac{dI_C}{dI_{CO}}\bigg|_{\beta \,\&\, I_B = const}.$$

The stability factor 'S' is a measure of bias stability of a transistor ckt. It may be observed that higher the value of stability factor, poor is the stability.

* **Derivation:-**

Since, the value of collector current in a transistor is given as

$$I_C = \beta I_B + (1+\beta)I_{CO} \rightarrow (1)$$

Here, I_C = ~~βI_B~~ Collector Current

I_B = Base current.

I_{CO} = Reverse Saturation Current

β = CE current gain.

Differentiating (1) w.r.to I_C

$$1 = \frac{d}{dI_C}(\beta I_B) + \frac{d}{dI_C}(1+\beta)I_{CO}$$

Assuming 'β' as const, we have

$$1 = \beta\frac{dI_B}{dI_C} + (1+\beta)\cdot\frac{dI_{CO}}{dI_C}$$

$$= \beta\cdot\frac{dI_B}{dI_C} + (1+\beta)\cdot\frac{1}{S}$$

x'y with 's' on B.s $\left(\because S = \frac{dI_C}{dI_{CO}}\right)$

(or) $S = S\cdot\beta\cdot\frac{dI_B}{dI_C} + (1+\beta)$

$$S\left[1 - \beta\left(\frac{dI_B}{dI_C}\right)\right] = 1+\beta$$

$$\boxed{S = \frac{1+\beta}{1-\beta\left(\frac{dI_B}{dI_C}\right)}} \rightarrow (2)$$

The above exp'n for stability factor is a general exp'n for any biasing ckt.

Stability factor for CE config'n :-

For CE, I_C is given as

$$I_C = \beta I_B + (1+\beta)I_{CO}.$$

But $S = \frac{dI_C}{dI_{CO}}\bigg|_{\beta \,\&\, I_B = const}.$

Diff w.r.to I_{CO}

$\therefore$ ~~$I_C = 0 + (1+\beta)I_{CO}$~~

$$\Rightarrow \frac{dI_C}{dI_{CO}} = 0 + (1+\beta)$$

$$\Rightarrow \boxed{S = 1+\beta}$$

For ex: if $\beta = 50$, $S = 51$.

Indicates that I_C changes 51 times change in I_{CO}. Hence, in CE, I_C dependence on

I_{CO} which in turn depends on the temperature.

∴ CE bias stabilization is of utmost importance to improve the stability factor.

Methods of transistor Biasing:-

There are 4 methods of transistor biasing which are most widely used:

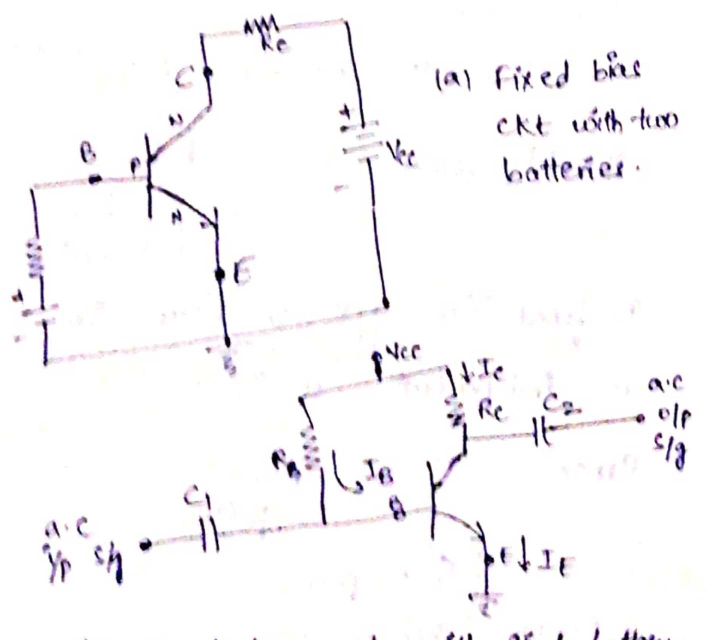
(1) Fixed bias (2) collector to base bias

(3) Self-bias (or) Voltage divider Bias

(4) Emitter Bias.

** FIXED BIAS CIRCUIT :-

The fig shows a fixed bias ckt. In this ckt two d.c batteries are used. The battery V_{BB} & V_{CC} are used. The battery V_{BB} is a low value battery & V_{CC} is a high value battery.



(a) Fixed bias ckt with two batteries.

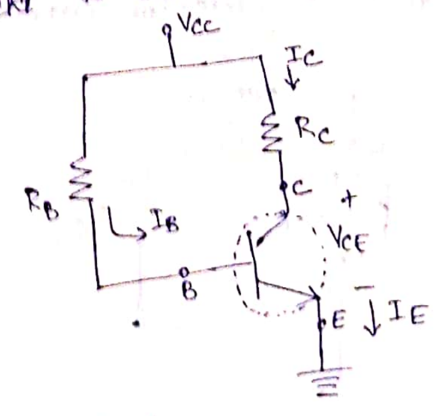
(b) Fixed bias ckt with single battery.

The fixed bias ckt may be replaced with more practical ckt in which a single supply V_{CC} is used. In this ckt, both the base and collector resistors are connected to +ve side of battery V_{CC} as shown in fig. (b).

→ It is the simplest d.c bias configuration. For the d.c analysis we can replace capacitor with an O.C b'coz the reactance of a capacitor for d.c is

$$X_C = \frac{1}{2\pi f C} = \frac{1}{2\pi (0) C} = \infty .$$

The d.c equivalent of a fixed bias ckt as shown is

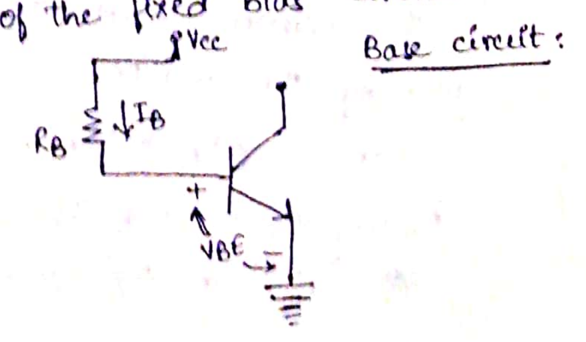


D.C Analysis

Now, we will find the value of d.c bias voltages & currents in the base & collector portions of the transistor.

Case(i) :- Consider the i/p portion of the fixed bias circuit.

Base circuit :



Applying KVL for the i/p side, we get

$$V_{CC} = I_B R_B + V_{BE} \quad \text{--- (1)}$$

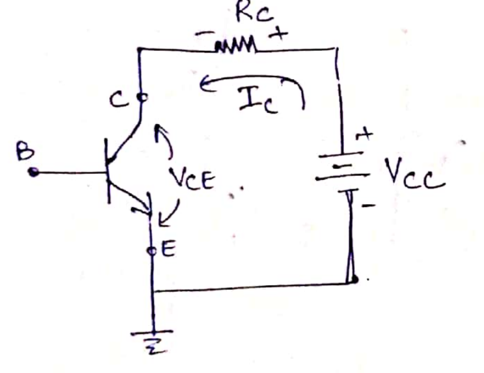
(or) $I_B R_B = V_{CC} - V_{BE}$

(or) $I_B = \dfrac{V_{CC} - V_{BE}}{R_B}$ --- (2)

The values of voltages V_{CC} & V_{BE} are fixed, therefore value of I_B depends on the base resistor R_B. For simplification, we may neglect the value of V_{BE} b'coz it is small.

Hence, $I_B \approx \dfrac{V_{CC}}{R_B}$ --- (3)

Case (ii): collector current:



Considering the o/p portion of the fixed bias ckt,

Applying KVL for o/p portion

$$I_C R_C + V_{CE} = V_{CC}$$

(or) $V_{CE} = V_{CC} - I_C R_C$ --- (4)

The collector current 'I_C' is given by the relation

$$I_C = \beta I_B \quad \text{--- (5)}$$

Putting the value of I_B, (3) in (5)

$$\therefore I_C = \beta\left(\frac{V_{CC}}{R_B}\right) \quad \text{--- (6)}$$

~~From Q-poin~~

The I_C is β times greater than the base current and doesnot depend upon the collector-resistor. Hence, Q-point for fixed-bias ckt is

$$Q \equiv (V_{CE}, I_C)$$

where $V_{CE} = V_{CC} - I_C \cdot R_C$

and $I_C = \beta I_B = \beta\left(\dfrac{V_{CC}}{R_B}\right)$.

From Q-Point, it may be observed that the values of collector current I_C and collector-emitter voltage depend upon the value of 'β' which in turn depends strongly on temp.

It means that Q-point will change with change in 'β' due to variation in temp.

This shows that a stable Q-point cannot be achieved in a fixed-bias ckt.

Stability Factor for Fixed-Bias ckt:

Stability factor $S = \dfrac{\beta+1}{1-\beta\left[\frac{dI_B}{dI_C}\right]}$

In fixed bias $\dfrac{dI_B}{dI_C} = 0$ b'coz I_B is independent of I_C.

Hence, $S = \dfrac{\beta+1}{1-\beta(0)}$

$$\boxed{S = \beta+1}$$

If $\beta = 100$ then $S = 101$.

So, I_C changes 101 times for any change in I_{CO}.

Due to large value of 'S', stability is poor.

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TRANSISTOR BIASING AND THERMAL STABILIZATION :-

BIASING :-

The basic function of a transistor is its amplification. For faithful amplification (amplified magnitude of a signal w/o any change in shape), the following conditions must be satisfied.

(i) The Emitter-base junction should be f/w biased.
(ii) The collector-base junction should be reverse biased.
and (iii) There should be proper zero signal collector current.

The proper flow of zero signal collector current (proper operating point of transistor and the maintenance of proper collector - emitter voltage during the passage of signals as transistor biasing.

When a transistor is not properly biased, it works inefficiently & produce distortion in the O/P signal. Hence a transistor should be biased properly. Transistor is biased either with the help of battery or associating a circuit with transistor. The latter method is generally employed. The circuit used with transistor is known as biasing circuit.

STABILISATION :-

The maintenance of stable operating point is known as stabilisation.

Firstly, many of the transistor parameters are markedly temperature sensitive. Secondly, when a transistor is replaced by another of same type, then there is a spread in the values of transistor parameters. The problem of operating point instability is not faced in case of vaccum tubes. The reason is that

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the parameters are almost independent of working temperature and it is also possible to manufacture tubes with identical characteristics. So, stabilization of the operating point is necessary due to the following reasons :-

Temp↑ I_{CO} ↓ β ← V_{BE}

(a) Temperature dependent of I_C

(b) Individual Variations and

(c) Thermal Runaway.

(a) <u>Temperature dependence of I_C</u> :- The instability of I_C is caused by the following three sources:

(i) The collector leakage current I_{CO} is greatly influenced by temperature changes. The I_{CO} doubles for every 10°C rise in temperature.

(ii) Increase of β with increase of temperature.

(iii) Variation of V_{BE} (Base to Emitter Voltage) with temperature.

Here it should be remembered that V_{CE} also changes with temperature but the change is very small. Hence, I_C is almost independent of V_{CE}.

(b) <u>Individual Variations</u> :-

When a transistor is replaced by another transistor of the same type, the value of β and V_{BE} are not exactly the same. Hence, ~~it~~ is the operating point is changed. So, it is necessary to stabilise the operating point irrespective of individual variations in transistor parameters.

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Thermal Runaway :-

Depending upon the construction of a transistor, the collector junction can withstand a max. temp. The range of temp is between 60°C to 100°C for Ge transistor and 150°C to 225°C for Si transistor.

If the temperature increases beyond this range then transistor burns out. The increase in the collector junction temperature is due to thermal runaway. When the collector current flows in a transistor, it is heated. i.e., its temperature increases. This further increases the transistor temperature. Consequently, there is a further increase in transistor leakage current. The action becomes cumulative, and the transistor may immediately burn out. This self-destruction of an unstabilized transistor is known as thermal runaway.

The following techniques are used for stabilization :

(i) Stabilization Techniques :- This technique uses a resistive biasing circuit which permits such a variation of base current I_B as to maintain I_C almost constant inspite of variation of I_{CO}, β and V_{BE}.

(ii) Compensation Techniques :- In this technique temperature sensitive devices such as diodes, transistors, thermistors etc. are used. Such devices produce compensating voltages and currents in such a way that the operating point is maintained stable.

STABILITY FACTOR :-

The stability factor 'S' is defined as the rate of change of collector current I_C with respect to the reverse saturation current I_{CO}, keeping β and V_{BE} constant i.e.,

(i) $$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{\Delta I_C}{\Delta I_{CO}} \quad \text{———} \quad (1)$$

5, 7, 13, 14, 16, 17, 20, 22, ~~39~~, 41, 44, ~~45~~, 47, 54, 56, 58, ~~59~~. C4.

(ii) $$S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\,\beta\text{-constant}} = S' = \frac{\Delta I_C}{\Delta V_{BE}} \quad \text{———} \quad (2)$$

(iii) $$S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO},\,V_{BE}\ \text{constant}} = S'' = \frac{\Delta I_C}{\Delta \beta}$$

Since, there are three variables which are temp. dependent, we can define three stability factors as ~~below~~ above.

Key Points :-

1. Ideally, stability factor should be perfectly zero to keep operating point stable.
2. Practically stability factor should have the value as minimum as possible. Thermal stability of a circuit is assessed by deriving a stability factor, 'S'.

Stability Factor 'S' :-

For a CE configuration collector current is given as

$$I_C = \beta I_B + I_{CEO}$$

or

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

When I_{CBO} changes by ΔI_{CBO}, I_B changes by ∂I_B and I_C changes by ∂I_C. So this eq'n becomes,

$$\partial I_C = \beta\, \partial I_B + (1+\beta)\, \partial I_{CBO}$$

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$$1 = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta) \frac{\partial I_{CBO}}{\partial I_C}$$

$$1 - \beta \frac{\partial I_B}{\partial I_C} = (1+\beta) \frac{\partial I_{CBO}}{\partial I_C}$$

$$\frac{\partial I_{CBO}}{\partial I_C} = \frac{1 - \beta(\partial I_B / \partial I_C)}{(1+\beta)}$$

$$S = \frac{\partial I_C}{\partial I_{CBO}}$$

$$S = \frac{(1+\beta)}{1 - \beta(\partial I_B / \partial I_C)}$$

This eq'n can be considered as a standard eq'n for deviation for stability factors of other biasing ckts.

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LOAD LINE ANALYSIS CH-4

(i) DC Load line :-

→ The d.c. load line is a line on the O/p charac. of a transistor which gives the values of I_c & V_{ce} corresponding to zero signal cond's.

Consider the output section of a basic amplifier circuit shown in fig. (2). Applying Kirchhoff's voltage law, we have

$$V_{CC} = R_c I_c + V_{ce} + R_e I_e$$

or $$V_{CC} = V_{ce} + I_c (R_c + R_e) \qquad (\because I_e \approx I_c)$$

Here V_{CC} and $(R_c + R_e)$ are constant, therefore it represents a straight line known as load line. The load line can be plotted in the following way :

(i) We put $I_c = 0$, then V_{ce} would be maximum

$\therefore \quad (V_{ce})_{max} = V_{CC}$

This locates a point (say B) of the load line on X-axis. The coordinates of this point are (V_{CC}, 0)

(ii) We put $V_{ce} = 0$, then $I_c = V_{CC} / (R_c + R_e)$. This locates the second point (say A) of the load line on Y-axis. The coordinates of this point are $\{0, V_{CC}/(R_c + R_e)\}$.

The d.c. load line is shown in fig. (3).

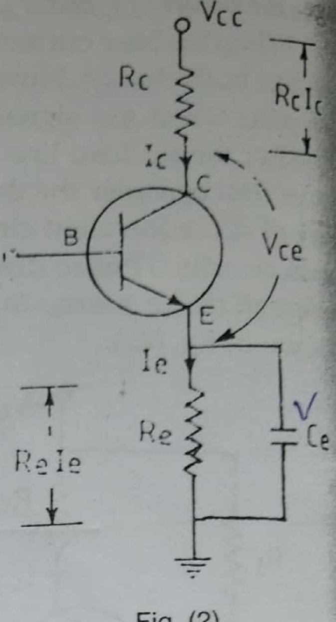

Fig. (2)

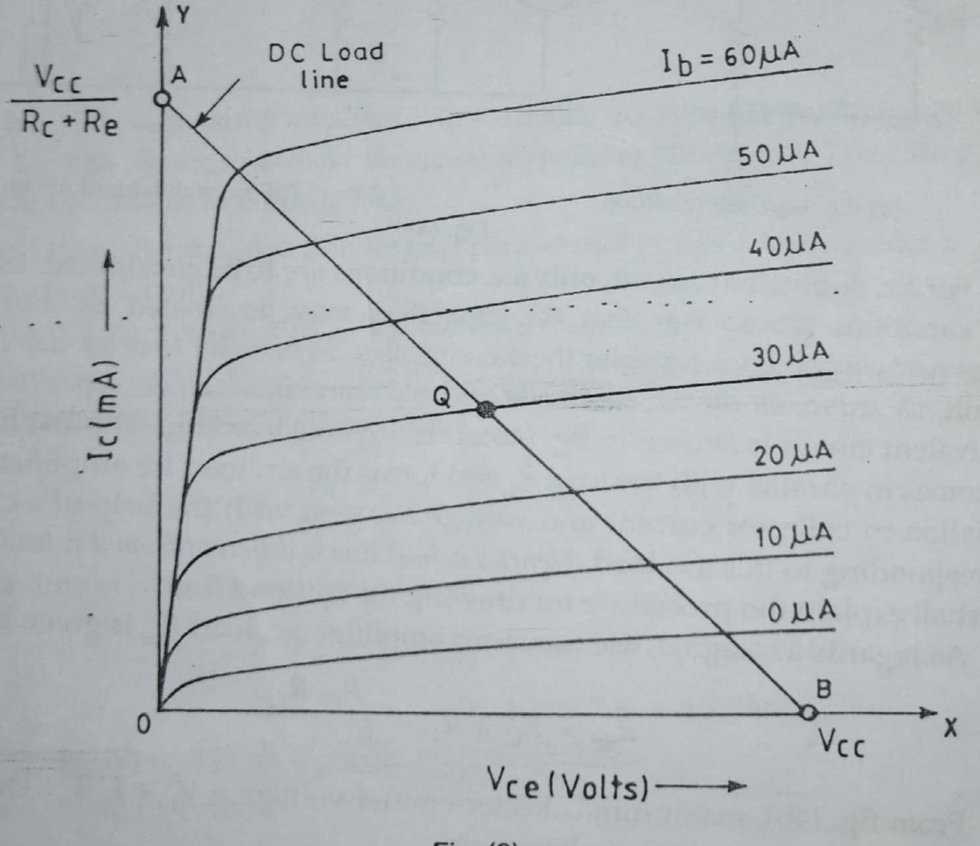

Fig. (3)

If I_b = 30 μA is set by the biasing circuit, then the intersection of 30 μA and load line *i.e.*, a point Q in fig. (3) gives the *operating point*.

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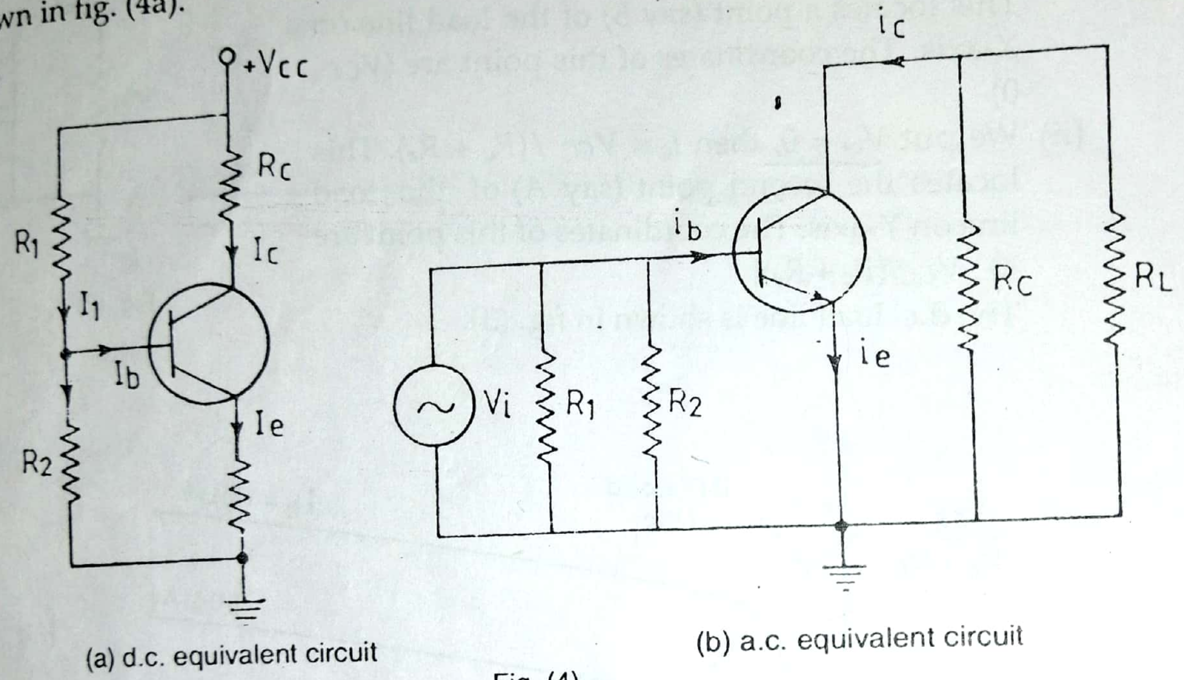
(2) A.C. load line.

The a.c. load line is a line on the output-characteristics of a transistor circuit which gives the values of I_c and V_{ce} when signal is applied.

When the base current is changed in d.c. bias, the collector current and collector voltage both change. Now the operating point shifts on d.c. load line. Actually this happens when a.c. signal is applied to the transistor. Now the question is that whether the a.c. load line is the same as d.c. load line. To understand this question, let us first consider the d.c. and a.c. equivalent circuits of a transistor amplifier. In case of d.c. equivalent circuit, no signal is applied and all the capacitors look like open circuits. Thus to draw the d.c. equivalent circuit, we *open all the capacitors and reduce all the a.c. sources to zero.* The d.c. equivalent circuit of a transistor amplifier is shown in fig. (4a).



(a) d.c. equivalent circuit

(b) a.c. equivalent circuit

Fig. (4)

For a.c. equivalent circuit, only a.c. conditions are to be considered. In this case, the variations are so fast that the capacitors may be treated as short circuits. Moreover we need not consider the d.c. supplies. So in order to draw a.c. equivalent circuit, *we reduce all the d.c. sources to zero and short circuit all the capacitors.* The a.c. equivalent circuit is shown in fig. (4b). It is obvious from fig. (4b) that the resistor R_C comes in parallel with the load R_L and forms the a.c. load for amplifier. Now the variation in collector current and voltage are seen with the help of a.c. load line corresponding to this a.c. load. *Hence a.c. load line is different from d.c. load line.* Now we shall explain the procedure for drawing the a.c. load line.

As regards a.c. signal, the transistor amplifier a.c. load R_{ac} is given by

$$R_{ac} = R_C \parallel R_L = \frac{R_C R_L}{R_C + R_L}$$

From fig. (4b), maximum collector-emitter voltage = $V_{ce} + I_c R_{ac}$. This locates a point C on collector emitter voltage axis.

Maximum collector current = $I_c + V_{ce} / R_{ac}$. This locates a point *D* on collector current axis.

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The a.c. load line is shown in fig. (5).

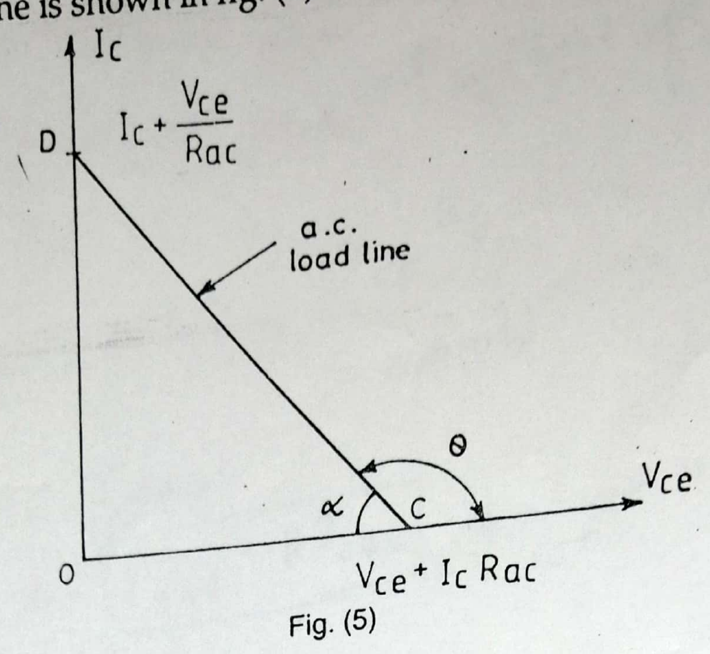

Fig. (5)

The slope of load line is given by

$$\tan\alpha = \frac{OD}{OC} = \frac{[I_c + (V_{ce}/R_{ac})]}{[V_{ce} + I_c R_{ac}]}$$

$$= \frac{[I_c + (V_{ce}/R_{ac})]}{R_{ac}\ [(V_{ce}/R_{ac}) + I_c]}$$

$$= \frac{1}{R_{ac}}$$

Example 1. *In a transistor amplifier,* $R_C = 10$ KΩ, $R_L = 30$ KΩ *and* $V_{CC} = 20$ V. *The value of* R_1 *and* R_2 *are so as to fix the operating point at* 10 V, 1 mA. *Draw the d.c. and a.c. load lines. Assume* R_e *is negligible.*

D.C. load line For d.c. load line we require two end points viz. maximum V_{ce} point and maximum I_c point.

Maximum $V_{ce} = V_{CC} = 20$ V. This locates a point *B* on V_{ce} axis.

Maximum $I_c = V_{CC}/R_c + R_e = 20/10$ KΩ $= 2$ mA. This locates point *A* on I_c axis.

A.C. load line. In case of a.c. load line,

$$R_{ac} = \frac{R_C\ R_L}{R_C + R_L} = \frac{10 \times 30}{10 + 30} = 7{\cdot}5\ \text{K}\Omega$$

Now maximum collector emitter voltage

$$= V_{ce} + I_c\ R_{ac} = 10 + 1\ \text{mA} \times 7{\cdot}5\ \text{K}\Omega$$

$$= 10 + 7{\cdot}5 = 17{\cdot}5\ \text{V}$$

This locates a point *D* on V_{ce} axis

Maximum collector current

$$= I_c + \frac{V_{ce}}{R_{ac}} = 1\ \text{mA} + \frac{10\ \text{V}}{7{\cdot}5\ \text{K}\Omega} = 1\ \text{mA} + 1{\cdot}33\ \text{mA}$$

$$= 2{\cdot}33\ \text{mA}$$

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Field Effect Transistors

The field effect transistor is a semiconductor device which depends for its operation on the control of current by electric field.

There are two main types of field effect transistors the junction field effect transistor (JFET) & the metal oxide semiconductor (MOS) field effect transistor (MOSFET)

The advantages of FET over the conventional transistor are:

1. Its operation depends up on the flow of majority carriers only
2. It is immune to radiation
3. It exhibits a high i/p resistance
4. It is less noisy than bipolar jn transistor
5. It exhibits no offset voltage at zero drain current
6. It has thermal stability

Demerit:-
it has relatively small gain-bandwidth product in comparison to transistor

FET
↳ stands for field effect transistor.
It is a three terminal ~~unipolar~~ solid state device. In FET current is controlled by electric field.

Following are standard FET Notation

Source: The source S is the terminal through which the majority carriers enter the bar. Conventional current entering the bar at S is designated by I_S.

Drain:- the drain D is the terminal through which the majority carriers leave the bar. current is denoted as I_D.
V_{DS} is drain to source voltage

Gate:- Heavily doped regions of acceptor impurities have been formed on both sides of ntype bar by alloying, by diffusion or by any other procedure available for creating p-n jn. these impurity regions are called the gate G. The voltage applied betn the gate G & source S in the direction to reverse bias the pn jn is designated as V_{GS}. current is I_G.

Channel:- in ntype material the region betn two gate regions is the channel through which the majority carriers move from source to drain.

classification

FET (field effect transistor)

- Junction FET (JFET)
  - Nchannel
  - pchannel
- METAL OXIDE SEMICONDUCTOR FET (MOSFET / IGFET) or Insulated gate FET
  - DE MOSFET (depletion)
    - Nchannel
    - pchannel
  - E-~~ONLY~~ MOSFET (enhancement)
    - pchannel
    - n channel

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Construction and characteristics of JFET's.

The basic construction of the n-channel JFET is shown in fig.

ohmic contacts, Drain (D), p^+, p^+, n, Gate (G), n channel, depletion region, Source (S)

ntype material forms the channel between the 2 embedded layers of heavily doped ptype material. The top of the ntype channel is connected through an ohmic contact to a terminal referred to as the Drain (D), while the lower end of the same material is connected through an ohmic contact to a terminal referred to as the Source (S).

The two ptype materials are connected together and to the gate (G) terminal.

In the absence of any applied potentials the JFET has 2 p-n junctions under no bias conditions. The result is depletion region at each jn.

Depletion region is that region void of free carriers and ∴ unable to support conduction through the region.

Water analogy provide a sense for the JFET control at the gate terminal.

Source, Gate, Drain

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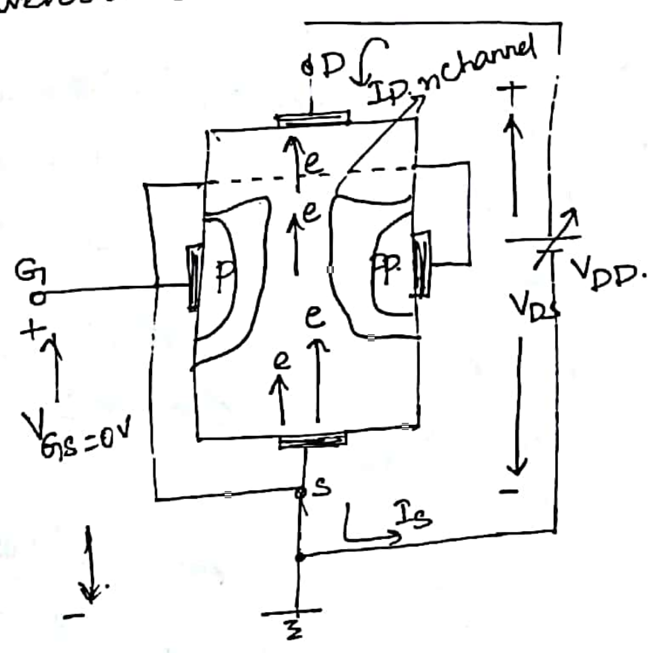
The source of water pressure can be linked to the applied voltage from drain to source that will establish a flow of water (electrons) from the source. The gate through an applied signal controls the flow of water to the drain.

$V_{GS} = 0\,V$, V_{DS} some positive value.

A +ve voltage V_{DS} has been applied across the ~~terminal~~ channel & the gate has been connected directly to source to establish the condition $V_{GS} = 0\,V$. The result is gate & source terminals at the same potential & and a depletion region in the low end of each p-type material similar to the distribution of the no bias conditions of above fig.

The instant V_{DS} is applied, the electrons will be drawn to the drain terminal establishing conventional current I_D with the direction in fig.



The drain & source currents are equal

$$I_D = I_S.$$

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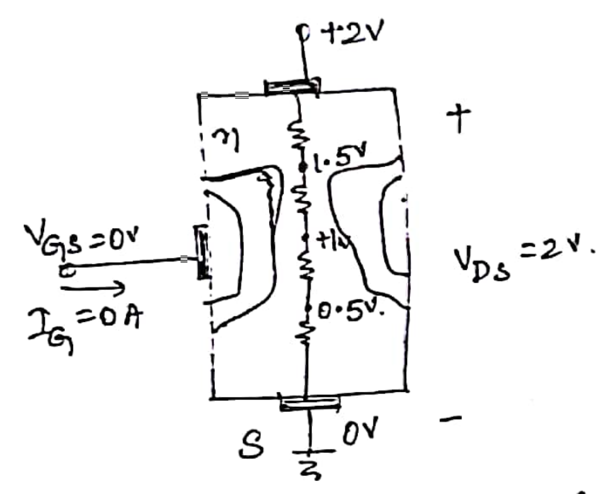
The depletion region is wider near the top of both p-type materials. The reason for this change in widths of the region is best explained as. 3



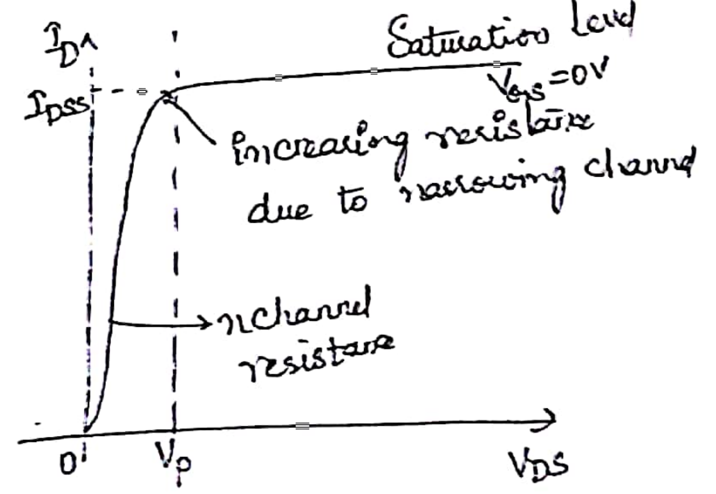
Assume a uniform resistance in the n channel, the resistance of the channel can be broken down to the divisions appearing as in fig.

The Current I_D will establish the Voltage levels through the channel as indicated. The result is that the upper region of the p type material is reverse biased by about 1.5V with the lower region only reverse biased by 0.5V

The fact that the pn jn is RB for the length of the channel results in a gate current of '0' ampers.

i.e $I_G=0A$

As the Voltage V_{DS} is increased from 0 to a few Volts, the current will increase and plot of I_D Vs V_{DS} will appear as.



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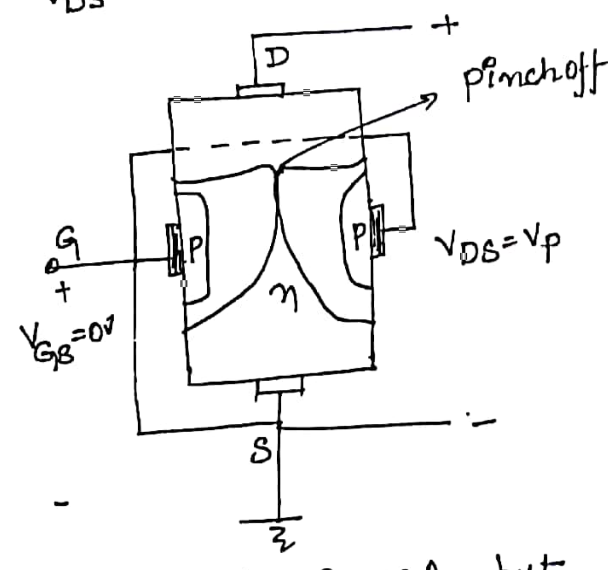
For low values of V_{DS} the resistance i.e essentially constant.
As V_{DS} increases & approaches V_P the depletion regions
will widen which reduce the channel width.
The reduced path of conduction causes the resistance
to increase. & curve fig the
The more horizontal the curve, the higher the resistance
which approaches ∞ in horizontal region.
If V_{DS} is increased to a level where it appears
two depletion regions would "touch" this condition
is referred to as pinch off will result.
'V_{DS}' know called as pinch off voltage → V_P



from the fig $I_D = 0A$ but hardly is this case &
I_D maintains a saturation level defined as I_{DSS}
Even though $V_{DS} > V_P$ the depletion regions will increase
in length along the channel but the level of I_D remains
essentially the same.
∴ When $V_{DS} > V_P$ the characteristics are of
current source.
∴ I_{DSS} = max drain current & is defined by
Conditions $V_{GS} = 0V$ & $V_{DS} > |V_P|$

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2) $V_{GS} < 0V$

4

V_{GS} is the controlling voltage of JFET.
The gate terminal voltage is set at lower & lower potentials levels as compared to source.

The effect of applying -ve bias V_{GS} is to establish depletion regions similar to those obtained with $V_{GS} = 0V$ but at lower levels of V_{DS}.

Saturation level will reach at lower level of V_{DS} or pinch off.

I_D (mA) ohmic region; Saturation region; break down region
I_{DSS} 8, 7, 6, 5, 4, 3, 2, 1
A, B, C
$V_{GS} = 0V$
$V_{GS} = -1V$
$V_{GS} = -2V$
$V_{GS} = -3V$
$V_{GS} = -4V = V_P$
0, 5, 10, 15, 20, 25, V_{DS} (V)
V_B
$4V = V_P$ for $V_{GS} = 0$
locus of pinch off values.

OA: ohmic region : linear characteristic
JFET obeys ohms law.
behaves as resistor
pt A known as knee

AB:- I_D increases with increase of V_{DS} at inverse square law rate up to pt B.
~~B is called pinch off pt~~

BC: pinch off region:- amplifier region
JFET operates as a constant current source.
Here gate channel jn is RB by V_{DS}.

Since $V_{GS} = 0$
$\therefore I_D$ can be given by Schockley's eqn as

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$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2$$

$$= I_{DSS}\left[1-\frac{V_{GS}}{V_{GS(off)}}\right]$$

Break down region:-

If V_{DS} is increased further to pt. C this region is obtained. The Voltage at C is break down Voltage. The Voltage I_D increases enormously because Beyond this Voltage of reverse breakdown Voltage (avalanche)

∴ The increase in V_{DS} makes a JFET to behave first as a resistor (ohmic) then as a constant current source (pinch off region) and finally as a constant Voltage source (break down region)

∴ **Important Conclusions. are for nchannel**

1) the maximum current is defined as I_{DSS} & occurs when $V_{GS}=0V$ and $V_{DS} \geq |V_P|$

2) For V_{GS} less than (more -ve than) the pinch off level the $I_D = 0A$

3) for all V_{GS} betn 0V and V_P, I_D range betn I_{DSS} & 0A.

ohmic region is referred to as Voltage Controlled resistance region. (because resistance can be Varied by varying V_{GS})

$$\therefore r_d = \frac{r_o}{\left(1-\frac{V_{GS}}{V_P}\right)^2}$$

r_o → resistance with $V_{GS}=0V$

In pinch off region FET is used as amplifier.

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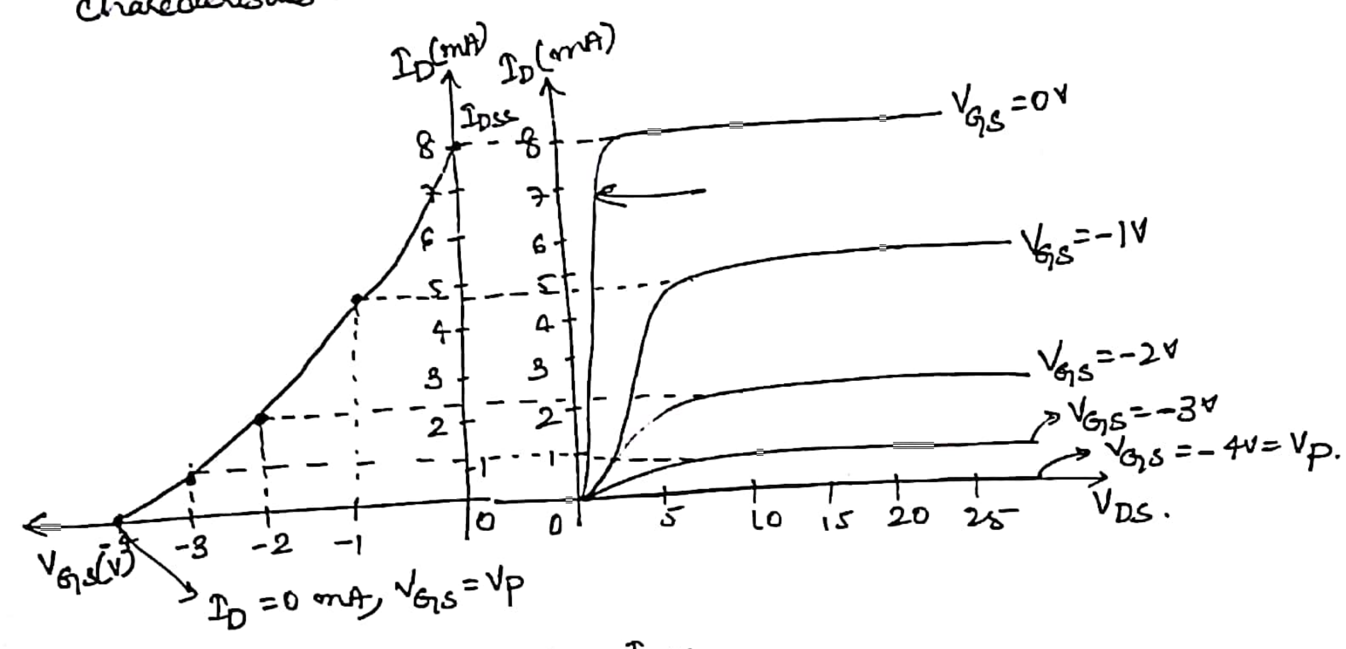
Transfer characteristics

The linear relationship does not exist betⁿ the o/p & i/p quantities of JFET.

∴ The relation betⁿ I_D & V_{GS} is given as

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad \text{--- (1)}$$

The transfer curve can be obtained using drain characteristics as



1) When $V_{GS} = 0V$, $I_D = I_{DSS}$

2) $V_{GS} = V_P$, $I_D = 0$ mA.

The drain characteristics relate o/p quantity to another output quantity where as transfer characteristics are a plot of o/p current Vs an input controlling quantity (V_{GS})

∴ transfer from i/p to o/p variables.

Derivate (1) wrt V_{GS} we get

$$\frac{\partial I_{DS}}{\partial V_{GS}} = \frac{-2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right) \quad \text{--- (2)}$$

Let $g_{m0} = \dfrac{-2I_{DSS}}{V_P}$

→ g_m for $V_{GS} = 0V$

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$\therefore g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)$

from ①

$$\left(1 - \frac{V_{GS}}{V_P}\right) = \sqrt{\frac{I_{DS}}{I_{DSS}}}$$

$\therefore$

$$g_m = g_{mo}\sqrt{\frac{I_{DS}}{I_{DSS}}}$$

$$\text{or } g_m = \frac{-2I_{DSS}}{V_P} \times \sqrt{\frac{I_{DS}}{I_{DSS}}}$$

$$\boxed{g_m = \frac{-2}{V_P}\sqrt{I_{DS}\, I_{DSS}}}$$

eqn ① can also be written as

$$V_{GS} = V_{GS(off)}\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$$

$\hookrightarrow$ voltage at which channel is cutoff.

__FET parameters__

a) __Drain Resistance__ r_d

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\Big|_{V_{GS} = \text{Const}}$$

r_d ranges from $10k\,\Omega$ to $50k\,\Omega$

b) __TransConductance__ g_m

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}\Big|_{V_{DS} = \text{const}}$$

$g_m \rightarrow 2m\mho$ to $6m\mho$

c) __Amplification factor__ μ

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}\Big|_{I_D \text{ const}}$$

$$\boxed{\mu = \frac{\Delta V_{DS}}{\Delta I_D} \cdot \frac{\Delta I_D}{\Delta V_{GS}} = r_d \cdot g_m}$$

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Applications JFET

1) RF Amplifiers, FM tuners
2) used in cascade amplifiers. & test equipment for its low Cin (input capacitance)
3) oscillator ckts for low freq drift
4) FM & TV receivers.
5) digital ckts in Computers because of small size
6) buffer in measuring instrument for its high i/p impedance & low o/p impedance
7) Voltage Variable resistor
8) it has -ve temp coefficient of resistance.

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MOSFET

depletion enhancement

DEPLETION-TYPE MOSFET

The characteristics are similar to those of a JFET between cutoff & saturation at I_{DSS}.

Basic Construction

Basic Construction of n channel depletion type mosfet is shown in fig as

Drain
SiO_2
n channel
Metal Contacts
Gate
n
n
p Substrate
Substrate
n doped regions
Source

A slab of p-type material is formed from a si base and is referred to as substrate. The Source & drain terminals are connected through metallic contacts to n doped regions linked by n channel. The gate is also connected to a metal contact surface but remains insulated from the n channel by a very thin SiO_2 layer. SiO_2 is a type of insulator referred to as a dielectric. ~~that~~ there is no direct electrical connection betn gate terminal & the channel of MOSFET due to SiO_2 layer.

This SiO_2 accounts for the very desirable high i/p impedance of the device.

The name metal oxide semiconductor FET is now because metal for drain, source & gate connections, oxide for SiO_2 insulating layer and semiconductor for basic structure in which n and p type regions are diffused.

The insulating layer betn the gate & channel has resulted in another name for the device. Insulated gate FET is IGFET.

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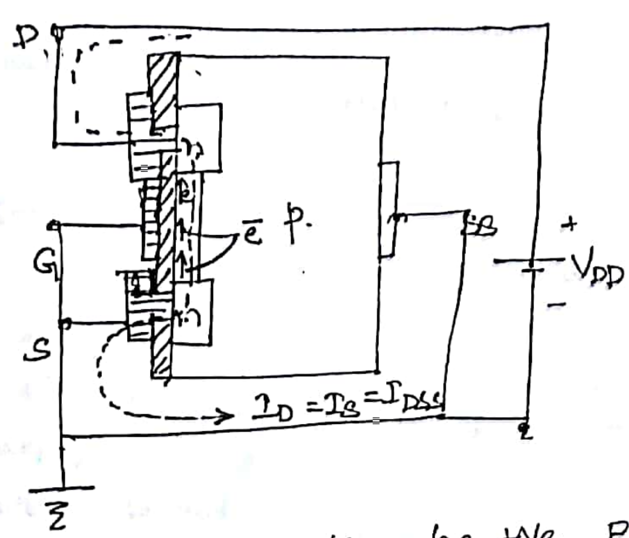
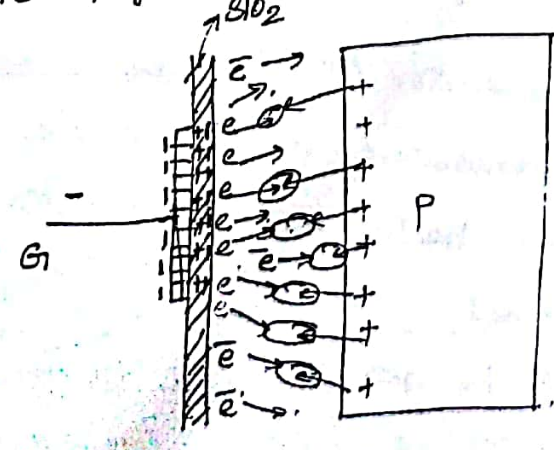
Basic Operation & Characteristics

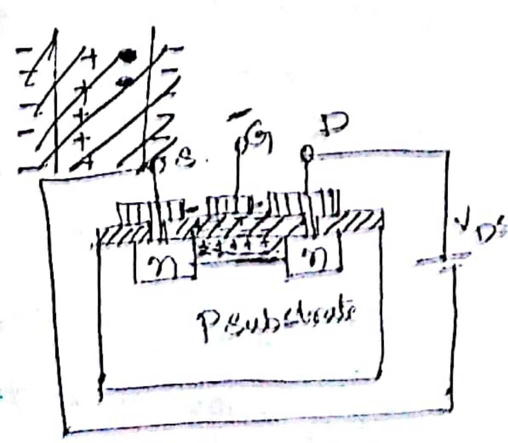
In fig V_{GS} is set to zero volts and a voltage V_{DS} is applied across the drain to source terminals.



The result is an attraction for +ve potential at the drain by free $\bar{e}$ of the n channel and a current similar to the established through the channel of the JFET.

When V_{GS} has been set at a -ve voltage such as -1V. The negative potential at the gate will tend to pressure $\bar{e}$ towards the p type substrate & attract holes from the p type substrate as shown. i.e like charges repel & unlike charges attract





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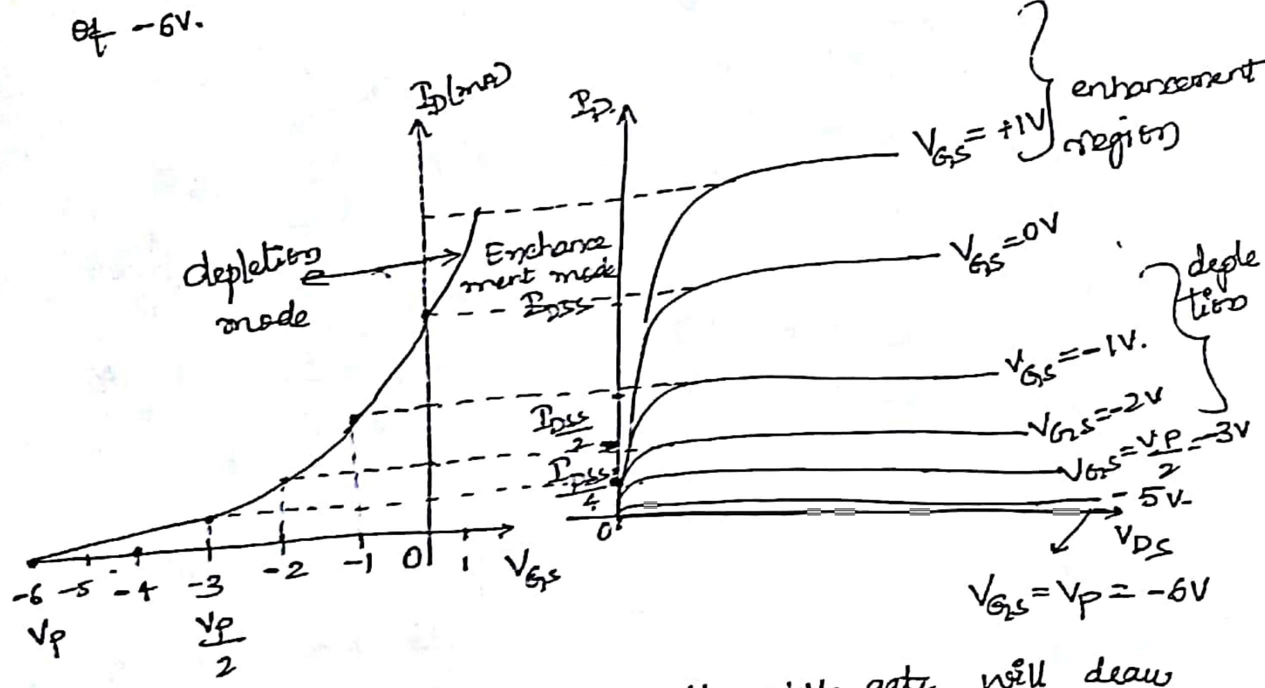
Depending on the magnitude of the -ve established by V_{GS} a level of recombination betn $\bar{e}$ & holes will occurs that & will reduce the number of free $\bar{e}$ and in the nchannel available for conduction. The more -ve the bias, the higher the rate of recombination. the resulting drain current is ∴ reduced with increasing -ve bias for V_{GS} for -1, -2V and so on to the pinch off level of -6V.



The positive value of V_{GS}, the +ve gate will draw additional electrons and establish new carriers through the collisions resulting.

As the gate to source voltage continues to increase in the +ve direction the I_D increases rapidly.

The application of +ve gate to source voltage has "enhanced" the level of free carriers in the channel compared to that encountered with V_{GS}=0V.

∴ the region of +ve gate voltage on the drain or transfer characteristics is often referred to as the

enhancement region..

The Shockley's equation is applicable for the depletion type MOSFET in both depletion & enhancement regions.

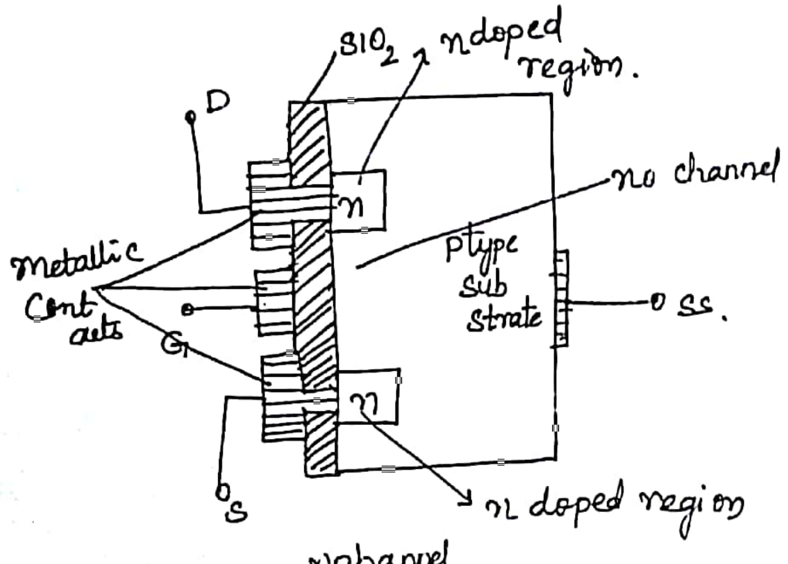
ENHANCEMENT-TYPE MOSFET

The characteristics of enhancement-type MOSFET are quite different from others.

1. The transfer curve is not defined by Shockley's eqn
2. I_D is now cutoff until the gate to source voltage reaches a specific magnitude.
3. Current control in an n-channel device is now effected by +ve gate to source voltage

Construction

A slab of p-type material is formed from a Si base and is referred to as substrate



n-channel

The source & drain terminals are connected through metallic contacts to n doped regions but their is absence of channel betn the two n-doped regions.

This is primary diff betn ~~primary~~ depletion & enhancement type MOSFET's.

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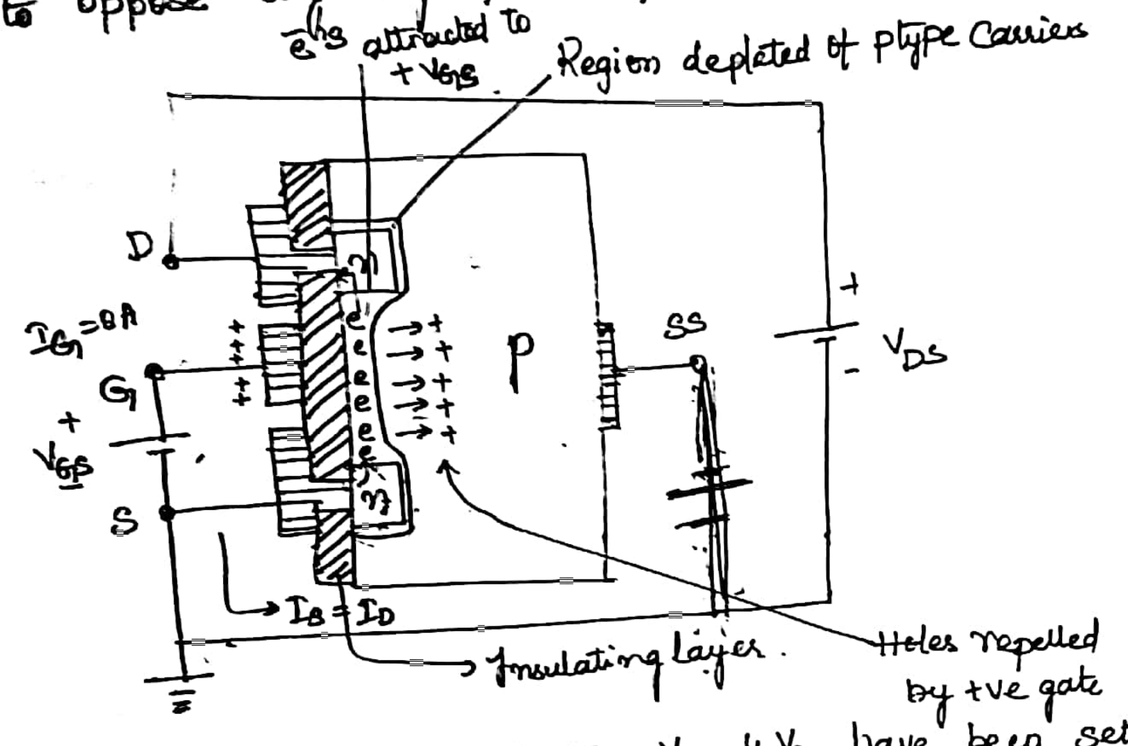
Operation & Characteristics

If $V_{GS} = 0V$ and a voltage is applied betn drain & source. Because of absence of an n channel the current of effectively zero amps (but in depletion MOSFET & JFET current $I_D = I_{DSS}$).

With V_{DS} some +ve voltage, $V_{GS} = 0V$, there are 2 reverse biased pn junctions betn n doped regions & the p substrate to oppose any significant flow betn drain & source.



In the above fig both V_{DS} & V_{GS} have been set at some +ve voltages greater than 0V, establishing drain & gate at a +ve potential wrt the source.

The +ve potential at the gate will pressure the holes in the p substrate along the edge of SiO_2 layer to leave the area and enter deeper regions of the p substrate.

The result is a depletion region near the SiO_2 insulating layer void of holes. But the e's in the p substrate will be attracted to the +ve gate & accumulate in the region near the surface of SiO_2 layer. The SiO_2 layer & its insulating qualities will prevent the -ve carriers form being

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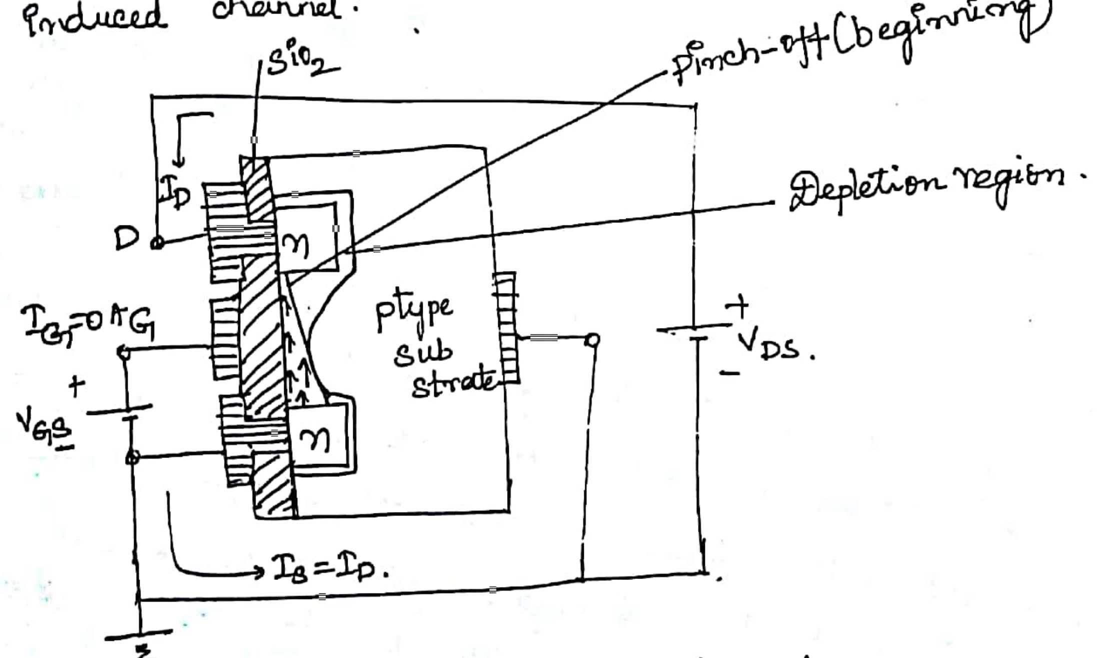
absorbed at the gate terminal.

As V_{GS} increases in magnitude, the concentration of $\bar{e}$'s near the SiO_2 surface increases until the induced ntype region can support a measurable flow b/n drain & source. The level of V_{GS} that results in the significant increase in drain current is called the threshold voltage (V_T)

Since the channel is not existence with $V_{GS}=0V$ and enhanced by the application of +ve V_{GS} this type of MOSFET is called enhancement Type MOSFET.

As $V_{GS} > V_T$ the density of free carriers in the induced channel will increase, resulting in increased level of I_D. if V_{GS} = const & ↑ the level of V_{DS} the I_D will eventually reach a saturation level. as The leveling off of I_D is due to pinching-off process. depicted by the narrower channel at the drain end of the induced channel.



Applying Kirchhoff's Voltage law to the terminal Voltages of the MOSFET we find that

$$V_{DG} = V_{DS} - V_{GS} \quad \text{---} (1)$$

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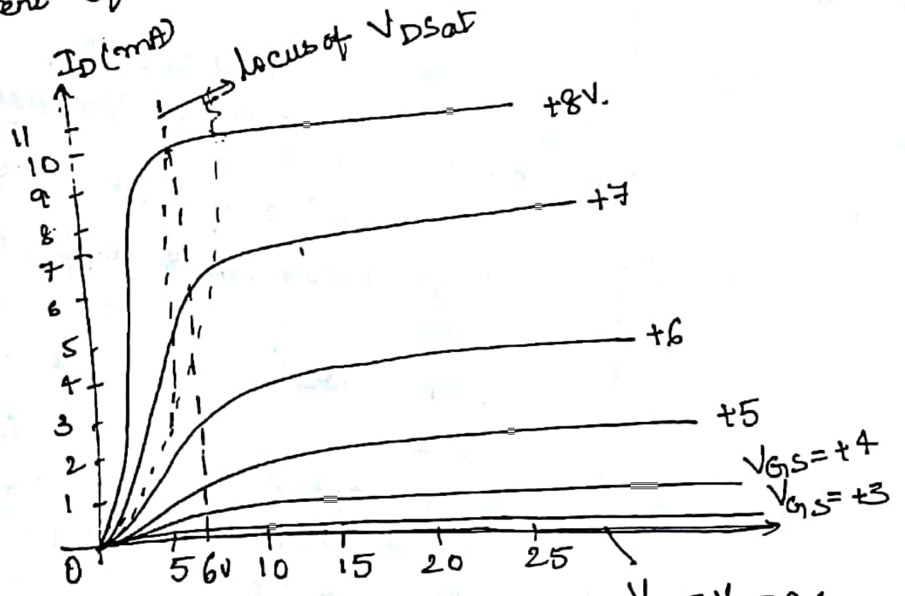
If V_{GS} = is fixed for 8V and V_{DS} is increased from 2 to 5V the Voltage V_{DG} = −6 to −3V.

∴ the gate will become less and less +ve w.r.t drain. this reduction in gate to drain voltage will in turn reduce the attractive forces for free carriers (electrons) in this region of the induced channel, causing a reduction in the effective channel width.

Eventually the channel will be reduced to the pt of pinch off & a saturation condition will be established. The saturation level for V_{DS} is related to the level of applied V_{GS} by

$$\boxed{V_{DS_{sat}} = V_{GS} - V_T}$$

For values of V_{GS} less than the threshold level, the drain current of an enhancement-type MOSFET is 0mA.



For levels of $V_{GS} > V_T$ the I_D is related to the applied gate to source voltage as

$$\boxed{I_D = K(V_{GS} - V_T)^2}$$

'K' is a Const that is a f^n of the construction of the device.

$$K = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

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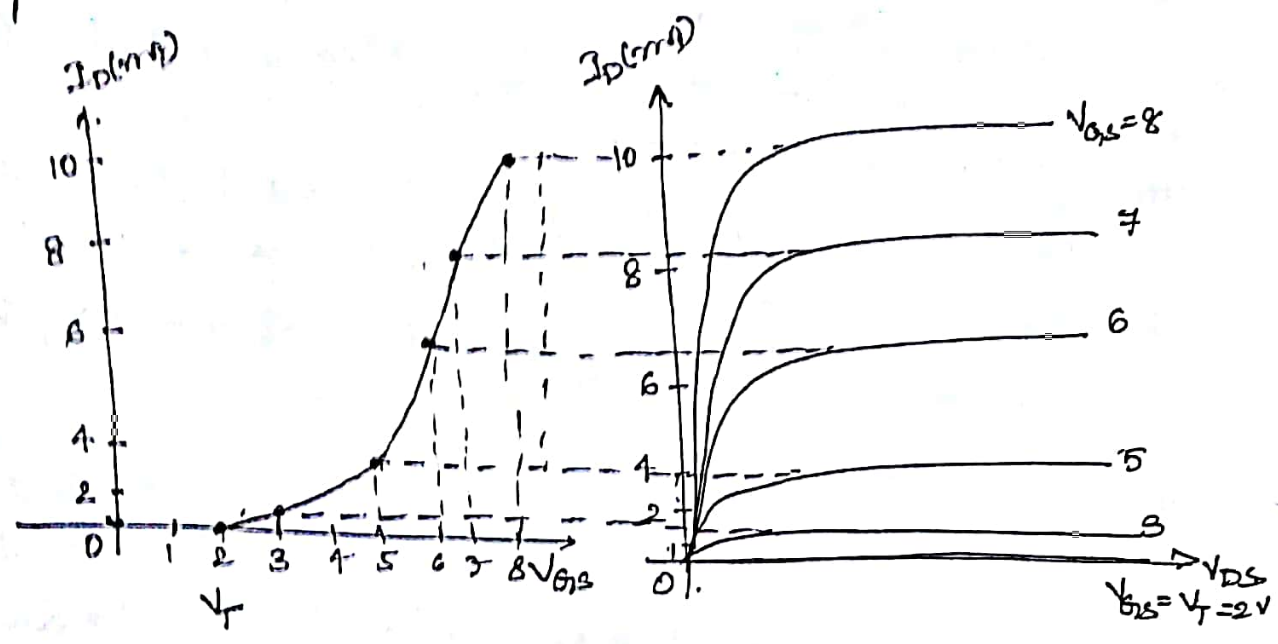
$I_D = 0mA$ for $V_{GS} \leq V_T$. Transfer characteristics for n channel device, it is now totally in the +ve V_{GS} region & does not rise until $V_{GS} = V_T$



Comparison Between JFET and MOSFET

JFET	MOSFET
1. The gate is not insulated from the channel	1. The gate is insulated from the channel by a layer of insulating oxide (SiO_2)
2. There are two types: P-type and N-type channel	2. There are 4 types: ptype enhancement MOSFET, Ntype " ", ptype depletion ", N type " MOSFET
3. Operated only in depletion mode.	3. Can be operated in depletion as well as enhancement mode.
4. There is a continuous channel	4. There is continous channel only in depletion type, but not in enhancement type.
5. Higher i/p impedance. >10MΩ	5. Very high i/p impedance >10,000MΩ
6. Drain resistance is higher. r_d = 100K to 1MΩ	6. Drain resistance lower r_d = 1K to 50KΩ.

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Design of biasing for JFET

* FET - Field Effect Transistor - It's a semiconductor device which depends for its operation on the control of current by an electric field.

FET

- Junction field Effect Transistor (or) FET
- Metal - oxide - semiconductor Transistor (MOSFET)

FET differs from the BJT in the following characteristics

1. It's operation depends upon the flow of majority carriers only.
2. It's simpler to fabricate & occupies less space.
3. It exhibits a high input resistance, typically many megaohms.
4. It's less noisy compared to BJT.
5. It exhibits no offset voltage at zero drain current

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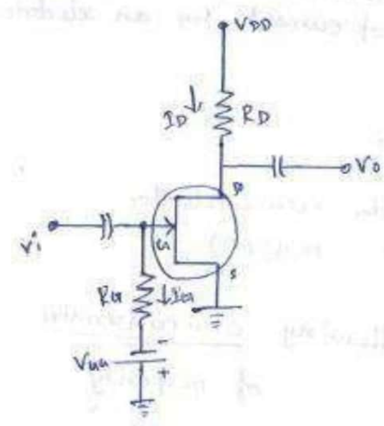
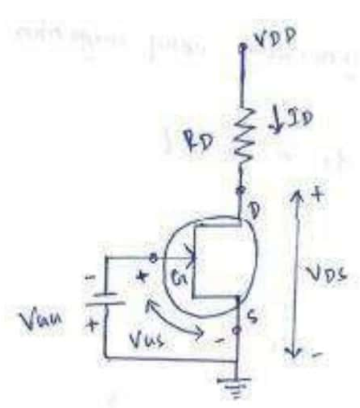
1. Fixed Bias | Gate Bias



* To make the gate-source junction reverse biased a separate supply V_{GG} is connected such that gate is more negative than the source.

Dc Analysis:

* For dc analysis coupling capacitors are open circuited.
* The current through R_G is I_G which is 0.
* This permits R_G to replace by short circuit equivalent, simplifying the fixed bias circuit.



* We know for dc analysis

$$I_G = 0 \text{ amps}$$

* Apply KVL to the Gate to source junction

$$V_{GS} + V_{GG} = 0$$

$$\therefore V_{GS} = -V_{GG}$$

* Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude & hence the name fixed bias circuit

* For fixed bias circuit the I_D can be calculated as

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

* Apply KVL to the Drain to Source junction

$$V_{DS} + I_D R_D - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D$$

Q-Point

$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$V_{DSQ} = V_{DD} - I_{DQ} R_D$$

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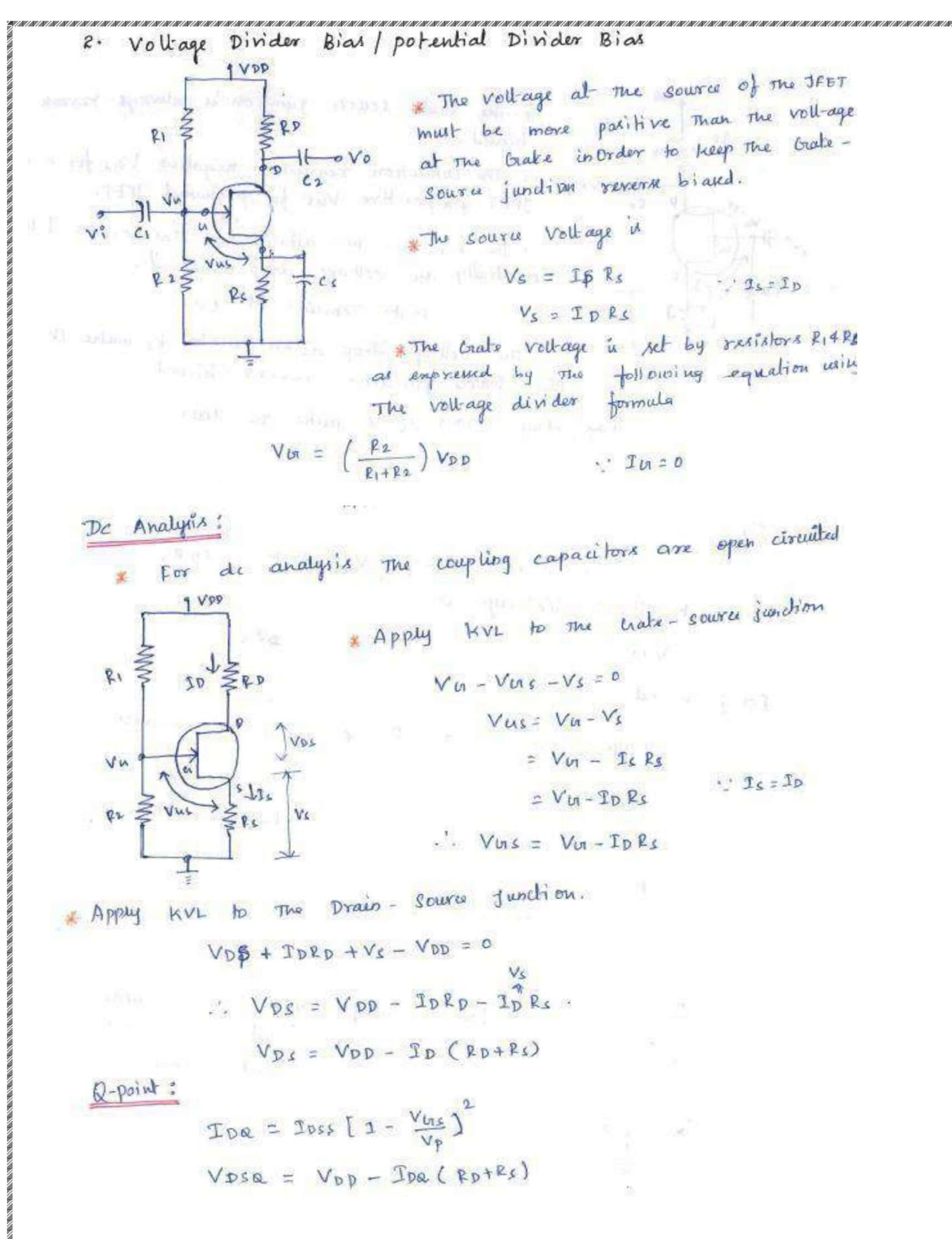

2. Voltage Divider Bias / potential Divider Bias

* The voltage at the source of the JFET must be more positive than the voltage at the Gate in order to keep the Gate-Source junction reverse biased.

* The source voltage is

$$V_S = I_S R_S \qquad \because I_S = I_D$$

$$V_S = I_D R_S$$

* The Gate voltage is set by resistors R_1 & R_2 as expressed by the following equation using the voltage divider formula

$$V_G = \left(\frac{R_2}{R_1+R_2}\right) V_{DD} \qquad \because I_G = 0$$

Dc Analysis :

* For dc analysis the coupling capacitors are open circuited

* Apply KVL to the Gate-source junction

$$V_G - V_{GS} - V_S = 0$$

$$V_{GS} = V_G - V_S$$

$$= V_G - I_S R_S \qquad \because I_S = I_D$$

$$= V_G - I_D R_S$$

$$\therefore V_{GS} = V_G - I_D R_S$$

* Apply KVL to the Drain-Source junction.

$$V_{DS} + I_D R_D + V_S - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D - \underbrace{I_D R_S}_{V_S}$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

Q-point :

$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$V_{DSQ} = V_{DD} - I_{DQ}(R_D + R_S)$$

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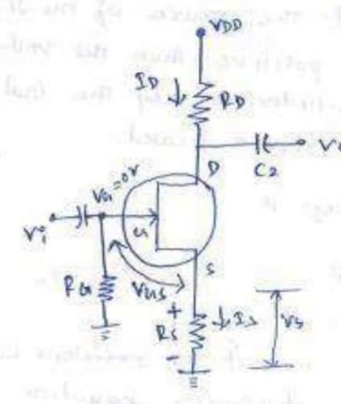
3. Self Bias



* The Gate-source junction is always reverse biased.
* The condition requires negative V_{GS} for n-channel JFET & positive V_{GS} for p-channel JFET.
* The R_G does not affect the bias because it has essentially no voltage drop across it.
* ∴ The Gate remains at 0V.
* The voltage drop across resistor R_S make the Gate-Source junction reverse biased.

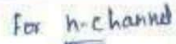
* I_S produces voltage drop across R_S & make the source positive w.r.to ground.

Since

$$I_S = I_D \quad \& \quad V_G = 0 \quad \text{Then} \quad V_S = I_S R_S = I_D R_S$$

* The Gate-Source Voltage is

$$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$$



For p channel:

* The voltage drop across R_S & make the source negative w.r.t ground.

Since

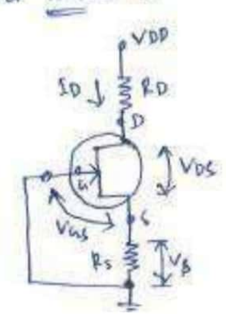
$$I_S = I_D \quad \& \quad V_G = 0 \quad \text{then} \quad V_S = -I_S R_S = -I_D R_S$$

* The Gate-Source Voltage is

$$V_{GS} = V_G - V_S = 0 - (-I_D R_S) = I_D R_S$$

DC Analysis:

For n-channel



For dc analysis the coupling capacitors are replaced by open circuit & R_G is replaced by short circuit equivalent, since $I_G = 0$.

W.K.T

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad —①$$

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Substitute the value of V_{GS} in eqn ①

$$① \Rightarrow I_D = I_{DSS}\left(1 - \frac{(-I_D R_S)}{V_P}\right)^2 \rightarrow \text{for n-channel}$$

$$= I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

Apply KVL to the Drain to source junction

$$V_S + V_{DS} + I_D R_D - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - V_S - I_D R_D$$

$$= V_{DD} - I_D R_S - I_D R_D$$

$$\therefore V_{DS} = V_{DD} - I_D(R_S + R_D)$$

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FET Small Signal model

A ckt which satisfies eqn $i_d = g_m v_{gs} + \frac{1}{r_d} v_{ds}$ is indicated in fig.

The low freq small signal model has a Norton's output ckt with a dependent current generator whose current is proportional to gate to source voltage.

The proportionality factor is the transconductance g_m, which is consistent with the definition of g_m in

$$g_m = \frac{i_d}{V_{gs}}\Big|_{V_{DS}}$$

The output resistance is r_d, which is consistent with the definition in

$$r_d = \frac{V_{ds}}{i_d}\Big|_{V_{GS}}$$

The i/p resistance between gate and source is infinite since it is assumed that the reverse biased gate takes no current.

The FET model of fig should be compared with the h-parameter model of the bipolar jn transistor, but the latter also has a Norton's output circuit. Whereas in the current generated depends upon the i/p current whereas in the FET model the generator current depends upon the i/p voltage.

There is no feedback at low frequencies from output to input in the FET, whereas such feedback exists in the bipolar transistor through the parameter h_{re}.

The high i/p resistance is replaced by 1KΩ resistor in CE amplifier.

The FET is much more ideal amplifier than the conventional transistor at low frequencies.

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The high freq model is given in fig. This is similar

except that the capacitances between pairs of nodes have been added. The capacitor C_{gs} represents the barrier capacitance between gate and source and C_{gd} is the barrier capacitance between gate and drain.

Because of these internal capacitances, feedback exists between the i/p and o/p ckts and voltage amplification drops rapidly as the freq is increased.

VVR (Voltage variable resistor)

→ It can be used to vary the voltage gain of a multistage amplifier. This act^n is referred as automatic gain control (AGC)

JFET is operated in constant current portion of its o/p charac. i.e., in saturat^n region. FET can also be used in the region before pinch-off where V_{DS} is small. Here it works as variable ~~res~~ resistance device i.e., the channel resistance is controlled by the gate bias voltage V_{GS}. In such an appl^n the FET is referred to as voltage variable resistor (VVR) or voltage dependent resistor (VDR).

The VVR can be used to vary the voltage gain of a multistage amplifier. This action is referred as automatic gain control (AGC). If the signal is low then voltage gain of the stages can be increased and when becomes high, the gain can be reduced automatically. In this way, the general level of amplificat^n is maintained fairly constant.

Q

1) FET opert?
2) Write about MOSFET.

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