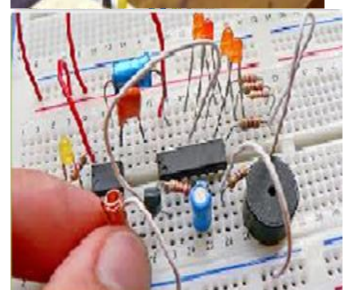
SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

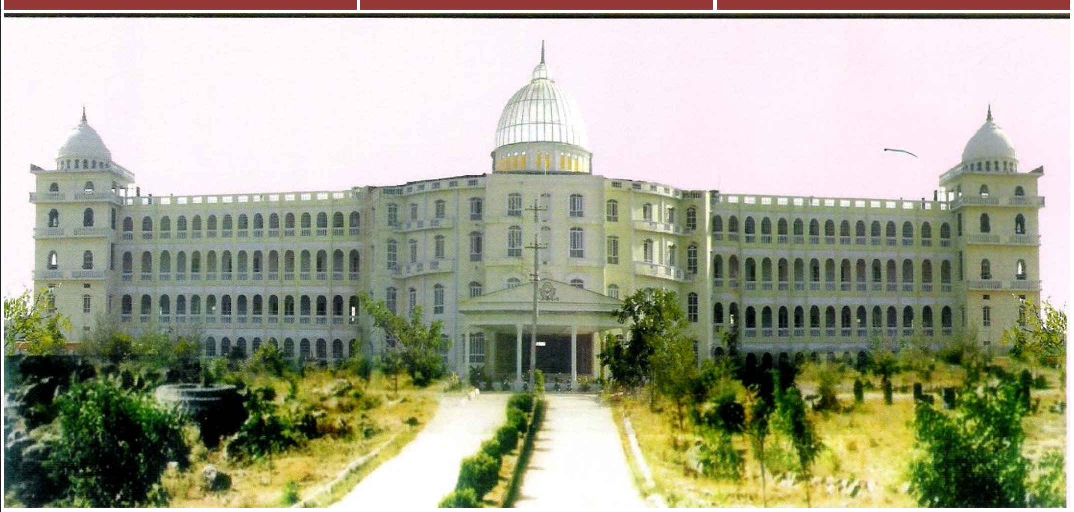
ANALOG ELECTRONICS LAB (R20ECE21L4)



Prepared By

P.PRASHANT Assoc.Prof

CSE	AE LAB	II Year	I Sem



SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY
(an Autonomous Institution under JNTUH)

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

B. TECH –ELECTRONICS & COMMUNICATION ENGINEERING

INSTITUTION VISION

To be a premier Institution in Engineering & Technology and Management with competency, values and social consciousness.

INSTITUTION MISSION

IM_1 Provide high quality academic programs, training activities and research facilities.

IM_2 Promote Continuous Industry-Institute interaction for employability, Entrepreneurship, leadership and research aptitude among stakeholders.

IM_3 Contribute to the economical and technological development of the region, state and nation.

DEPARTMENT VISION

To be a technologically adaptive centre for computing by grooming the students as top notch professionals.

DEPARTMENT MISSION

DM_1 To offer quality education in computing.

DM_2 To provide an environment that enables overall development of all the stakeholders.

DM_3 To impart training on emerging technology like Data Analytics, Artificial Intelligence and Internet Of Things.

DM_4 To encourage participation of stakeholders in research and development.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO 1: **Higher Degrees & Professional Employment:** Graduates with ability to pursue career in core industries or higher studies in reputed institution.

PEO 2: **Domain Knowledge:** Graduates with ability to apply professional knowledge/skills to design and develop product or process.

PEO 3: **Engineering Career:** Graduates with excellence in Electronics and Communication Engineering along with effective inter-personnel skills.

PEO 4: **Lifelong Learning:** Graduates equipped with skills in recent technologies and be receptive to attain professional competence through life-long learning.

PROGRAM OUTCOMES (POs) & PROGRAM SPECIFIC OUTCOMES (PSOs)

PO	Description
PO 1	**Engineering Knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO 2	**Problem Analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO 3	**Design / development of Solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO 4	**Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO 5	**Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO 6	**The engineer and Society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO 7	**Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO 8	**Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice
PO 9	**Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO 10	**Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO 11	**Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one’s own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO 12	**Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological Change
Program Specific Outcomes	
PSO 1	**Basic Electronic and communications knowledge:** Apply basic knowledge related to electronic circuits, VLSI, communication systems, signal processing and embedded systems to solve engineering/societal problems.
PSO 2	**Design Methods:** Design, verify and authenticate electronic functional elements for different applications, with skills to interpret and communicate results.
PSO 3	**Experimentation & Communications:** Engineering and management concepts are used to analyze specifications and prototype electronic experiments/projects either independently or in teams.

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY
(An Autonomous Institution under UGC, New Delhi)

B.Tech. - II Year – I Semester

L	T	P	C
0	0	3	1.5

(R20ECE21L4) Analog Electronics Lab

PART A: (Only for Viva-voice Examination)

Electronic Workshop Practice (In 3 Lab Sessions):

1. Identification, Specifications, Testing of R, L, C Components (Color Codes), Potentiometers, Switches (SPDT, DPDT, and DIP), Coils, Gang Condensers, Relays, Bread Boards, PCB's
2. Identification, Specifications and Testing of Active Devices, Diodes, BJT's, Low power JFET's, MOSFET's, Power Transistors, LED's, LCD's, SCR, UJT.
3. Study and operation of
   i) Multimeters (Analog and Digital)
   ii) Function Generator
   iii) Regulated Power Supplies
   iv) CRO.

PART B: (For Laboratory Examination – Minimum of 10 experiments)

1. Forward & Reverse Bias Characteristics of PN Junction Diode.
2. Zener diode characteristics and Zener as voltage Regulator.
3. Half Wave Rectifier with & without filters.
4. Full Wave Rectifier with & without filters.
5. Input & Output Characteristics of Transistor in CB Configuration and h-parameter calculations.
6. Input & Output Characteristics of Transistor in CE Configuration and h-parameter calculations.
7. FET characteristics.
8. Design of Self-bias circuit.
9. Frequency Response of CC Amplifier.
10. Frequency Response of CE Amplifier.
11. Frequency Response of Common Source FET amplifier .
12. SCR characteristics.
13. UJT Characteristics

PART C: Equipment required for Laboratories:

1. Regulated Power supplies (RPS) -0-30 V
2. CRO's -0-20 MHz.
3. Function Generators -0-1 MHz.
4. Multimeters
5. Decade Resistance Boxes/Rheostats
6. Decade Capacitance Boxes
7. Ammeters (Analog or Digital) -0-20 µA, 0-50µA, 0-100µA, 0-200µA, 0-10 mA.
8. Voltmeters (Analog or Digital) -0-50V, 0-100V, 0-250V
9. Electronic Components -Resistors, Capacitors, BJTs, LCDs, SCRs, UJTs, FETs, LEDs, MOSFETs, Diodes- Ge& Si type, Transistors – NPN, PNP type)

Course outcomes:

Upon completion of the Course, students will be able to:

C216.1 Determine the P-N-Junction diode & Zener diode characteristics (K3-Apply).
C216.2 Calculate the Input and Output characteristics of BJT and FET (K3-Apply).
C216.3 Evaluate Half Wave and Full Wave Rectifier with and without filters (K5-Evaluate).
C216.4 Differentiate Measurement of h-parameters of transistor in CB, CE, CC configurations (K2-Understand).
C216.5 Analyse the Frequency response of CE, CC and Common Source FET Amplifier (K4-Analyse).
C216.6 Measure SCR and UJT characteristics (K5-Evaluate).

Course Articulation Matrix:

Course Outcome	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C216.1	3	3	-	-	2	-	-	-	2	-	-	2	3	-	3
C216.2	3	3	-	-	2	-	-	-	2	-	-	2	3	-	3
C216.3	3	3	2	-	2	-	-	-	2	-	-	2	3	-	3
C216.4	3	3	2	-	2	-	-	-	2	-	-	2	3	-	3
C216.5	3	3	2	-	2.5	-	-	-	-	-	-	2	3	-	3
C216.6	3	3	2	-	2.5	-	-	-	-	-	-	2	3	-	3
C216	**3**	**3**	**2**	**-**	**2.1**	**-**	**-**	**-**	**2**	**-**	**-**	**2**	**3**	**-**	**3**

ANALOG ELECTRONICS LAB

<u>List of Experiments:</u>

1). Forward & Reverse Bias Characteristics of PN Junction Diode.

2). Zener Diode characteristics and Zener as voltage Regulator.

3). Input and Output characteristics of Transistor in CB configuration.

4). Input and Output characteristics of Transistor in CE configuration.

5). Half Wave Rectifier with and without filters.

6). Full Wave Rectifier with and without filters.

7). FET characteristics.

8). Measurement of h-parameters of transistor in CB, CE, CC configurations.

9). Frequency response of CE Amplifier.

10). Frequency response of CC Amplifier.

11). Frequency response of Common Source FET Amplifier.

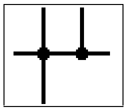
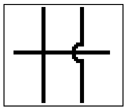
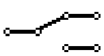
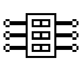
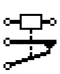
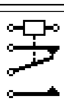
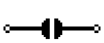
12). SCR characteristics.

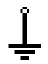
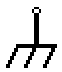
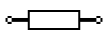
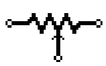
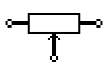
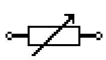
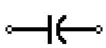
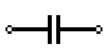
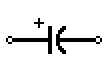
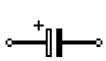
13). UJT characteristics.

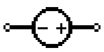
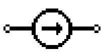
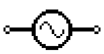
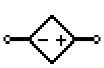
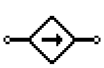
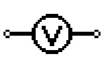
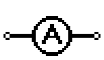
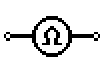
Electrical and Electronic Symbols

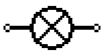
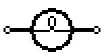
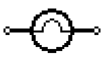
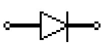
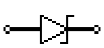
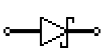
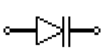
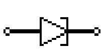
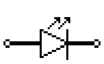
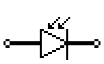
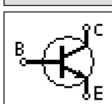
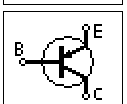
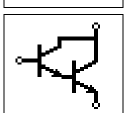
Electrical symbols and electronic circuit symbols are used for drawing schematic diagram. The symbols represent electrical and electronic components.

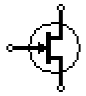
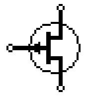
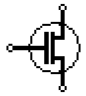
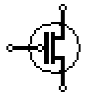
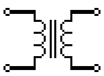
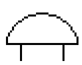
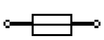
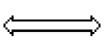
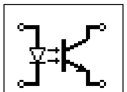
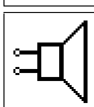
Table of Electrical and Electronic Symbols:

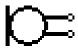
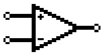
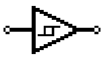
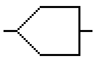
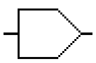
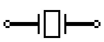
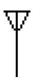
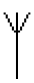
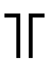
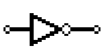
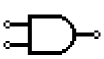
Symbol	Component name	Meaning
Wire Symbols		
	Electrical Wire	Conductor of electrical current
	Connected Wires	Connected crossing
	Not connected Wires	Wires are not connected
Switch Symbols and Relay Symbols		
	SPST Toggle Switch	Disconnects current when open
	SPDT Toggle Switch	Selects between two connections
	Pushbutton Switch (N.O)	Momentary switch - normally open
	Pushbutton Switch (N.C)	Momentary switch - normally closed
	DIP Switch	DIP switch is used for onboard configuration
	SPST Relay	Relay open / close connection by an electromagnet
	SPDT Relay	
	Jumper	Close connection by jumper insertion on pins.
	Solder Bridge	Solder to close connection

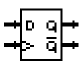
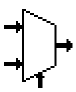
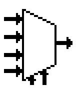
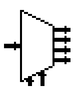
Ground Symbols		
	Earth Ground	Used for zero potential reference and electrical shock protection.
	Chassis Ground	Connected to the chassis of the circuit
	Digital / Common Ground	
Resistor Symbols		
	Resistor (IEEE)	Resistor reduces the current flow.
	Resistor (IEC)	
	Potentiometer (IEEE)	Adjustable resistor - has 3 terminals.
	Potentiometer (IEC)	
	Variable Resistor / Rheostat(IEEE)	Adjustable resistor - has 2 terminals.
	Variable Resistor / Rheostat(IEC)	
Capacitor Symbols		
	Capacitor	Capacitor is used to store electric charge. It acts as short circuit with AC and open circuit with DC.
	Capacitor	
	Polarized Capacitor	Electrolytic capacitor
	Polarized Capacitor	Electrolytic capacitor
	Variable Capacitor	Adjustable capacitance

Inductor / Coil Symbols		
	Inductor	Coil / solenoid that generates magnetic field
	Iron Core Inductor	Includes iron
	Variable Inductor	
Power Supply Symbols		
	Voltage Source	Generates constant voltage
	Current Source	Generates constant current.
	AC Voltage Source	AC voltage source
	Generator	Electrical voltage is generated by mechanical rotation of the generator
	Battery Cell	Generates constant voltage
	Battery	Generates constant voltage
	Controlled Voltage Source	Generates voltage as a function of voltage or current of other circuit element.
	Controlled Current Source	Generates current as a function of voltage or current of other circuit element.
Meter Symbols		
	Voltmeter	Measures voltage. Has very high resistance. Connected in parallel.
	Ammeter	Measures electric current. Has near zero resistance. Connected serially.
	Ohmmeter	Measures resistance

	Wattmeter	Measures electric power
Lamp / Light Bulb Symbols		
	Lamp / light bulb	Generates light when current flows through
	Lamp / light bulb	
	Lamp / light bulb	
Diode / LED Symbols		
	Diode	Diode allows current flow in one direction only (left to right).
	Zener Diode	Allows current flow in one direction, but also can flow in the reverse direction when above breakdown voltage
	Schottky Diode	Schottky diode is a diode with low voltage drop
	Varactor / Varicap Diode	Variable capacitance diode
	Tunnel Diode	
	Light Emitting Diode (LED)	LED emits light when current flows through
	Photodiode	Photodiode allows current flow when exposed to light
Transistor Symbols		
	NPN Bipolar Transistor	Allows current flow when high potential at base (middle)
	PNP Bipolar Transistor	Allows current flow when low potential at base (middle)
	Darlington Transistor	Made from 2 bipolar transistors. Has total gain of the product of each gain.

	JFET-N Transistor	N-channel field effect transistor
	JFET-P Transistor	P-channel field effect transistor
	NMOS Transistor	N-channel MOSFET transistor
	PMOS Transistor	P-channel MOSFET transistor
Misc. Symbols		
	Motor	Electric motor
	Transformer	Change AC voltage from high to low or low to high.
	Electric bell	Rings when activated
	Buzzer	Produce buzzing sound
	Fuse	The fuse disconnects when current above threshold. Used to protect circuit from high currents.
	Fuse	
	Bus	Contains several wires. Usually for data / address.
	Bus	
	Bus	
	Optocoupler / Opto-isolator	Optocoupler isolates onnection to other board
	Loudspeaker	Converts electrical signal to sound waves

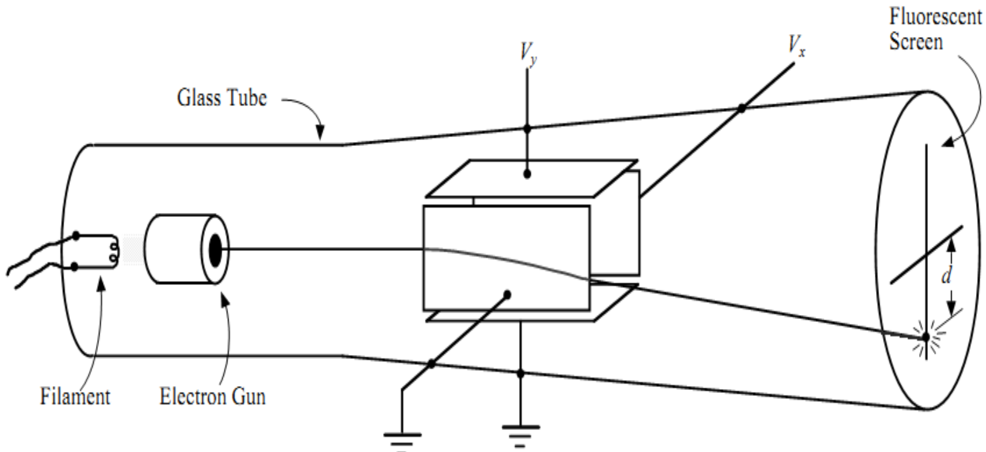
	Microphone	Converts sound waves to electrical signal
	Operational Amplifier	Amplify input signal
	Schmitt Trigger	Operates with hysteresis to reduce noise.
	Analog-to-digital converter (ADC)	Converts analog signal to digital numbers
	Digital-to-Analog converter (DAC)	Converts digital numbers to analog signal
	Crystal Oscillator	Used to generate precise frequency clock signal
Antenna Symbols		
	Antenna / aerial	Transmits & receives radio waves
	Antenna / aerial	
	Dipole Antenna	Two wires simple antenna
Logic Gates Symbols		
	NOT Gate (Inverter)	Outputs 1 when input is 0
	AND Gate	Outputs 1 when both inputs are 1.
	NAND Gate	Outputs 0 when both inputs are 1. (NOT + AND)
	OR Gate	Outputs 1 when any input is 1.

	NOR Gate	Outputs 0 when any input is 1. (NOT + OR)
	XOR Gate	Outputs 1 when inputs are different. (Exclusive OR)
	D Flip-Flop	Stores one bit of data
	Multiplexer / Mux 2 to 1	Connects the output to selected input line.
	Multiplexer / Mux 4 to 1	
	Demultiplexer / Demux 1 to 4	Connects selected output to the input line.

THE OSCILLOSCOPE

Introduction

The oscilloscope is a universal measuring instrument with applications in physics, biology, chemistry, medicine, and many other scientific and technological areas. It is used to give a visual representation of electrical voltages. Thus, any quantity which can be converted to a voltage can be displayed on an oscilloscope. Although the oscilloscope looks very complicated, once you familiarize yourself with its controls and functions, it is surprisingly easy to use. The purpose of this experiment is to develop familiarity with the oscilloscope and with the types of measurements that can be made with it.



How the Oscilloscope Works

The most important component of the oscilloscope is the cathode ray tube (CRT), a vacuum tube in which a filament is heated to "boil off" electrons which are then focused into a beam and "shot" toward the screen with an electron gun. In the photograph above, screen is the rectangular, gridded area on the left of the oscilloscope.

The screen is coated with fluorescent material which glows when it is hit by the electron beam. On its way to the screen, the beam passes between two sets of deflection plates (horizontal and vertical) and a voltage applied to these plates will cause the beam to curve. The sketch illustrates the CRT components with a negative voltage applied only to the vertical plates (Vy), causing the beam to bend downward. The amount of deflection d shown on the screen is proportional to the voltage applied to the plates, so you can measure a voltage by seeing where the beam hits the screen.

BREADBOARD

A **breadboard** is a construction base for prototyping of electronics. The term is commonly used to refer to **solderless breadboard**. Because the **solderless breadboard** does not require soldering, it is reusable. This makes it easy to use for creating temporary prototypes and experimenting with circuit design. Older breadboard types did not have this property. A **stripboard** (veroboard) and similar prototyping printed, which are used to build permanent soldered prototypes or one-offs, cannot easily be reused. A variety of electronic systems may be prototyped by using breadboards, from small analog and digital circuits to complete central processing units (CPUs).

Bus and terminal strips

Solderless breadboards are available from several different manufacturers, but most share a similar layout. The layout of a typical solderless breadboard is made up from two types of areas, called strips. Strips consist of interconnected electrical terminals.

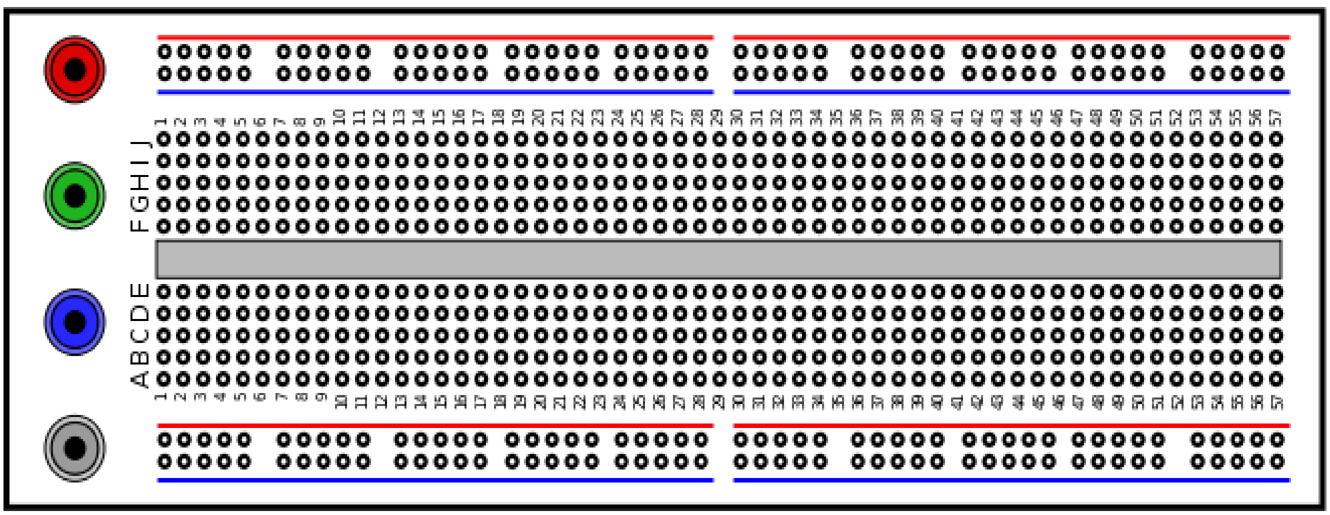
Bus strips:

Usually Bus strips to provide power to the electronic components. A bus strip usually contains two columns: one for ground and one for a supply voltage. However, some breadboards only provide a single-column power distributions bus strip on each long side. Typically the column intended for a supply voltage is marked in red, while the column for ground is marked in blue or black. Some manufacturers connect all terminals in a column. Others just connect groups of, for example, 25 consecutive terminals in a column. The latter design provides a circuit designer with some more control over crosstalk (inductively coupled noise) on the power supply bus. Often the groups in a bus strip are indicated by gaps in the color marking. Bus strips typically run down one or both sides of a terminal strip or between terminal strips. On large breadboards additional bus strips can often be found on the top and bottom of terminal strips.

Terminal strips:

Terminal strips are the main areas, to hold most of the electronic components. In the middle of a terminal strip of a breadboard, one typically finds a notch running in parallel to the long side. The notch is to mark the centerline of the terminal strip and provides limited airflow (cooling) to DIP ICs straddling the centerline. The clips on the right and left of the notch are each connected in a radial way; typically five clips (i.e., beneath five holes) in a row on each side of the notch are electrically connected. The five clip columns on the left of the notch are often marked as A, B, C, D, and E, while the ones on the right are marked F, G, H, I and J. When a "skinny" Dual In-line Pin package (DIP) integrated circuit (such as a typical DIP-14 or DIP-16, which have a 0.3 inch separation between the pin rows) is plugged into a breadboard, the pins of one side of the chip are supposed to go into column E while the pins of the other side go into column F on the other side of the notch.

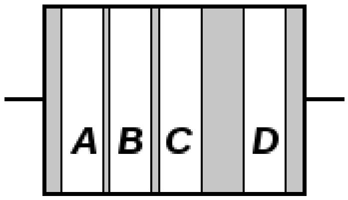
Some manufacturers provide separate bus and terminal strips. Others just provide breadboard blocks which contain both in one block. Often breadboard strips or blocks of one brand can be clipped together to make a larger breadboard. In a more robust variant, one or more breadboard strips are mounted on a sheet of metal. Typically, that backing sheet also holds a number of binding posts. These posts provide a clean way to connect an external power supply. This type of breadboard may be slightly easier to handle. Several images in this article show such solderless breadboards.

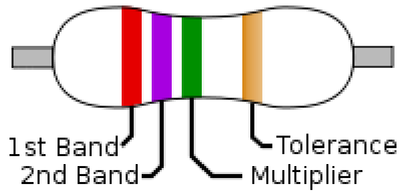


*Example **breadboard** drawing. Two bus strips and one terminal strip in one block. 25 consecutive terminals in a bus strip connected (indicated by gaps in the red and blue lines). Four **binding posts** depicted at the left.*

A "full size" terminal breadboard strip typically consists of around 56 to 65 rows of connectors, each row containing the above mentioned two sets of connected clips (A to E and F to J). Together with bus strips on each side this makes up a typical 784 to 910 tie point solderless breadboard. "Small size" strips typically come with around 30 rows. Miniature solderless breadboards as small as 17 rows (no bus strips, 170 tie points) can be found, but these are less well suited for practical use.

COLOR BANDS





To distinguish left from right there is a gap between the C and D bands.

- band **A** is first significant figure of component value (left side)
- band **B** is the second significant figure
- band **C** is the decimal multiplier
- band **D** if present, indicates tolerance of value in percent (no band means 20%)

For example, a resistor with bands of ***yellow, violet, red,*** *and* ***gold*** will have first digit 4 (yellow in table below), second digit 7 (violet), followed by 2 (red) zeros: 4,700 ohms. Gold signifies that the tolerance is ±5%, so the real resistance could lie anywhere between 4,465 and 4,935 ohms.

The standard color code:

Color	Significant figures	Multiplier	Tolerance		Temp. Coefficient (ppm/K)	
Black	0	$\times10^0$	–		250	U
Brown	1	$\times10^1$	±1%	F	100	S
Red	2	$\times10^2$	±2%	G	50	R
Orange	3	$\times10^3$	–		15	P
Yellow	4	$\times10^4$	(±5%)	–	25	Q
Green	5	$\times10^5$	±0.5%	D	20	Z
Blue	6	$\times10^6$	±0.25%	C	10	Z
Violet	7	$\times10^7$	±0.1%	B	5	M
Gray	8	$\times10^8$	±0.05% (±10%)	A	1	K
White	9	$\times10^9$	–		–	
Gold	–	$\times10^{-1}$	±5%	J	–	
Silver	–	$\times10^{-2}$	±10%	K	–	
None	–	–	±20%	M	–	

1. P-N JUNCTION DIODE CHARACTERISTICS

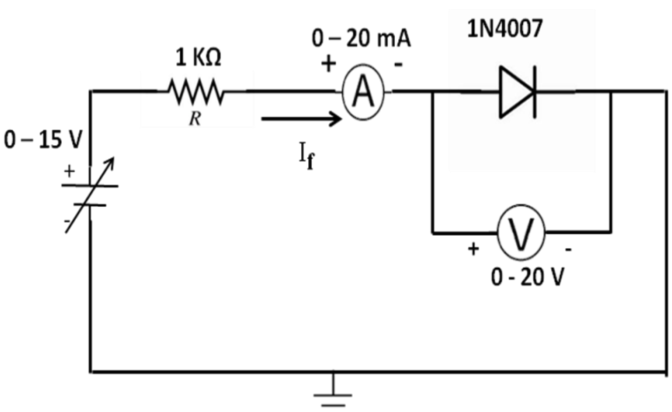
Aim: To draw the Voltage-current characteristics of PN junction diode under forward and reverse bias condition and to determine cut in voltage, reverse saturation current and forward dynamic resistance.

Apparatus Required:

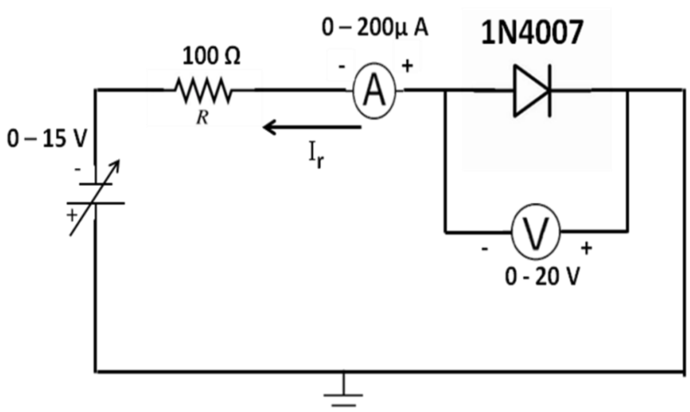
NAME	RANGE	TYPE	QUANTITY
REGULATED POWER SUPPLY (RPS)	0 -15 V		1
AMMETER	0 -20 mA		1
	0 -200 μA		
VOLTMETER	0 – 20 V		1
DIODE		1N4007	1
RESISTORS	100Ω		1
	1KΩ		1
BREADBOARD			1
CONNECTING WIRES			

CIRCUIT DIAGRAM:-

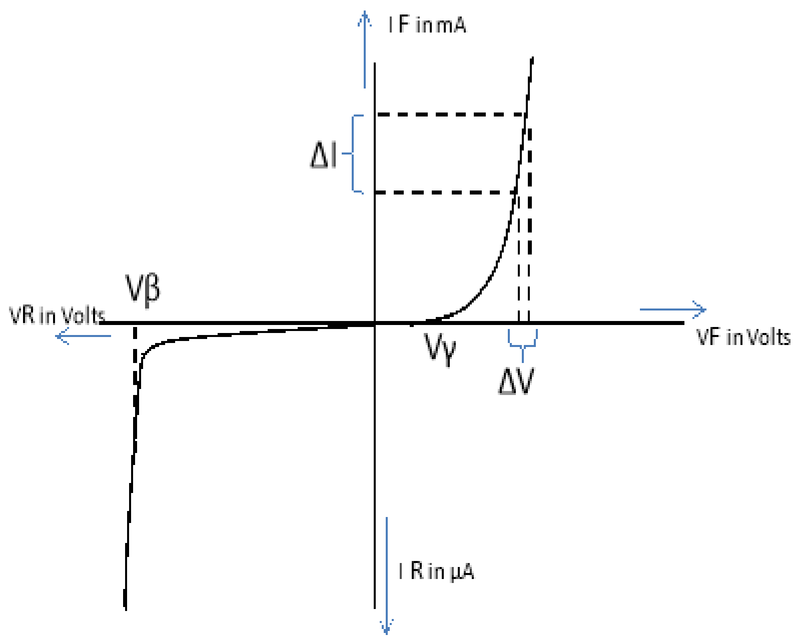
Forward bias:-



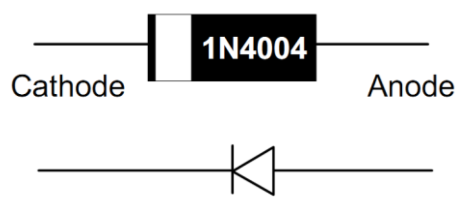
Reverse bias:-



Model waveform:-



THEORY:-



The figure shows the physical and schematic circuit symbol of the diode. The band on the diode and the bar on the left of the circuit symbol represent the cathode (n-type material) and must be noted. The p-type material (the anode) in the diode is located to the right. The circuit symbol of the diode is an arrow showing forward bias, when the p-side is positive with respect to the n-side, and the direction of the arrow represents the direction of large current flow.

A p-n junction diode conducts only in one direction. The V-I characteristics of the diode are curve between voltage across the diode and current through the diode. When external voltage is zero, circuit is open and the potential barrier does not allow the current to flow. Therefore, the circuit current is zero. When P-type (Anode is connected to +ve terminal and n- type (cathode) is connected to –ve terminal of the supply voltage, is known as forward bias. The potential barrier is reduced when diode is in the forward biased condition. At some forward voltage, the potential barrier altogether eliminated and current starts flowing through the diode and also in the circuit. The diode is said to be in ON state. The current increases with increasing forward voltage.

When N-type (cathode) is connected to +ve terminal and P-type (Anode) is connected –ve terminal of the supply voltage is known as reverse bias and the potential barrier across the junction increases. Therefore, the junction resistance becomes very high and a very small current (reverse saturation current) flows in the circuit. The diode is said to be in OFF state. The reverse bias current due to minority charge carriers.

PROCEDURE:-

Forward bias

1. Connections are made as per the circuit diagram.

2. For forward bias, the DC power supply +ve terminal is connected to the anode of the diode and –ve terminal is connected to the cathode of the diode using 1N4007.

3. Switch on the power supply and increases the input voltage gradually in Steps.

4. Note down the corresponding current flowing through the diode (in mA) and voltage across the diode for each and every step of the input voltage.

5. The reading of voltage and current are tabulated.

6. Graph is plotted between voltage and current.

7. From the graph calculate cut-in voltage, Static resistance and Dynamic resistances.

Reverse bias

1. Connections are made as per the circuit diagram.

2. For reverse bias, the DC power supply +ve terminal is connected to the cathode of the diode and –ve terminal is connected to the anode of the diode using 1N4007.

3. Switch on the power supply and increases the input voltage gradually in Steps.

4. Note down the corresponding current flowing through the diode (in µA) and voltage across the diode for each and every step of the input voltage.

5. The reading of voltage and current are tabulated.

6. Graph is plotted between voltage and current.

7. From the graph calculate Breakdown voltage.

Observations:

Forward bias

S.NO	Applied voltage (V)	Voltage across diode(V)	Current I_F (mA)
1			
2			
3			
.			
.			
.			
.			
.			
.			
.			
30			

Reverse bias

S.NO	Applied voltage (V)	Voltage across diode(V)	Current I_R (μA)
1			
2			
3			
.			
.			
.			
.			
.			
.			
.			
30			

Calculations:-

From the graph at a given operating point we can determine the static resistance (R_d) and dynamic resistance (r_d).

The static resistance (R_d) is defined as (R_d) = $\frac{V}{I}$ = __________

The Dynamic resistance (R_d) is defined as (r_d) = $\frac{\Delta V}{\Delta I}$ = __________

Precautions:-

1. All the connections should be correct.

2. While doing the experiment do not exceed the ratings of the diode. This may lead to damage of the diode.

3. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.

4. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

5. Parallax error should be avoided while taking the readings from the (if) Analog meters.

RESULT:- Forward and Reverse Bias characteristics for a p-n diode is observed.

VIVA QESTIONS:-

1. Define depletion region of a diode?

2. What is meant by transition & space charge capacitance of a diode?

3. Is the V-I relationship of a diode Linear or Exponential?

4. Define cut-in voltage of a diode and specify the values for Si and Ge diodes?

5. What are the applications of a p-n diode?

6. Draw the ideal characteristics of P-N junction diode?

7. What is the diode equation?

8. What is PIV?

9. What is the break down voltage?

10. What is the effect of temperature on PN junction diodes?

2. ZENER DIODE CHARACTERISTICS

AIM:

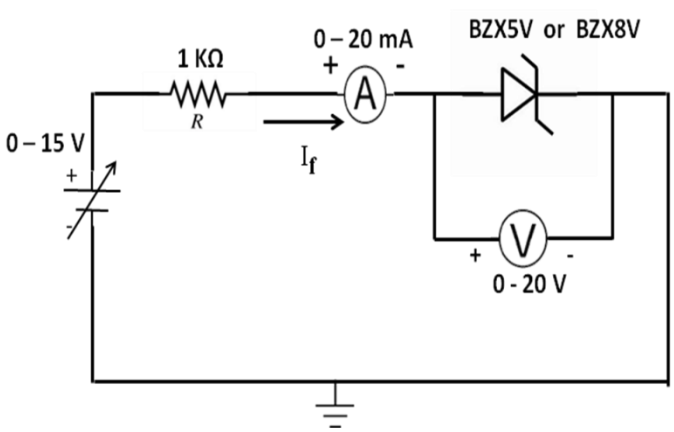
To volt-ampere characteristics of a given Zener diode, breakdown voltage, voltage regulation of a given zener diode and Dynamic reverse bias resistance at breakdown voltage.

Apparatus Required:

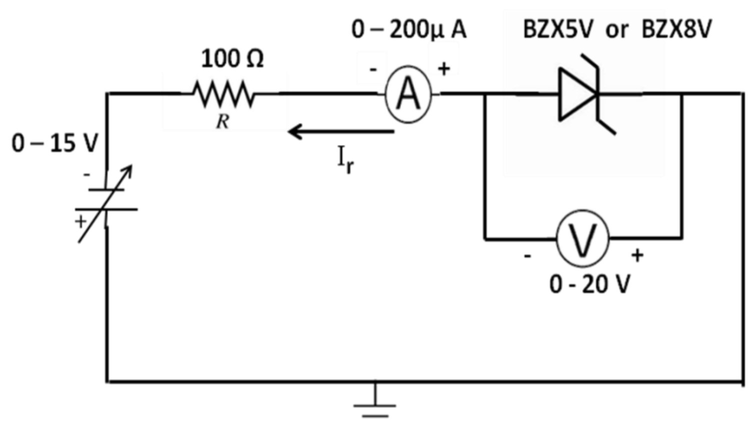
NAME	RANGE	TYPE	QUANTITY
REGULATED POWER SUPPLY (RPS)	0 -15 V		1
AMMETER	0 -20 mA		1
	0 -200 µA		
VOLTMETER	0 – 20 V		1
DIODE		BZX5V	1
		BZX8V	1
RESISTORS	100Ω		1
	1KΩ		1
BREADBOARD			1
CONNECTING WIRES			

<u>CIRCUIT DIAGRAM</u>:-

Forward bias:-



Reverse bias:-



<u>Theory:-</u>

A zener diode is heavily doped p-n junction diode, specially made to operate in the break down region. A p-n junction diode normally does not conduct when reverse biased. But if the reverse bias is increased, at a particular voltage it starts conducting heavily. This voltage is called Break down Voltage. High current through the diode can permanently damage the device. To avoid high current, we connect a resistor in series with zener diode. Once the diode starts conducting it maintains almost constant voltage across the terminals what ever may be the current through it, i.e., it has very low dynamic resistance. It is used in voltage regulators.

PROCEDURE:-

Forward bias:-

1. Connections are made as per the circuit diagram.

2. For forward bias, the DC power supply +ve terminal is connected to the anode of the diode and –ve terminal is connected to the cathode of the zener diode using BZX5V or BZX8V.

3. Switch on the power supply and increases the input voltage gradually in Steps.

4. Note down the corresponding current flowing through the diode (in mA) and voltage across the diode for each and every step of the input voltage and tabulate the readings.

5. Graph is plotted between voltage and current.

6. From the graph calculate cut-in voltage, Static resistance and Dynamic resistances.

Reverse bias:-

1. Connections are made as per the circuit diagram.

2. For reverse bias, the DC power supply +ve terminal is connected to the cathode of the diode and -ve terminal is connected to the anode of the zener diode using BZX5V or BZX8V.

3. Switch on the power supply and increases the input voltage gradually in Steps.

4. Note down the corresponding current flowing through the diode (in µA) and voltage across the diode for each and every step of the input voltage.

5. The reading of voltage and current are tabulated.

6. Graph is plotted between voltage and current, and from the graph calculate the Breakdown voltage.

Observations:

Forward bias

S.NO	Applied voltage (V)	Voltage across diode(V)	Current I_F (mA)

Reverse bias

S.NO	Applied voltage (V)	Voltage across diode(V)	Current I_R (μA)

Calculations:-

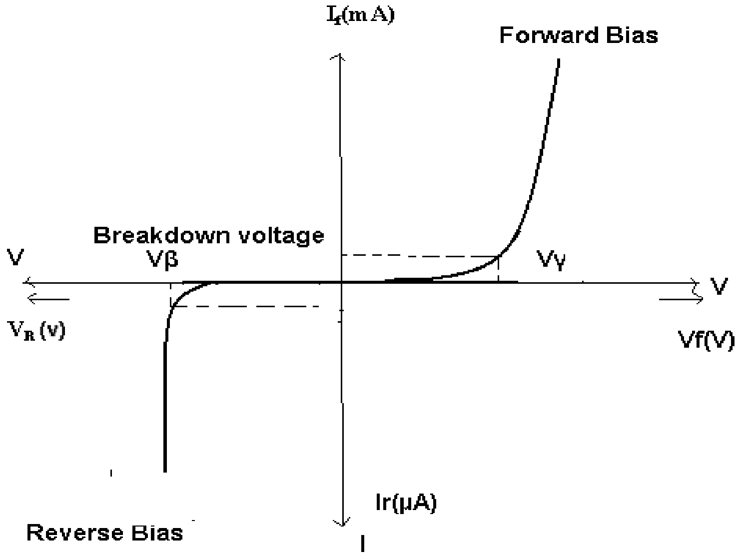
From the graph at a given operating point we can determine the static resistance (R_d) and dynamic resistance (r_d).

The static resistance (R_d) is defined as (R_d) = $\frac{V}{I}$ = __________

The Dynamic resistance (R_d) is defined as (r_d) = $\frac{\Delta V}{\Delta I}$ = __________

Breakdown voltage in reverse bias = ___________

MODEL WAVEFORMS:-



PRECAUTIONS:-

1. The terminals of the zener diode should be properly identified
2. While determined the load regulation, load should not be immediately shorted.
3. Should be ensured that the applied voltages & currents do not exceed the ratings of the diode.

RESULT:-

a) Static characteristics of zener diode are obtained and drawn.

b) Percentage regulation of zener diode is calculated.

VIVAQUESTIONS:-

1. *What type of temperature Coefficient does the zener diode have?*
2. *If the impurity concentration is increased, how the depletion width effected?*
3. *Does the dynamic impendence of a zener diode vary?*
4. *Explain briefly about avalanche and zener breakdowns?*
5. *Draw the zener equivalent circuit?*
6. *Differentiate between line regulation & load regulation?*
7. *In which region zener diode can be used as a regulator?*
8. *How the breakdown voltage of a particular diode can be controlled?*
9. *What type of temperature coefficient does the Avalanche breakdown has?*
10. *By what type of charge carriers the current flows in zener and avalanche breakdown diodes?*

3. TRANSISTOR COMMON -BASE CONFIGURATION

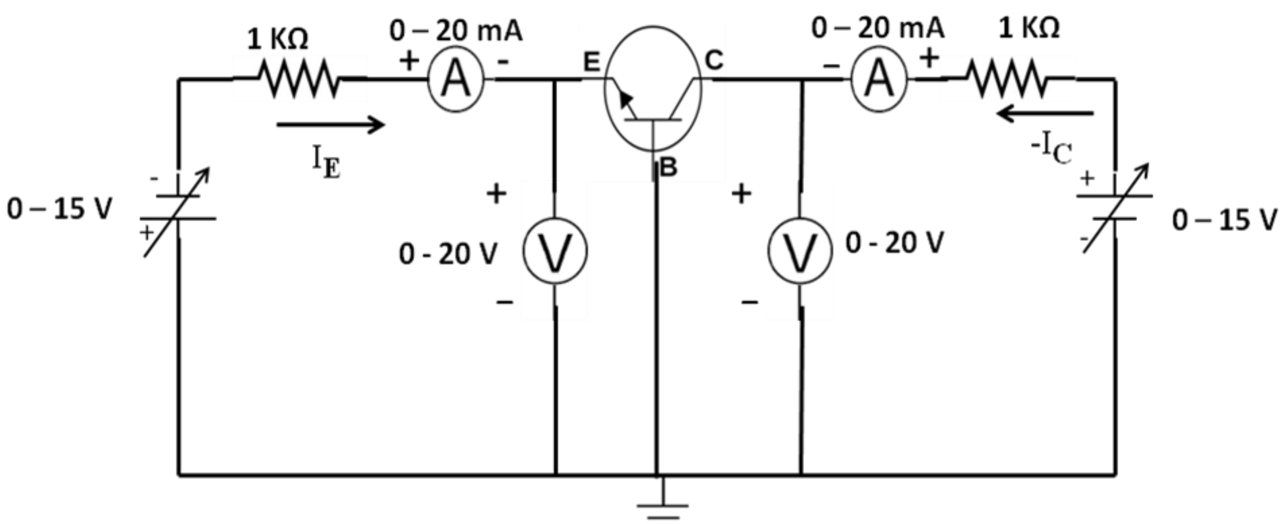
AIM:

1. To plot the input and output characteristics of a transistor connected in common base configuration.
2. To calculate the input dynamic resistance and output dynamic resistance at a given operating point.
3. To calculate the dc current gain (α_{dc}) and ac current gain (α_{ac}) at a given operating point.

Apparatus Required:

NAME	RANGE	TYPE	QUANTITY
REGULATED POWER SUPPLY (RPS)	0 -15 V		2
AMMETER	0 -20 mA 0 -200 μA		1
VOLTMETER	0 – 20 V		1
TRANSISTOR		BC107 (NPN)	1
RESISTORS	1KΩ		2
BREADBOARD			1
CONNECTING WIRES			

CIRCUIT DIAGRAM:-



THEORY:

A transistor is a three terminal active device. T he terminals are emitter, base, collector. In CB configuration, the base is common to both input (emitter) and output (collector). For normal operation, the E-B junction is forward biased and C-B junction is reverse biased.

In CB configuration, I_E is +ve, I_C is –ve and I_B is –ve. So,

$$V_{EB}=f1\ (V_{CB}, I_E) \text{ and}$$

$$I_C=f2\ (V_{CB}, I_B)$$

With an increasing the reverse collector voltage, the space-charge width at the output junction increases and the effective base width 'W' decreases. This phenomenon is known as "Early effect". Then, there will be less chance for recombination within the base region. With increase of charge gradient with in the base region, the current of minority carriers injected across the emitter junction increases.The current amplification factor of CB configuration is given by,

$$\alpha= \Delta I_C / \Delta I_E$$

PROCEDURE:

Input characteristics:

1. Connections are made as per the circuit diagram.
2. For plotting the input characteristics, set V_{CB} = 0V and vary V_{EE} gradually in steps and note down the corresponding I_E and V_{EB}.
3. Repeat the above step by keeping V_{CB} at 4V, 6V, and 10V.
4. Tabulate the readings.
5. Plot the graph between V_{EB} and I_E for constant V_{CB}.

Output characteristics:

1. Connections are made as per the circuit diagram.
2. For plotting the output characteristics, set I_E = 2 mA and vary V_{CC} gradually in steps and note down the corresponding I_C and V_{CB}.
3. Repeat the above step by keeping I_E = 4 mA, 6 mA.
4. Tabulate the readings.
5. Plot the graph between V_{CB} and I_C for constant I_E.

OBSERVATIONS:

Input characteristics:

V_{CB}=0V		V_{CB}=4V		V_{CB}=6V	
V_{EB}(V)	I_E(mA)	V_{EB}(V)	I_E(mA)	V_{EB}(V)	I_E(mA)

HALF PAGE

Output characteristics:

I_E = 2mA		I_E = 4mA		I_E = 6mA	
V_{CB}(V)	I_C(mA)	V_{CB}(V)	I_C(mA)	V_{CB}(V)	I_C(mA)

HALF PAGE

<u>Calculations</u>:-

Input dynamic resistance (r_i) = $\frac{\Delta V_{EB}}{\Delta I_{EB}}$ = __________

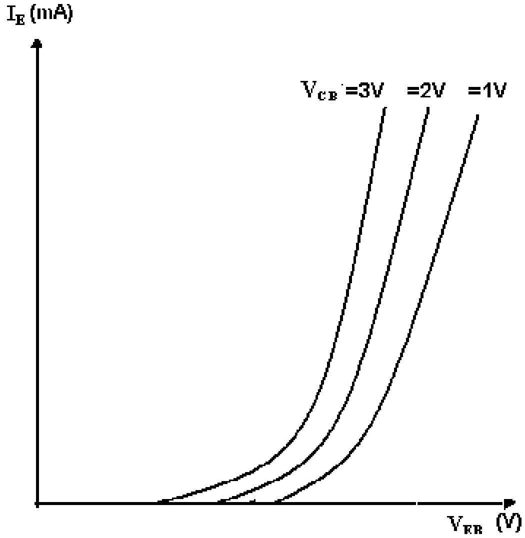
Output dynamic resistance (r_o) = $\frac{\Delta V_{CB}}{\Delta I_C}$ = __________

Dc current gain, (α_{dc}) = $\frac{I_C}{I_E}$ = _________

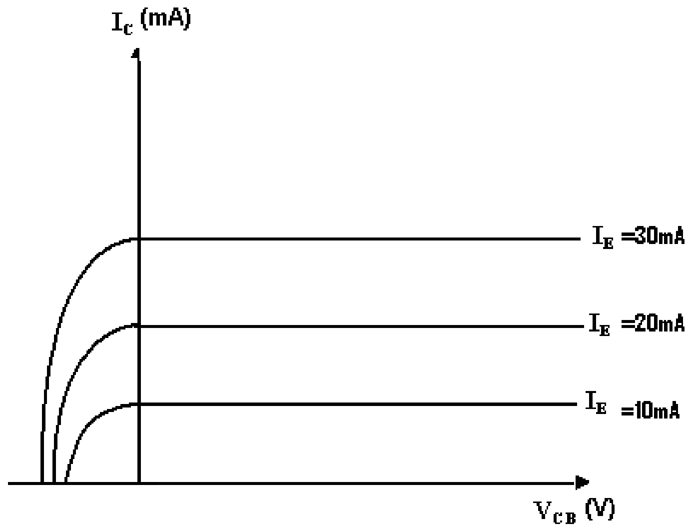
Ac current gain (α_{ac}) = $\frac{\Delta I_C}{\Delta I_E}$ = _________

MODEL GRAPHS:

Input characteristics



Output characteristics



PRECAUTIONS:

1. The supply voltages should not exceed the rating of the transistor.
2. Meters should be connected properly according to their polarities.

RESULT:

1. The input and output characteristics of the transistor are drawn.
2. The α of the given transistor is calculated.

Viva questions:

1. *What is the range of α for the transistor?*
2. *Draw the input and output characteristics of the transistor in CB configuration?*
3. *Identify various regions in output characteristics?*
4. *What is the relation between α and β?*
5. *What are the applications of CB configuration?*
6. *What are the input and output impedances of CB configuration?*
7. *Define α(alpha)?*
8. *What is EARLY effect?*
9. *Draw diagram of CB configuration for PNP transistor?*
10. *What is the power gain of CB configuration?*

4. TRANSISTOR CE CHARACTERSTICS

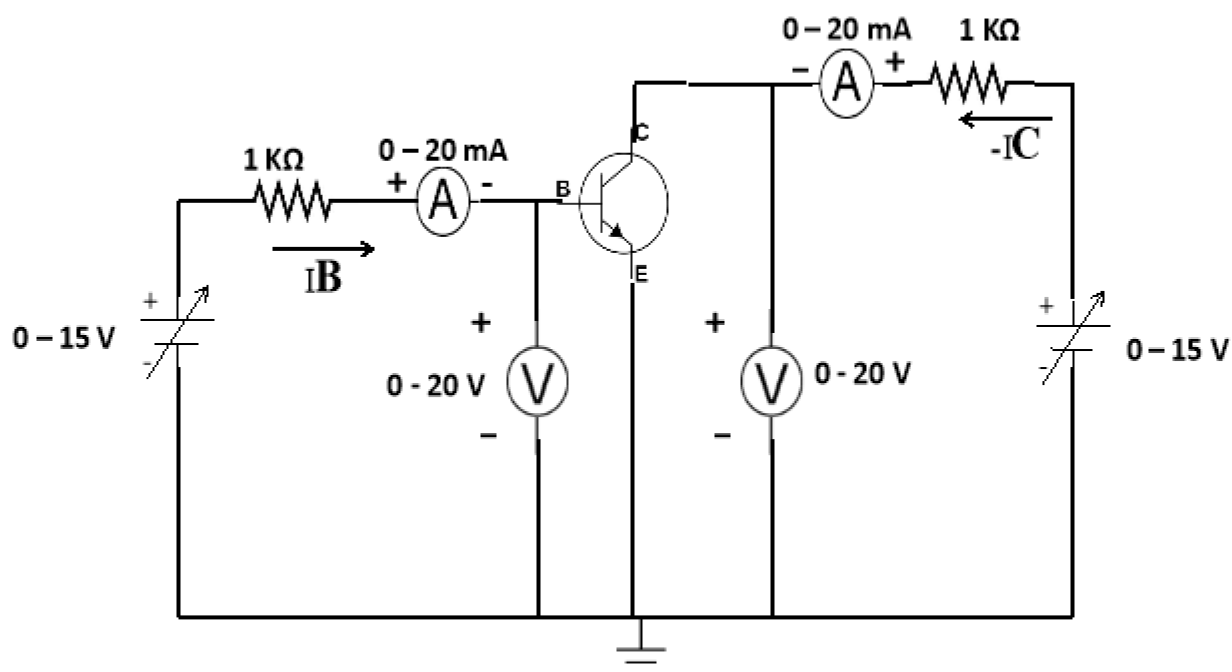
AIM: 1. To draw the input and output characteristics of transistor connected in CE configuration

2. To find β of the given transistor.

Apparatus Required:

NAME	RANGE	TYPE	QUANTITY
REGULATED POWER SUPPLY (RPS)	0 -15 V		2
AMMETER	0 -20 mA 0 -200 μA		1
VOLTMETER	0 – 20 V		1
TRANSISTOR		BC107 (NPN)	1
RESISTORS	1KΩ		2
BREADBOARD			1
CONNECTING WIRES			

CIRCUIT DIAGRAM:-



THEORY:

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and out put is taken across the collector and emitter terminals.

Therefore the emitter terminal is common to both input and output.

The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement I_B increases less rapidly with V_{BE} . Therefore input resistance of CE circuit is higher than that of CB circuit.

The output characteristics are drawn between I_c and V_{CE} at constant $I_{B.}$ the collector current varies with V_{CE} unto few volts only. After this the collector current becomes almost constant, and independent of $V_{CE.}$ The value of V_{CE} up to which the collector current changes with V_{CE} is known as Knee voltage. The transistor always operated in the region above Knee voltage, I_C is always constant and is approximately equal to $I_{B.}$

The current amplification factor of CE configuration is given by

$$B = \Delta I_C/\Delta I_B$$

PROCEDURE:

INPUT CHARECTERSTICS:

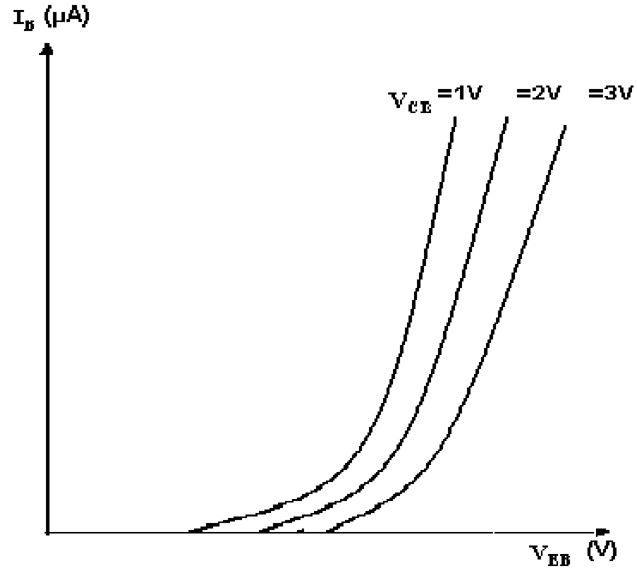
1. Connect the circuit as per the circuit diagram.
2. For plotting the input characteristics the output voltage V_{CE} is kept constant at 0V and for different values of V_{BE} note down the values of $I_{C.}$
3. Repeat the above step by keeping V_{CE} at 2V and 4V.
4. Tabulate all the readings.
5. plot the graph between V_{BE} and I_B for constant V_{CE}

OUTPUT CHARACTERSTICS:

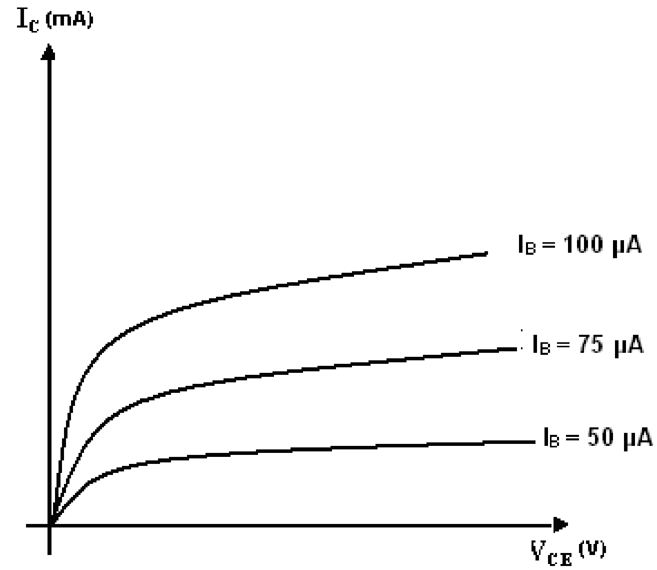
1. Connect the circuit as per the circuit diagram
2. for plotting the output characteristics the input current I_B is kept constant at 10μA and for different values of V_{CE} note down the values of I_C
3. repeat the above step by keeping IB at 75 μA 100 μA
4. tabulate the all the readings
5. plot the graph between V_{CE} and I_C for constant I_B

MODEL GRAPHS:

INPUT CHARACTERSTICS:



OUTPUT CHARECTERSTICS:



Observations:

HALF PAGE

INPUT CHARACTERISTICS:

V_{CE} = 1V		V_{CE} = 2V		V_{CE} = 4V	
V_{BE}(V)	I_B(μA)	V_{BE}(V)	I_B(μA)	V_{BE}(V)	I_B(μA)

OUT PUT CHAREACTARISTICS:

HALF PAGE

I_B = 50 μA		I_B = 75 μA		I_B = 100 μA	
V_{CE}(V)	I_C(mA)	V_{CE}(V)	I_CmA)	V_{CE}(V)	I_C(mA)

Calculations:-

Input dynamic resistance (r_i) = $\dfrac{\Delta V_{BE}}{\Delta I_B}$ = _________

Output dynamic resistance (r_o) = $\dfrac{\Delta V_{CE}}{\Delta I_C}$ = _________

Dc current gain, (α_{dc}) = $\dfrac{I_C}{I_B}$ = ________

Ac current gain (α_{ac}) = $\dfrac{\Delta I_C}{\Delta I_B}$ = ________

PRECAUTIONS:

1. The supply voltage should not exceed the rating of the transistor
2. Meters should be connected properly according to their polarities

RESULT:

1. the input and out put characteristics of a transistor in CE configuration are Drawn
2. the β of a given transistor is calculated

VIVA QUESTIONS:

1. *What is the range of β for the transistor?*
2. *What are the input and output impedances of CE configuration?*
3. *Identify various regions in the output characteristics?*
4. *what is the relation between α and β*
5. *Define current gain in CE configuration?*
6. *Why CE configuration is preferred for amplification?*
7. *What is the phase relation between input and output?*
8. *Draw diagram of CE configuration for PNP transistor?*
9. *What is the power gain of CE configuration?*
10. *What are the applications of CE configuration?*

5. HALF – WAVE RECTIFIER

AIM: -

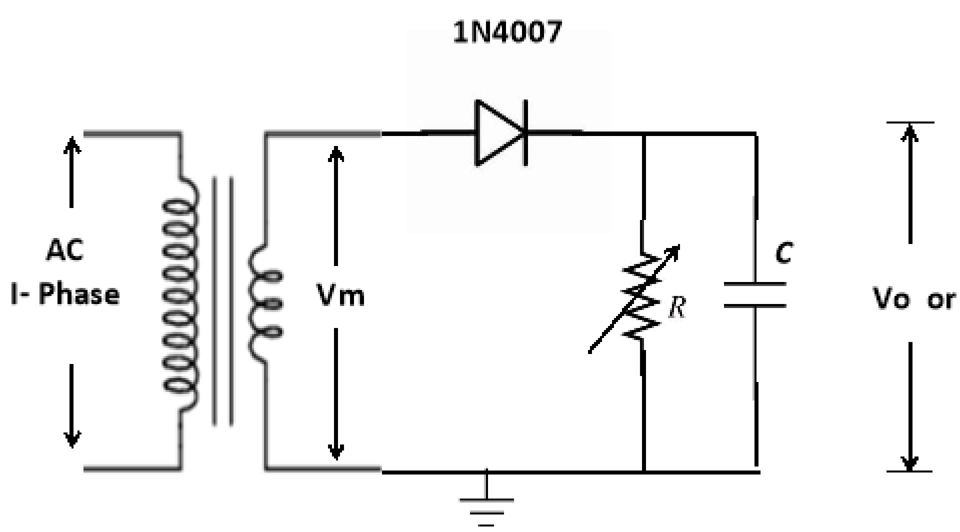
1.To observe the input and output waveforms of the Half-wave rectifier on CRO with and without filter.

2.To find load regulation and ripple factor of a half-wave rectifier both with and without filter.

Apparatus Required:

NAME	RANGE	TYPE	QUANTITY
STEP DOWN TRANSFORMER	230 V / 12-0-12		1
DIODE		1N4007	1
CAPACITORS	2 .2 μF		1
	100 μF		1
RESISTORS	100 Ω		1
	1KΩ		1
	2.2 KΩ		1
	5.8 KΩ		1
	10 KΩ		1
	1 MΩ		1
BREADBOARD			1
CATHODE RAY OSCILLOSCOPE	0 – 20 MHZ	DUEL CHANNEL	1
DIGITAL MULTIMETER			1
CONNECTING PROBES			SUFFICIENT
CONNECTING WIRES			SUFFICIENT

CIRCUIT DIAGRAM:-



THEORY: -

During positive half-cycle of the input voltage, the diode D1 is in forward bias and conducts through the load resistor R1. Hence the current produces an output voltage across the load resistor R1, which has the same shape as the +ve half cycle of the input voltage.

During the negative half-cycle of the input voltage, the diode is reverse biased and there is no current through the circuit. i.e, the voltage across R1 is zero. The net result is that only the +ve half cycle of the input voltage appears across the load. The average value of the half wave rectified o/p voltage is the value measured on dc voltmeter.

For practical circuits, transformer coupling is usually provided for two reasons.

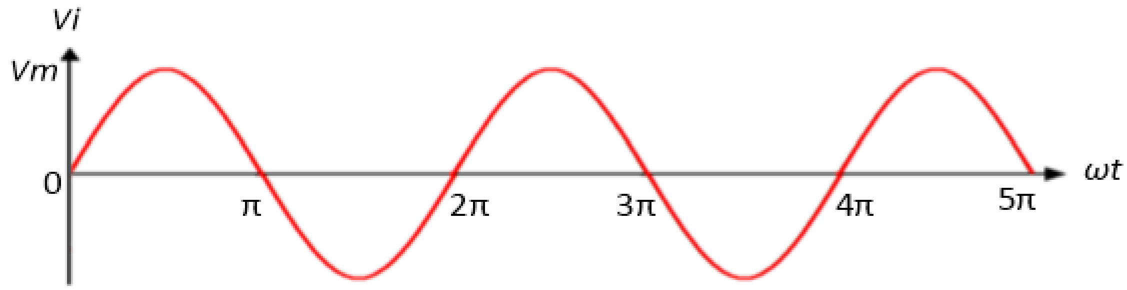
1. The voltage can be stepped-up or stepped-down, as needed.
2. The ac source is electrically isolated from the rectifier. Thus preventing shock hazards in the secondary circuit.

PROCEDURE:-

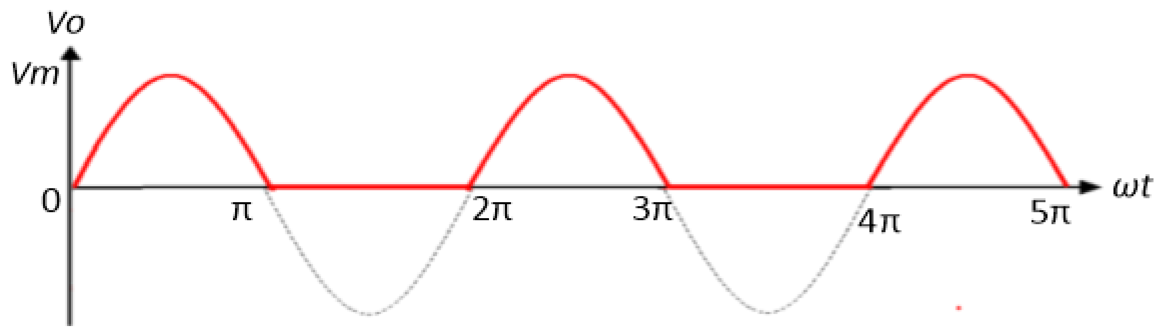
1. Connections are made as per the circuit diagram.
2. Connect the primary side of the transformer to ac mains and the secondary side to the rectifier input.
3. By the millimeter, measure the, ac and dc voltage at the output of the rectifier with 100 Ω load resistor $V_{AC(RMS)}$ and V_{DC} respectively.
4. From the CRO output, calculate V_m.
5. Repeat the above step by using different load resistors i.e. with 1 KΩ, 2.2 KΩ, 5.8 KΩ and 10 KΩ.
6. For each reading calculate the ripple factor and percentage regulation.
   (Calculate percentage regulation using 1 MΩ resistor as no load.)
7. Repeat the above steps (3, 4, 5 and 6) by using 2.2 µF capacitor filter.
8. Repeat the above steps (3, 4, 5 and 6) by using 100 µF capacitor filter.
9. Plot the graphs for ***AC input I-Phase signal***, ***output of rectifier without filter*** and ***output of rectifier with filter*** by considering 1 KΩ resistor as load.

Expected Waveforms:

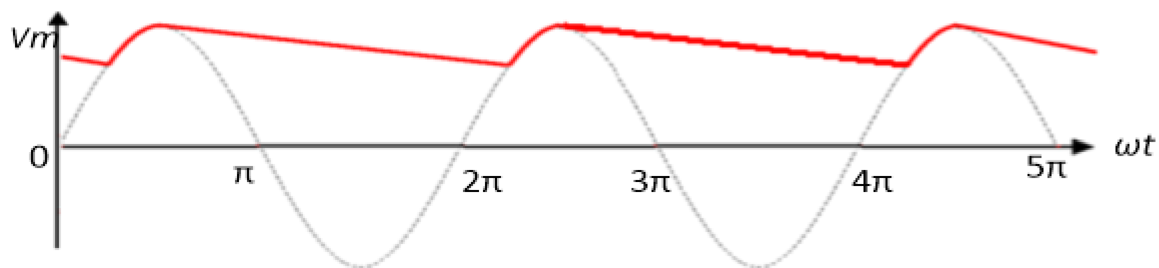
Input waveform:



Without filter output waveform:



With filter output waveform:



Observations

Observation for without filter with varying load resistance:

S. No.	Load Resistor	V_m	V_{dc} = V_m / π	V_{ac}(rms) = Vm / 2	Ripple factor(γ)	% Regulation

Observation for with filter c= 2.2 µF with varying load resistance:

S. No.	Load Resistor	V_m	V_{dc} $= V_m / Л$	V_{ac}(rms) = Vm / 2	Ripple factor(γ)	% Regulation

Observation for with filter c= 100 µF with varying load resistance:

S. No.	Load Resistor	V_m	V_{dc} $= V_m / Л$	V_{ac}(rms) = Vm / 2	Ripple factor(γ)	% Regulation

CALCULATIONS:

Theoretical Calculations:-

Without Filter:-

$V_{rms}=V_m/2$ = ________

$V_m=2V_{rms}$ = ________

$V_{dc}=V_m/\Pi$ = ________

Ripple factor $r=\sqrt{(V_{rms}/V_{dc})^2-1}=1.21$

With Filter:-

Ripple factor, $r=1/(2\sqrt{3}\, f\, C\, R)$ = ________

Where f =50Hz, C =100µF, R=1KΩ.

Practical calculations:-

V_{ac}= ________

V_{dc}= ________

Ripple factor with out Filter = V_{ac} / V_{dc} = ________

Ripple factor with Filter = V_{ac} / V_{dc} = ________

$$\% \text{ Regulation} = \frac{(V_{NL}-V_{FL})}{V_{NL}} \times 100 = \_\_\_\_\_\_\_\_$$

PRECAUTIONS:

1. The primary and secondary sides of the transformer should be carefully identified.
2. The polarities of the diode should be carefully identified.
3. While determining the % regulation, first Full load should be applied and then it should be decremented in steps.

RESULT:-

1. The Ripple factor for the Half-Wave Rectifier with and without filters is measured.
2. The % regulation of the Half-Wave rectifier is calculated.

VIVA QUESTIONS:

1. *What is the PIV of Half wave rectifier?*
2. *What is the efficiency of half wave rectifier?*
3. *What is the rectifier?*
4. *What is the difference between the half wave rectifier and full wave Rectifier?*
5. *What is the o/p frequency of Bridge Rectifier?*
6. *What are the ripples?*
7. *What is the function of the filters?*
8. *What is TUF?*
9. *What is the average value of o/p voltage for HWR?*
10. *What is the peak factor?*

6. FULL-WAVE RECTIFIER

AIM:-

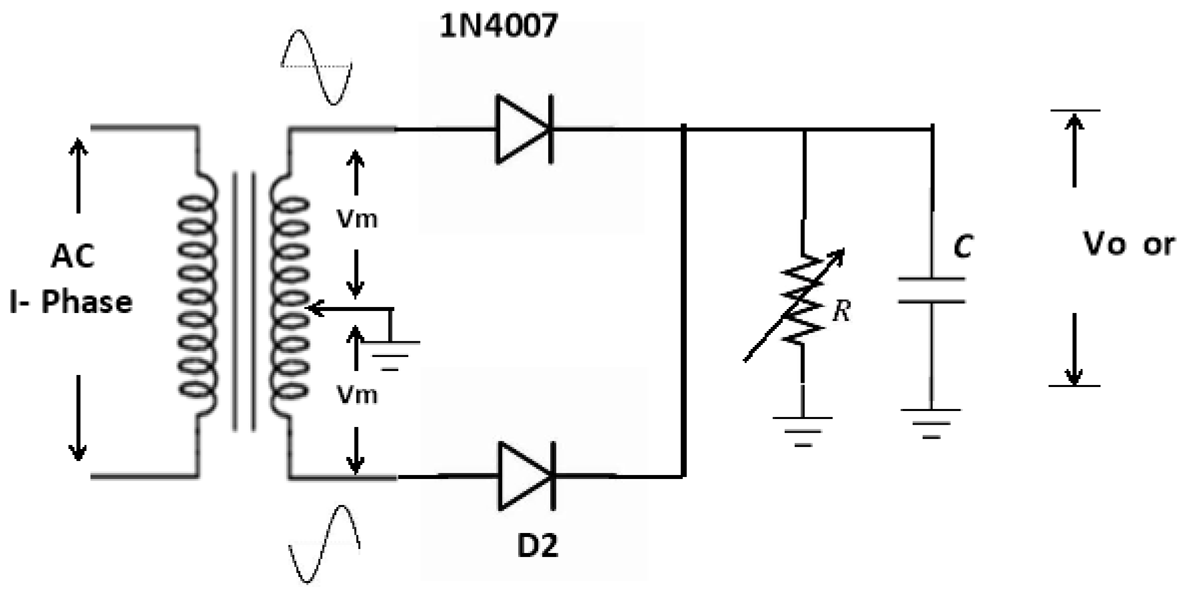
1.To observe the input and output waveforms of the Full-wave rectifier on CRO with and without filter.

2.To find load regulation and ripple factor of a Full-wave rectifier both with and without filter.

Apparatus Required:

NAME	RANGE	TYPE	QUANTITY
STEP DOWN TRANSFORMER	230 V / 12-0-12		1
DIODE		1N4007	2
CAPACITORS	2 .2 μF		1
	100 μF		1
RESISTORS	100 Ω		1
	1KΩ		1
	2.2 KΩ		1
	5.8 KΩ		1
	10 KΩ		1
	1 MΩ		1
BREADBOARD			1
CATHODE RAY OSCILLOSCOPE	0 – 20 MHz	DUEL CHANNEL	1
DIGITAL MULTIMETER			1
CONNECTING PROBES			SUFFICIENT
CONNECTING WIRES			SUFFICIENT

CIRCUIT DIAGRAM:-



THEORY:-

The circuit of a center-tapped full wave rectifier uses two diodes D1&D2. During positive half cycle of secondary voltage (input voltage), the diode D1 is forward biased and D2is reverse biased.

The diode D1 conducts and current flows through load resistor R_L. During negative half cycle, diode

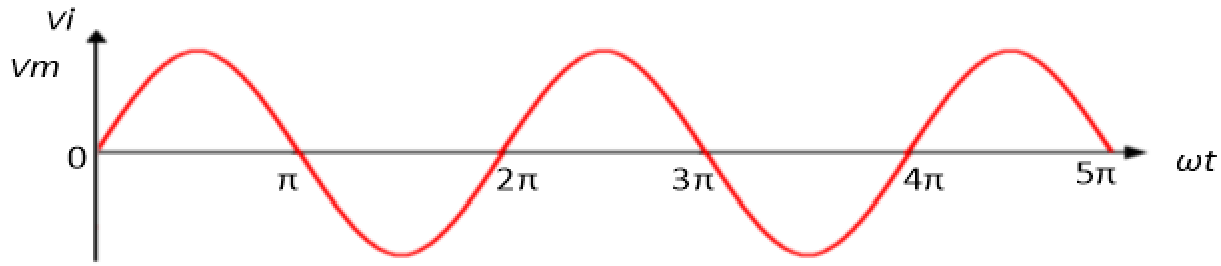
D2 becomes forward biased and D1 reverse biased. Now, D2 conducts and current flows through the load resistor R_L in the same direction. There is a continuous current flow through the load resistor R_L, during both the half cycles and will get unidirectional current as show in the model graph. The difference between full wave and half wave rectification is that a full wave rectifier allows unidirectional (one way) current to the load during the entire 360 degrees of the input signal and half-wave rectifier allows this only during one half cycle (180 degree).

PROCEDURE:-

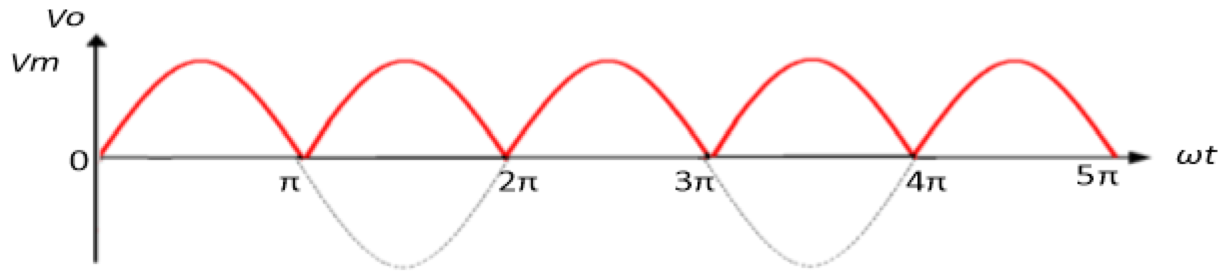
1. Connections are made as per the circuit diagram.
2. Connect the primary side of the transformer to ac mains and the secondary side to the rectifier input.
3. By the millimeter, measure the, ac and dc voltage at the output of the rectifier with 100 Ω load resistor $V_{AC(RMS)}$ and V_{DC} respectively.
4. From the CRO output, calculate V_m.
5. Repeat the above step by using different load resistors i.e. with 1 KΩ, 2.2 KΩ, 5.8 KΩ and 10 KΩ.
6. For each reading calculate the ripple factor and percentage regulation.
   (Calculate percentage regulation using 1 MΩ resistor as no load.)
7. Repeat the above steps (3, 4, 5 and 6) by using 2.2 µF capacitor filter.
8. Repeat the above steps (3, 4, 5 and 6) by using 100 µF capacitor filter.
9. Plot the graphs for ***AC input I-Phase signal***, ***output of rectifier without filter*** and ***output of rectifier with filter*** by considering 1 KΩ resistor as load.

Expected Waveforms:

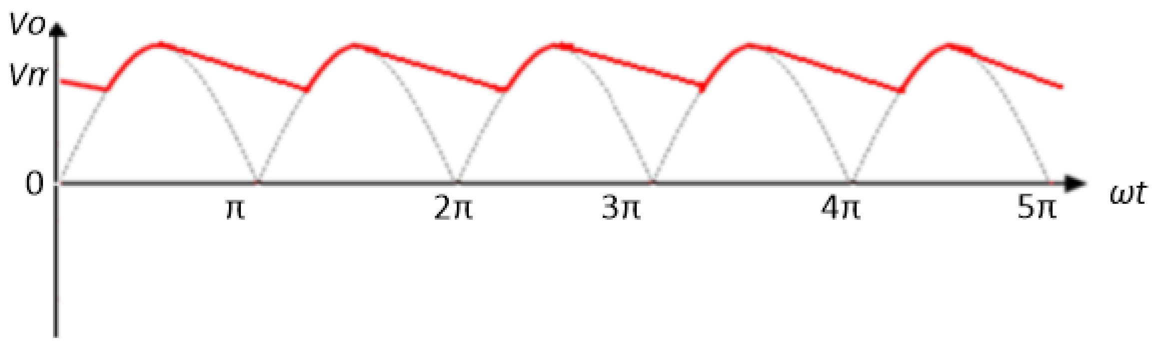
Input waveform:



Without filter output waveform:



With filter output waveform:



Observations

Observation for without filter with varying load resistance:

S. No.	Load Resistor	V_m	$V_{dc} = 2V_m / \pi$	V_{ac}(rms) = Vm / √2	Ripple factor(γ)	% Regulation

Observation for with filter c= 2.2 µF with varying load resistance:

S. No.	Load Resistor	V_m	V_{dc} $= 2V_m / \pi$	$V_{ac}(rms)$ $= Vm / \sqrt{2}$	Ripple factor(γ)	% Regulation

Observation for with filter c= 100 μF with varying load resistance:

S. No.	Load Resistor	V_m	V_{dc} $= 2V_m / \pi$	$V_{ac}(rms)$ $= Vm / \sqrt{2}$	Ripple factor(γ)	% Regulation

THEORITICAL CALCULATIONS:-

$Vrms = V_m / \sqrt{2}$ = __________

$Vm = V_{rms}\sqrt{2}$ = __________

$Vdc = 2V_m / \Pi$ = __________

***(i)Without filter**:* Ripple factor, $r = \sqrt{(Vrms/ Vdc)^2 - 1} = 0.482$

(ii)With filter**:* Ripple factor, $r = 1/ (4\sqrt{3}\, f\, C\, R_L)$ **=** ___________ (where f =50Hz , C =100μF , R_L=1KΩ)***

PRACTICAL CALCULATIONS:

Without filter:- V_{ac} = __________

V_{dc} = __________

Ripple factor, $r = V_{ac} / V_{dc}$ = __________

With filters:- V_{ac}= ________

V_{dc}= ________

Ripple factor=V_{ac} / V_{dc} = ________

PRECAUTIONS:

1. The primary and secondary side of the transformer should be carefully identified
2. The polarities of all the diodes should be carefully identified.

RESULT:-

The ripple factor of the Full-wave rectifier (with filter and without filter) is calculated.

VIVA QUESTIONS:-

1. *Define regulation of the full wave rectifier?*
2. *Define peak inverse voltage (PIV)? And write its value for Full-wave rectifier?*
3. *If one of the diode is changed in its polarities what wave form would you get?*
4. *Does the process of rectification alter the frequency of the waveform?*
5. *What is ripple factor of the Full-wave rectifier?*
6. *What is the necessity of the transformer in the rectifier circuit?*
7. *What are the applications of a rectifier?*
8. *What is ment by ripple and define Ripple factor?*
9. *Explain how capacitor helps to improve the ripple factor?*
10. *Can a rectifier made in INDIA (V=230v, f=50Hz) be used in USA (V=110v, f=60Hz)?*

7. FET CHARACTERISTICS

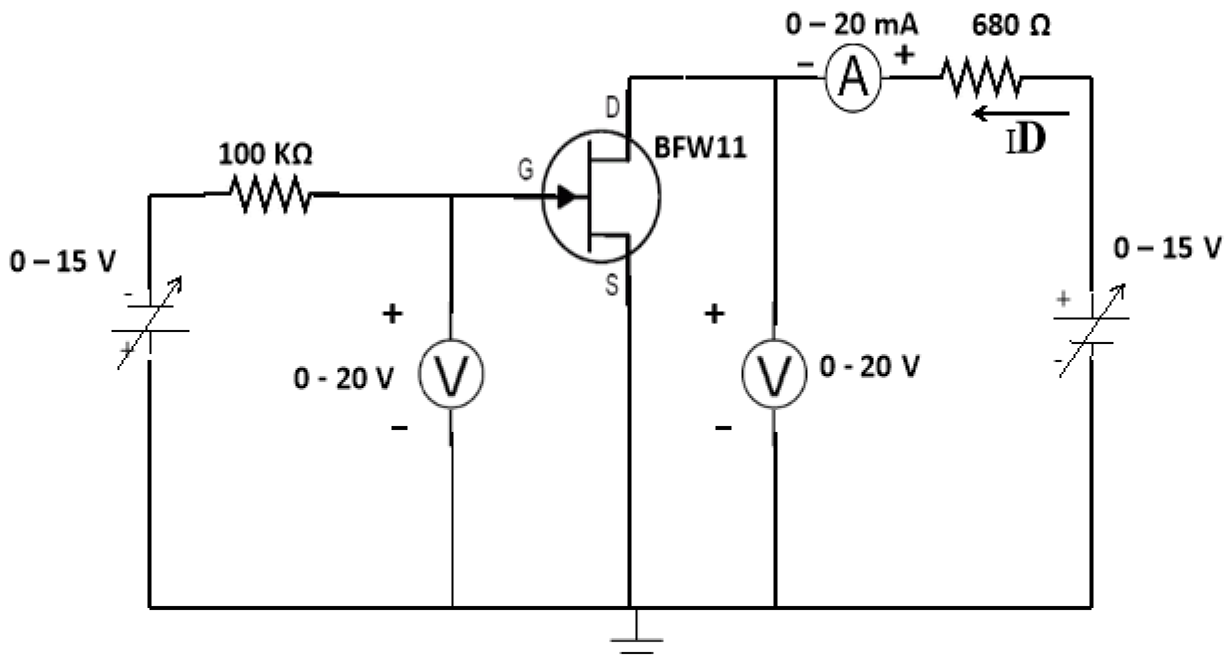
AIM: a). To plot a family of **drain** and **transfer** characteristics of a given FET.

b). To find the FET parameters ***drain resistance*** *(r_d)*, ***amplification factor*** *(μ)*, and ***trans-conductance*** *(g_m)* of the given FET.

Apparatus Required:

NAME	RANGE	TYPE	QUANTITY
REGULATED POWER SUPPLY (RPS)	0 – 15 V		2
AMMETER	0 – 20 mA		1
	0 – 200 μA		
VOLTMETER	0 – 20 V		1
FIELD EFFECT TRANSISTOR (FET)		BFW11	1
RESISTORS	100KΩ		1
	680Ω		1
BREADBOARD			1
CONNECTING WIRES			SUFFICIENT

Circuit Diagram:-



Theory:

A FET is a three terminal device, having the characteristics of high input impedance and less noise, the Gate to Source junction of the FET s always reverse biased. In response to small applied voltage from drain to source, the n-type bar acts as sample resistor, and the drain current increases linearly with $V_{DS.}$ With increase in I_D the ohmic voltage drop between the source and the channel region reverse biases the junction and the conducting position of the channel begins to remain constant. The V_{DS} at this instant is called "pinch of voltage".

If the gate to source voltage (V_{GS}) is applied in the direction to provide additional reverse bias, the pinch off voltage ill is decreased.

In amplifier application, the FET is always used in the region beyond the pinch-off.

$$F_{DS} = I_{DSS*}(1-V_{GS}/V_P)\hat{}2$$

Procedure:

To obtain drain characteristics:

1. All the connections are made as per the circuit diagram.
2. To plot the drain characteristics, keep $\mathbf{V_{GS}}$ constant at **0V** (V_{GS} can be set 0V by short circuiting the terminals of input power supply).
3. Vary the **drain voltage** (V_{DD}) and observe the values of **source voltage** (V_{DS}) and **drain current** (I_D) and note down values in convenient steps.
4. Repeat the above step 3 for different values of $\mathbf{V_{GS}}$ at **-1V** and **-2V.**
5. All the readings are tabulated and plot the graph V_{DS} verses I_D for a constant V_{GS}.

To obtain transfer characteristics:

6. To plot the transfer characteristics, keep $\mathbf{V_{DS}}$ constant at **0.5 V.**
7. Vary the **gate voltage** (V_{GG}) and observe the values of **gate source voltage** (V_{GS}) and **drain current** (I_D) and note down values in convenient steps.
8. Repeat step 7 for different values of $\mathbf{V_{DS}}$ at **1 V** and **1.5 V**.
9. The readings are tabulated and plot the graph V_{GS} verses I_D for a constant V_{DS}.
10. From drain characteristics, calculate the values of dynamic resistance (r_d) by using the formula

    $$r_d = \Delta V_{DS}/\Delta I_D$$

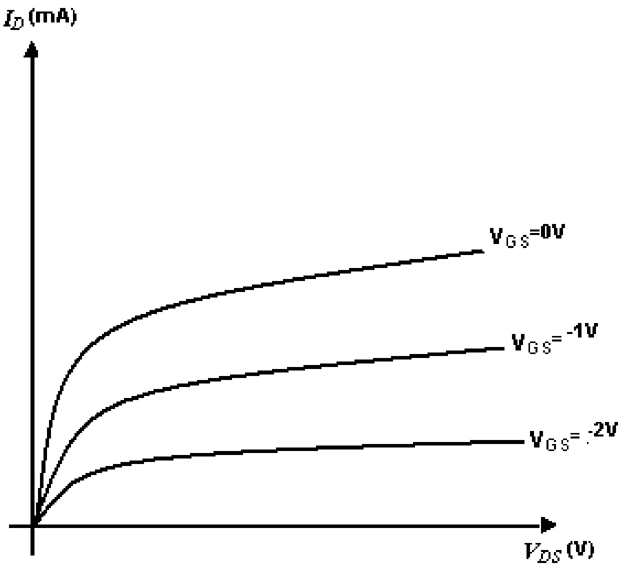
11. From transfer characteristics, calculate the value of transconductace (g_m) By using the formula

    $$G_m = \Delta I_D/\Delta V_{DS}$$

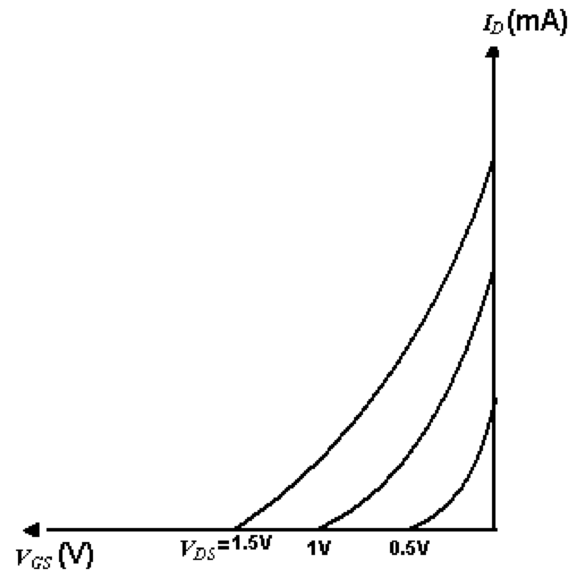
12. Amplification factor (μ) = dynamic resistance. Tran conductance $\mu = \Delta V_{DS}/\Delta V_{GS}$

Model Graph:

Drain Characteristics:



Transfer Characteristics:



Observations:

Drain characteristics:

S.NO	V_{GS}=0V		V_{GS}= - 1V		V_{GS}= - 2V	
	V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)

Transfer characteristics:

S.NO	V_{DS} =0.5V		V_{DS}=1V		V_{DS} =1.5V	
	V_{GS} (V)	I_D(mA)	V_{GS} (V)	I_D(mA)	V_{GS} (V)	I_D(mA)

<u>Calculations:</u>

At a suitable operating point, the parameters are calculated as follows:

1. Drain resistance, $rd \quad \frac{\Delta VBE}{\Delta IB}$ vith V_{GS} as constant = ________
2. Trans-conductance, $gm = \frac{\Delta ID}{\Delta VGS}$ h V_{DS} as constant = ________
3. Amplification factor, $\mu = \frac{\Delta VDS}{\Delta VGS}$ th I_D as constant = ________

These parameters are related by the equation $\mu = r_d\, g_m$

Precautions:

1. The three terminals of the FET must be care fully identified
2. Practically FET contains four terminals, which are called source, drain, Gate, substrate.
3. Source and case should be short circuited.
4. Voltages exceeding the ratings of the FET should not be applied.

Result :

1. The drain and transfer characteristics of a given FET are drawn
2. The dynamic resistance (r_d), amplification factor (μ) and Tran conductance (g_m) of the given FET are calculated.

VIVA QUESTIONS:

1. *What are the advantages of FET?*
2. *Different between FET and BJT?*
3. *Explain different regions of V-I characteristics of FET?*
4. *What are the applications of FET?*
5. *What are the types of FET?*
6. *Draw the symbol of FET.*
7. *What are the disadvantages of FET?*
8. *What are the parameters of FET?*

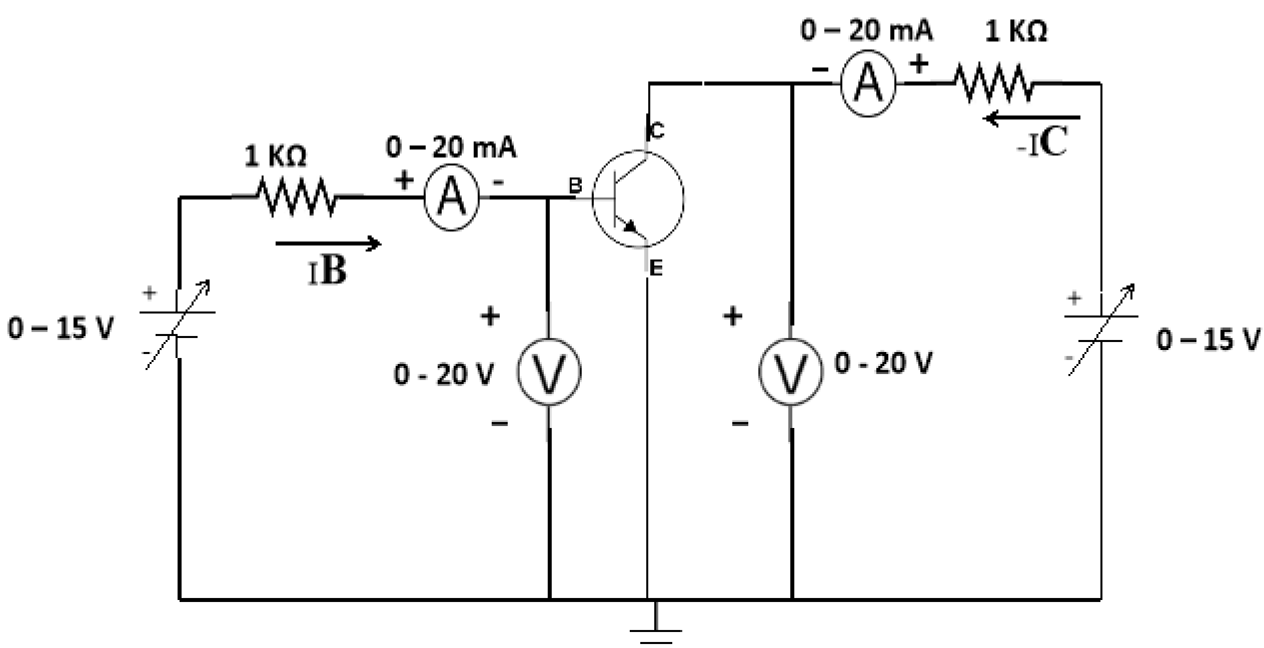
8. Measurement of *h*-parameters of CE configuration

Aim: To calculate the *h* -parameters of transistor in CE configuration.

Apparatus Required:

NAME	RANGE	TYPE	QUANTITY
REGULATED POWER SUPPLY (RPS)	0 – 15 V		2
AMMETER	0 – 20 mA		1
	0 – 200 µA		
VOLTMETER	0 – 20 V		1
TRANSISTOR		BC107 (NPN)	1
RESISTORS	100KΩ		1
	100 Ω		1
BREADBOARD			1
CONNECTING WIRES			SUFFICIENT

Circuit Diagram:-



THEORY:

Input characteristics: The two sets of characteristics are necessary to describe the behavior of the CE configuration one for input or base emitter circuit and other for the output or collector emitter circuit. In input characteristics the emitter base junction forward biased by a very small voltage V_{BB} where as collector base junction reverse biased by a very large voltage V_{CC}. The input characteristics are a plot of input current I_B V_s the input voltage V_{BE} for a range of values of output voltage V_{CE} . The following important points can be observed from these characteristics curves.

1. The characteristics resemble that of CE configuration.
2. Input resistance is high as I_B increases less rapidly with V_{BE}
3. The input resistance of the transistor is the ratio of change in base emitter voltage ΔV_{BE} to change in base current ΔI_B at constant collector emitter voltage (V_{CE}) i.e. Input resistance or input impedance $h_{ie} = \Delta V_{BE} / \Delta I_B$ at V_{CE} constant.

Output characteristics: A set of output characteristics or collector characteristics are a plot of out put current I_C V_S output voltage V_{CE} for a range of values of input current I_B .The following important points can be observed from these characteristics curves.

The transistor always operates in the active region. I.e. the collector current I_C increases with V_{CE} very slowly. For low values of the V_{CE} the I_C increases rapidly with a small increase in $V_{CE.}$ The transistor is said to be working in saturation region.

Output resistance is the ratio of change of collector emitter voltage $\Delta V_{CE,}$ to change in collector current ΔI_C with constant $I_{B.}$ Output resistance or Output impedance hoe = $\Delta V_{CE} / \Delta I_C$ at I_B constant.

Input Impedance $h_{ie} = \Delta V_{BE} / \Delta I_B$ at V_{CE} constant

Output impedance $h_{oe} = \Delta V_{CE} / \Delta I_C$ at I_B constant

Reverse Transfer Voltage Gain $h_{re} = \Delta V_{BE} / \Delta V_{CE}$ at I_B constant

Forward Transfer Current Gain $h_{fe} = \Delta I_C / \Delta I_B$ at constant V_{CE}

PROCEDURE:

1. Connect a transistor in CE configuration circuit for plotting its input and output characteristics.
2. Take a set of readings for the variations in I_B with V_{BE} at different fixed values of output voltage V_{CE} .
3. Plot the input characteristics of CE configuration from the above readings.
4. From the graph calculate the input resistance h_{ie} and reverse transfer ratio h_{re} by taking the slopes of the curves.
5. Take the family of readings for the variations of I_C with V_{CE} at different values of fixed I_B.
6. Plot the output characteristics from the above readings.
7. From the graphs calculate h_{fe} ands h_{oe} by taking the slope of the curves.

Tabular Forms

Input Characteristics:

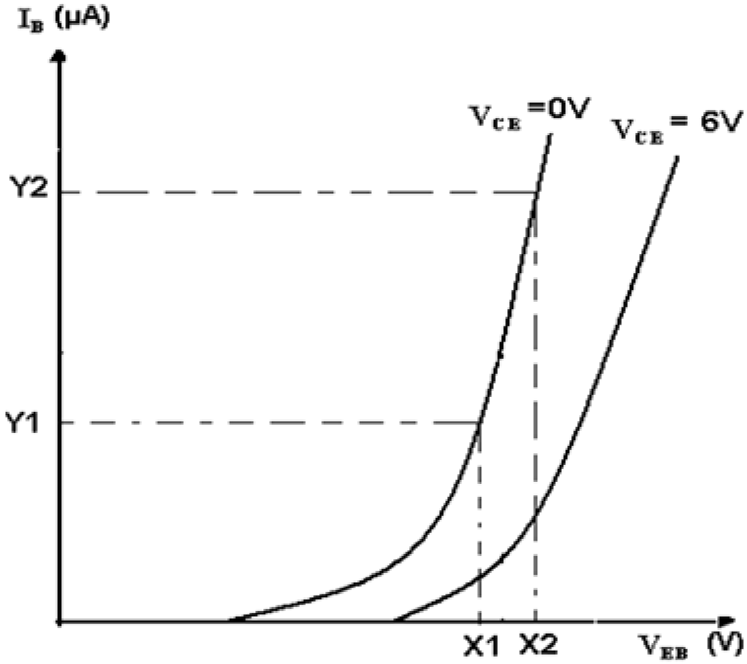
S.NO	V_{CE}=0V		V_{CE}=6V	
	V_{BE}(V)	I_B(μA)	V_{BE}(V)	I_B(μA)

Output Characteristics:

S.NO	I_B = 20 μA		I_B = 40 μA		I_B = 60 μA	
	V_{CE} (V)	I_C(mA)	V_{CE} (V)	I_C(mA)	V_{CE} (V)	I_C(mA)

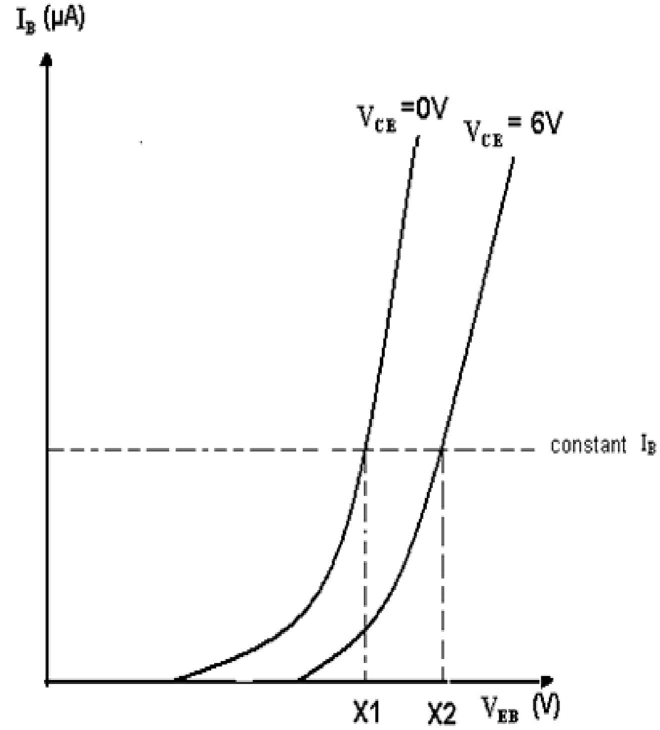
MODEL WAVEFORM:

Input Characteristics



hie = $\Delta V_{BE} / \Delta I_B$ at V_{CE} constant

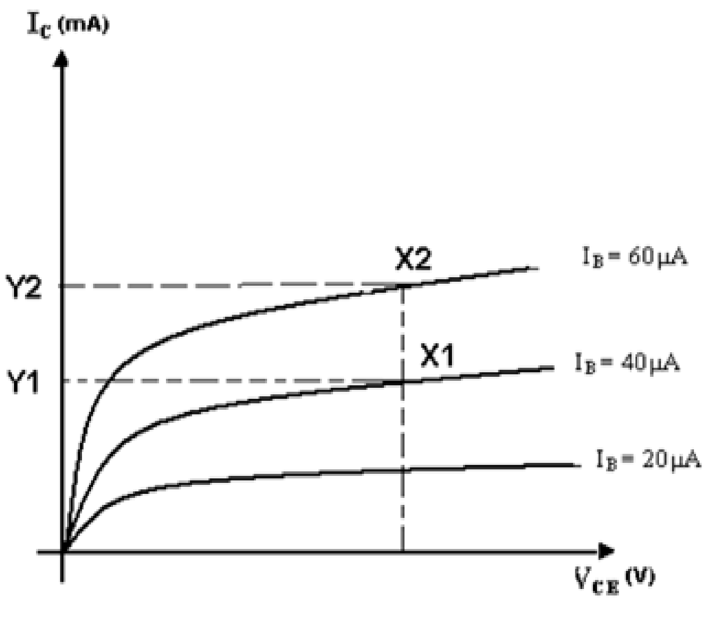
= (X2 - X1) / Y2 - Y1



hre = $\Delta V_{BE} / \Delta V_{CE}$ at I_B constant

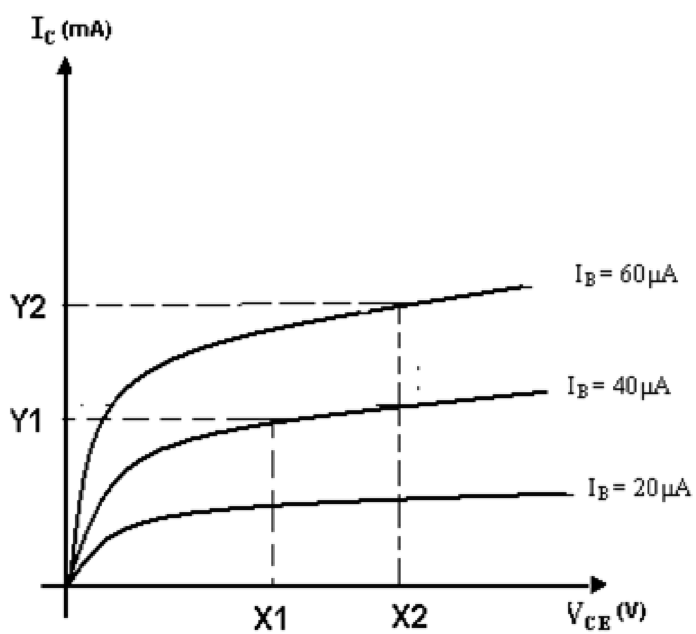
= (X2 - X1) / (V_{CE}=6V)-(V_{CE}=0V)

Output Characteristics



hfe = $\Delta I_C / \Delta I_B$ at constant V_{CE}

= Y2 - Y1 / (X2 - X1)



hoe = $\Delta V_{CE} / \Delta I_C$ at I_B constant

= Y2 - Y1 / (X2 - X1)

RESULT: The H-Parameters for a transistor in CE configuration are calculated from the input and output characteristics.

1. Input Impedance h_{ie} = _________
2. Reverse Transfer Voltage Gain h_{re} = _________
3. Forward Transfer Current Gain h_{fe} = _________
4. Output conductance h_{oe} = _________

***VIVA QUESTIONS*:**

1. *What are the h-parameters?*
2. *What are the limitations of h-parameters?*
3. *What are its applications?*
4. *Draw the Equivalent circuit diagram of H parameters?*
5. *Define H parameter?*
6. *What are tabular forms of H parameters monoculture of a transistor?*
7. *What is the general formula for input impedance?*
8. *What is the general formula for Current Gain?*
9. *What is the general formula for Voiltage gain?*

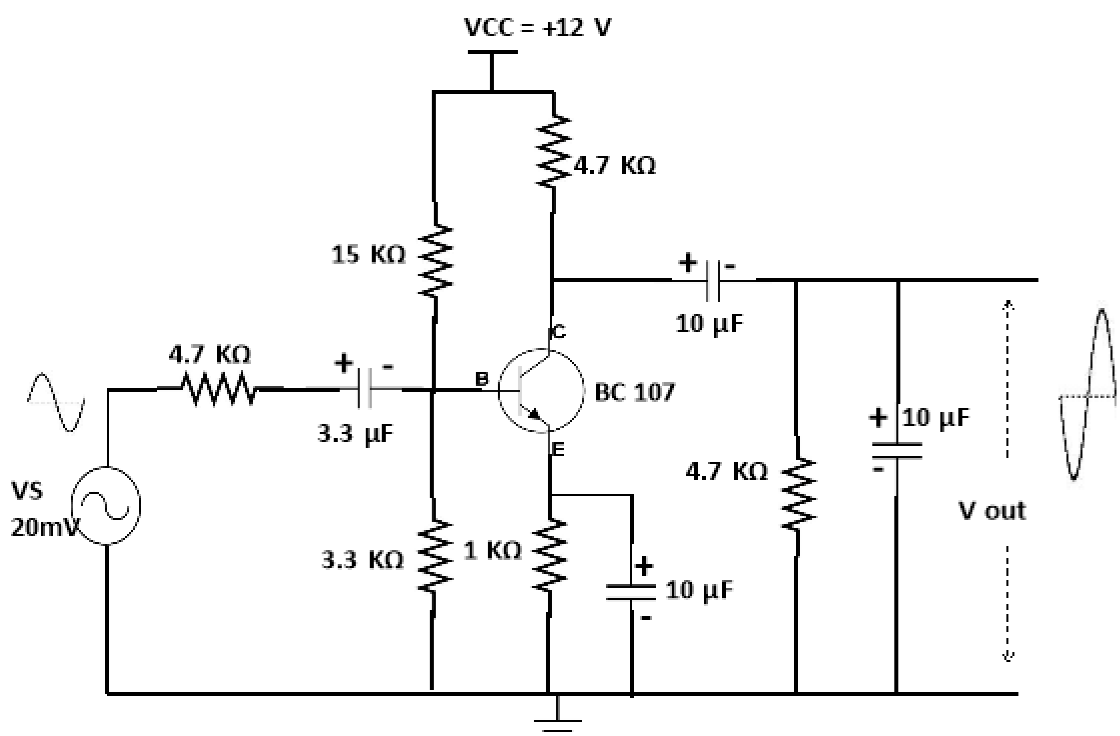
9. TRANSISTOR COMMON EMITTER AMPLIFIER

AIM: 1. To design and plot the frequency response of a CE amplifier and to find the 'Voltage gain' and 'Bandwidth' from the frequency response curve of the CE amplifier.

Apparatus Required:

NAME	RANGE	TYPE	QUANTITY
REGULATED POWER SUPPLY (RPS)	0 – 15 V		2
AMMETER	0 – 20 mA 0 – 200 µA		1
VOLTMETER	0 – 20 V		1
TRANSISTOR		BC107 (NPN)	1
RESISTORS	33KΩ, 3.3 KΩ, 1.5 KΩ, 1 KΩ, 330 Ω, 2.2 KΩ, 4.7 KΩ.		
CAPACITORS	3.3µF, 10 µF – 3 NO.		
CATHODE RAY OSCILLOSCOPE	0 – 20 MHZ	DUEL CHANNEL	1
FUNCTION GENERATOR			1
BREADBOARD			1
CONNECTING WIRES			SUFFICIENT

Circuit Diagram:-



THEORY:

The CE amplifier provides high gain &wide frequency response. The emitter lead is common to both input & output circuits and is grounded. The emitter-base circuit is forward biased. The collector current is controlled by the base current rather than emitter current. The input signal is applied to base terminal of the transistor and amplifier output is taken across collector terminal. A very small change in base current produces a much larger change in collector current. When +VE half-cycle is fed to the input circuit, it opposes the forward bias of the circuit which causes the collector current to decrease, it decreases the voltage more –VE. Thus when input cycle varies through a -VE half-cycle, increases the forward bias of the circuit, which causes the collector current to increases thus the output signal is common emitter amplifier is in out of phase with the input signal.

PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. Apply the input of 20mV peak-to-peak and 1 KHz frequency using Function Generator.
3. Measure the Output Voltage Vo (p-p) for various load resistors.
4. Tabulate the readings in the tabular form.
5. The voltage gain can be calculated by using the expression $\mathbf{A_v = (V_0/V_i)}$.
6. For plotting the frequency response the input voltage is kept Constant at 20mV peak-to-peak and the frequency is varied from 100Hz to 1MHz Using function generator
7. Note down the value of output voltage for each frequency.
8. All the readings are tabulated and voltage gain in dB is calculated by Using The expression

$$A_v = 20 \log_{10} (V_0/V_i)$$

9. A graph is drawn by taking frequency on x-axis and gain in dB on y-axis on Semi-log graph.

The band width of the amplifier is calculated from the graph using the expression,

$$\text{Bandwidth, } BW = f_2 - f_1$$

Where f_1 lower cut-off frequency of CE amplifier, and

Where f_2 upper cut-off frequency of CE amplifier

The bandwidth product of the amplifier is calculated using the expression

Gain Bandwidth product = 3-dBmidband gain X Bandwidth

OBSERVATIONS:

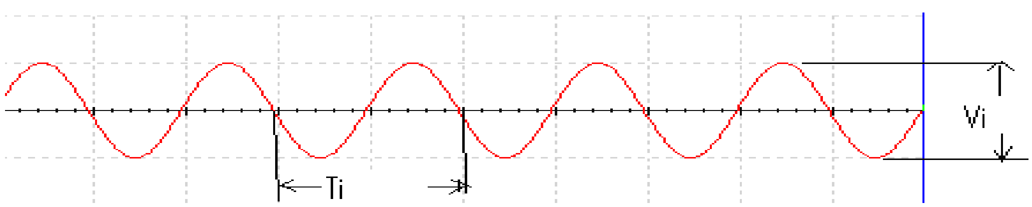
ONE PAGE

Frequency Response: Input voltage V_i = 20mV

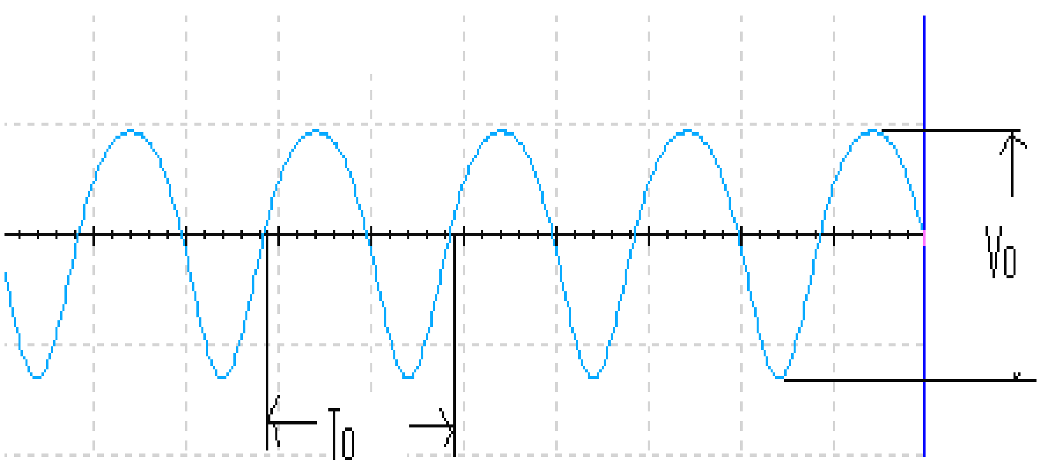
FREQUENCY (in Hz)	OUTPUT VOLTAGE (V_0) In volts	GAIN IN dB $A_v = 20 \log_{10} (V_0/V_i)$

MODELWAVE FORMS:

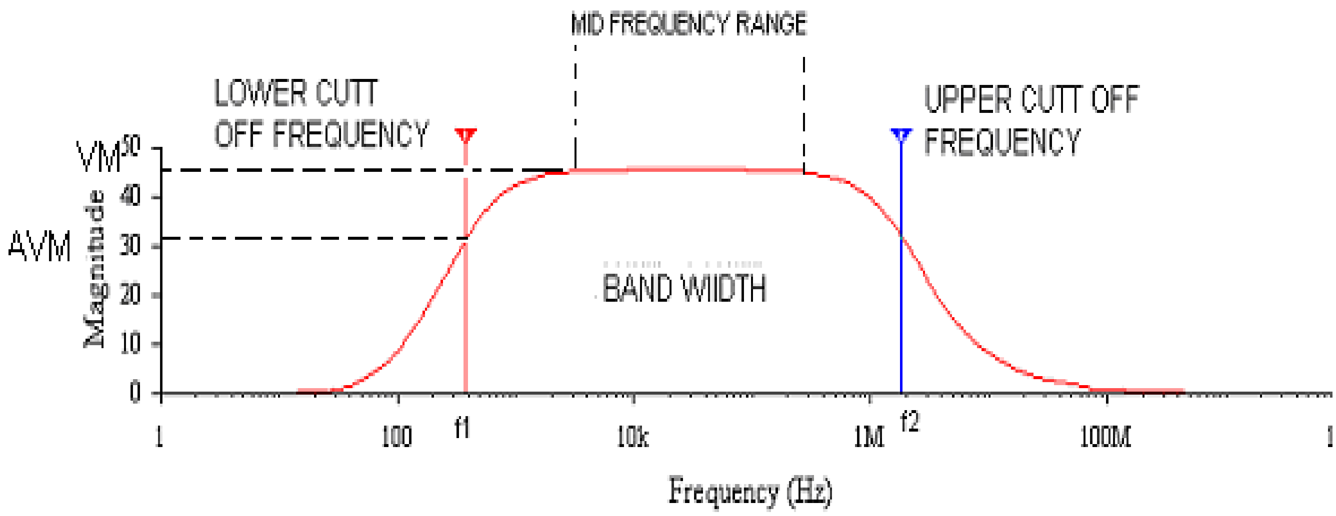
Input wave form



Output Wave Form



FREQUENCY RESPONSE



RESULT: The voltage gain and frequency response of the CE amplifier are obtained. Also gain bandwidth product of the amplifier is calculated.

VIVA QUESTIONS:

1. *What is phase difference between input and output waveforms of CE amplifier?*
2. *What type of biasing is used in the given circuit?*
3. *If the given transistor is replaced by a p-n-p, can we get output or not?*
4. *What is effect of emitter-bypass capacitor on frequency response?*
5. *What is the effect of coupling capacitor?*
6. *What is region of the transistor so that it is operated as an amplifier?*
7. *How does transistor acts as an amplifier?*
8. *Draw the h-parameter model of CE amplifier?*
9. *What type of transistor configuration is used in intermediate stages of a multistage amplifier?*
10. *What is Early effect?*

10. COMMON COLLECTOR AMPLIFIER

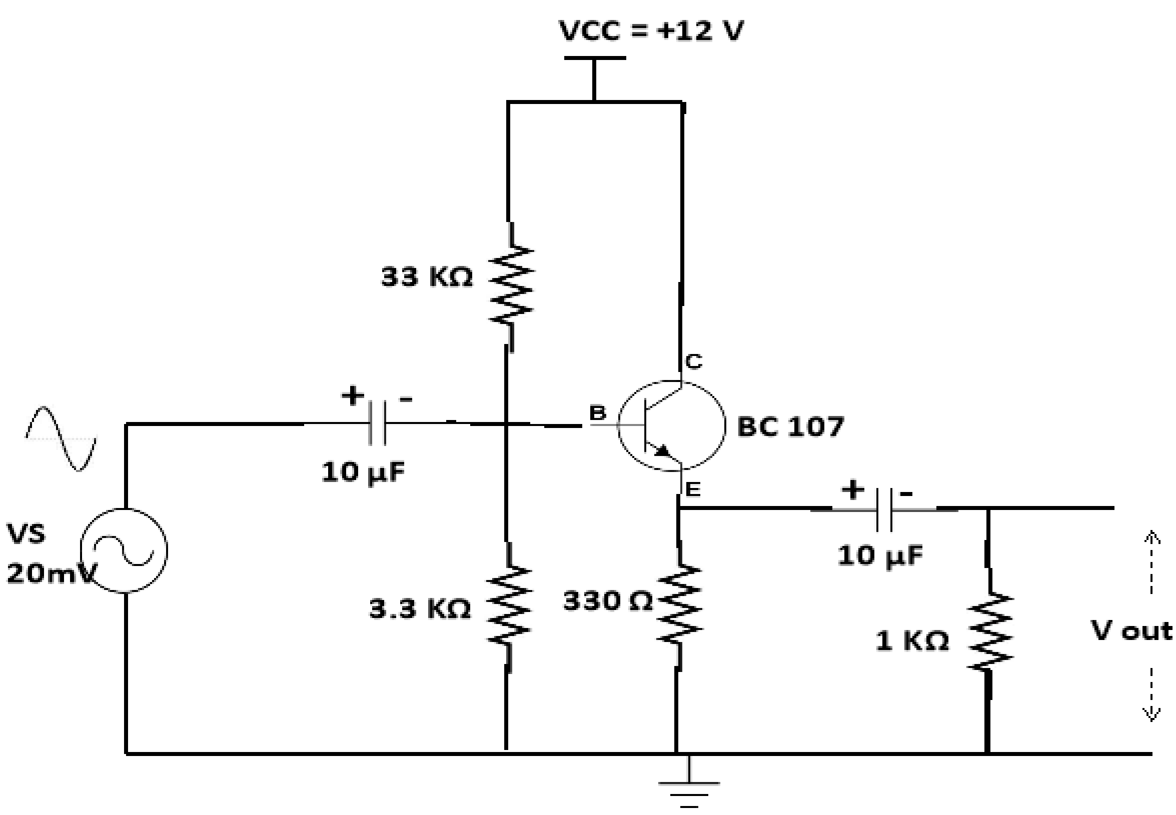
AIM: 1. To measure the voltage gain of a CC amplifier

2. To draw the frequency response of the CC amplifier

Apparatus Required:

NAME	RANGE	TYPE	QUANTITY
REGULATED POWER SUPPLY (RPS)	0 – 15 V		2
AMMETER	0 – 20 mA		1
	0 – 200 μA		
VOLTMETER	0 – 20 V		1
TRANSISTOR		BC107 (NPN)	1
RESISTORS	33KΩ, 3.3 KΩ, 1.5 KΩ, 1 KΩ, 330 Ω, 2.2 KΩ, 4.7 KΩ.		
CAPACITORS	10 μF		2
CATHODE RAY OSCILLOSCOPE	0 – 20 MHz	DUEL CHANNEL	1
FUNCTION GENERATOR			1
BREADBOARD			1
CONNECTING WIRES			SUFFICIENT

Circuit Diagram:-



THEORY:

In common-collector amplifier the input is given at the base and the output is taken at the emitter. In this amplifier, there is no phase inversion between input and output. The input impedance of the CC amplifier is very high and output impedance is low. The voltage gain is less than unity. Here the collector is at ac ground and the capacitors used must have a negligible reactance at the frequency of operation.

This amplifier is used for impedance matching and as a buffer amplifier. This circuit is also known as emitter follower.

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. For calculating the voltage gain the input voltage of 20mV peak-to-peak and 1 KHz frequency is applied and output voltage is taken for various load resistors.
3. The readings are tabulated.

The voltage gain calculated by using the expression,

$$A_v=V_0/V_i$$

4. For plotting the frequency response the input voltage is kept constant a 20mV peak-to- peak and the frequency is varied from 100Hzto 1MHz.
5. Note down the values of output voltage for each frequency.

All the readings are tabulated the voltage gain in dB is calculated by using the expression,

$$A_v=20\log 10(V0/V_i)$$

6. A graph is drawn by taking frequency on X-axis and gain in dB on y-axis on Semi-log graph sheet. The Bandwidth of the amplifier is calculated from the graph using the Expression,

$$\text{Bandwidth } BW=f_2-f_1$$

Where f_1 is lower cut-off frequency of CE amplifier

f_2 is upper cut-off frequency of CE amplifier

The gain Bandwidth product of the amplifier is calculated using the expression,

Gain -Bandwidth product=3-dB midband gain X Bandwidth

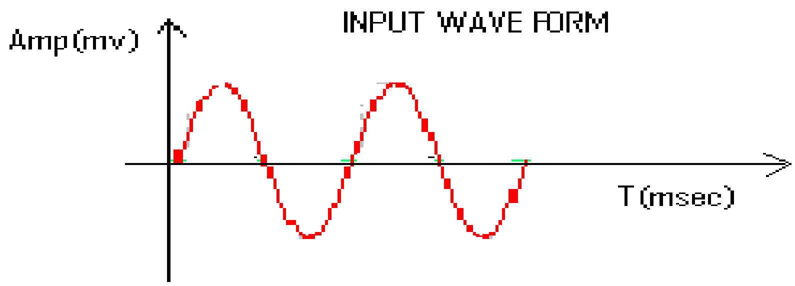
OBSERVATIONS:

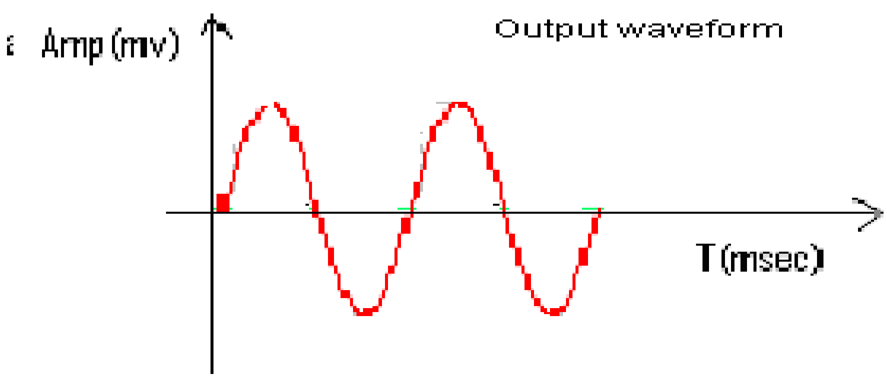
ONE PAGE

Frequency response: V_i=20mV

FREQUENCY(Hz)	OUTPUT VOLTAGE(V_0)	GAIN IN dB $A_v=20\log 10(V0/V_i)$

WAVEFORM:





PRECAUTIONS:

1. The input voltage must be kept constant while taking frequency response.
2. Proper biasing voltages should be applied.

RESULT:

The voltage gain and frequency response of the CC amplifier are obtained. Also gain Bandwidth product is calculated.

VIVA QUESTIONS:

1. *What are the applications of CC amplifier?*
2. *What is the voltage gain of CC amplifier?*
3. *What are the values of input and output impedances of the CC amplifier?*
4. *To which ground the collector terminal is connected in the circuit?*
5. *Identify the type of biasing used in the circuit?*
6. *Give the relation between α, β and γ.*
7. *Write the other name of CC amplifier?*
8. *What are the differences between CE,CB and CC?*
9. *When compared to CE, CC is not used for amplification. Justify your answer?*
10. *What is the phase relationship between input and output in CC?*

11. COMMON SOURCE FET AMPLIFIER

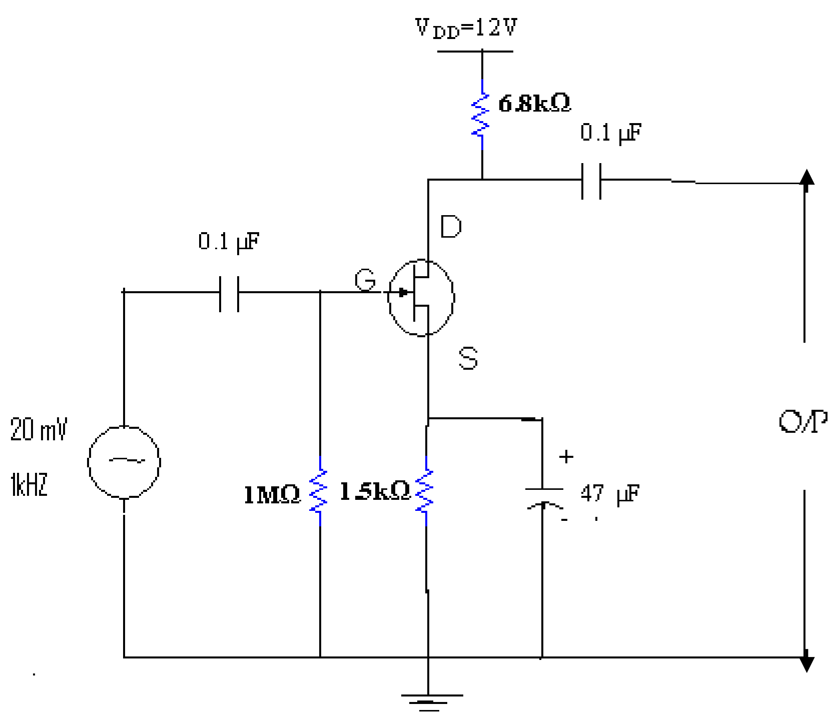
AIM: 1. To obtain the frequency response of the common source FET Amplifier

2. To find the Bandwidth.

Apparatus Required:

NAME	RANGE	TYPE	QUANTITY
REGULATED POWER SUPPLY (RPS)	0 – 15 V		2
AMMETER	0 – 20 mA		1
	0 – 200 μA		
VOLTMETER	0 – 20 V		1
FET N-CHANNEL		BFW11	1
RESISTORS	1.5 KΩ, 1MΩ, 6.8 KΩ.		
CAPACITORS	0.1 μF, 47 μF		
CATHODE RAY OSCILLOSCOPE	0 – 20 MHZ	DUEL CHANNEL	1
FUNCTION GENERATOR			1
BREADBOARD			1
CONNECTING WIRES			SUFFICIENT

Circuit Diagram:-



THEORY:

A field-effect transistor (FET) is a type of transistor commonly used for weak-signal amplification (for example, for amplifying wireless (signals). The device can amplify analog or digital signals. It can also switch DC or function as an oscillator. In the FET, current flows along a semiconductor path called the channel. At one end of the channel, there is an electrode called the source. At the other end of the channel, there is an electrode called the drain. The physical diameter of the channel is fixed, but its effective electrical diameter can be varied by the application of a voltage to a control electrode called the gate. Field-effect transistors exist in two major classifications. These are known as the junction FET (JFET) *and the* metal-oxide- semiconductor FET (MOSFET). The junction FET has a channel consisting of N-type semiconductor (N-channel) or P-type semiconductor (P-channel) material; the gate is made of the opposite semiconductor type. In P-type material, electric charges are carried mainly in the form of electron deficiencies called holes. In N-type material, the charge carriers are primarily electrons. In a JFET, the junction is the boundary between the channel and the gate.

Normally, this P-N junction is reverse-biased (a DC voltage is applied to it) so that no current flows between the channel and the gate. However, under some conditions there is a small current through the junction during part of the input signal cycle. The FET has some advantages and some disadvantages relative to the bipolar transistor. Field-effect transistors are preferred for weak-signal work, for example in wireless, communications and broadcast receivers. They are also preferred in circuits and systems requiring high impedance. The FET is not, in general, used for high-power amplification, such as is required in large wireless communications and broadcast transmitters.

Field-effect transistors are fabricated onto silicon integrated circuit (IC) chips. A single IC can contain many thousands of FETs, along with other components such as resistors, capacitors, and diodes.

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. A signal of 1 KHz frequency and 50mV peak-to-peak is applied at the
   Input of amplifier.
3. Output is taken at drain and gain is calculated by using the expression,

$$A_v=V_0/V_i$$

4. Voltage gain in dB is calculated by using the expression,

A_v=20log 10(V0/V_i)

5. Repeat the above steps for various input voltages.

6. Plot A_v $v_{s.}$ Frequency

7. The Bandwidth of the amplifier is calculated from the graph using the Expression,

Bandwidth **BW=f_2-f_1**

Where f_1 is lower 3 dB frequency

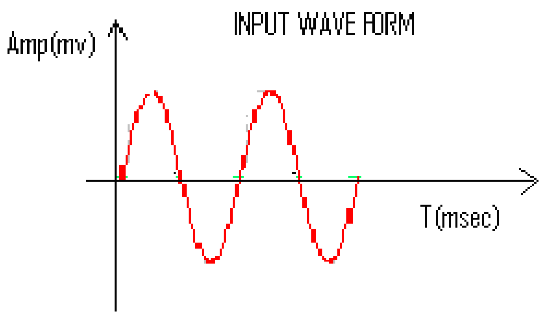
f_2 is upper 3 dB frequency

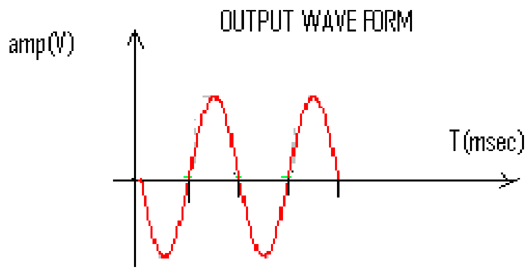
ONE PAGE

OBSERVATIONS:

S.NO	INPUT VOLTAGE(V_i)	OUTPUT VOLTAGE(V_0)	VOLTAGE GAIN A_v= (V0/V_i)

MODEL GRAPH:





PRECAUTIONS:

1. All the connections should be tight.
2. Transistor terminals must be identified properly

.

RESULT: The frequency response of the common source FET Amplifier and Bandwidth is obtained.

VIVA QUESTIONS

1. *What is the difference between FET and BJT?*
2. *FET is unipolar or bipolar?*
3. *Draw the symbol of FET?*
4. *What are the applications of FET?*
5. *FET is voltage controlled or current controlled?*
6. *Draw the equivalent circuit of common source FET amplifier?*
7. *What is the voltage gain of the FET amplifier?*
8. *What is the input impedance of FET amplifier?*
9. *What is the output impedance of FET amplifier?*
10. *What are the FET parameters?*
11. *What are the FET applications?*