ACADEMIC REGULATIONS COURSE STRUCTURE AND DETAILED SYLLABUS

M.Tech.

EMBEDDED SYSTEMS

(With effect from 2022-2023)

Choice Based Credit System (CBCS)

MR22 REGULATION

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY
(An Autonomous Institution under UGC, New Delhi)
Sheriguda(V), Ibrahimpatnam(M), Ranga Reddy Dist. – 501 510

Academic Regulations of M.Tech (Regular/Full Time) Programmes, 2022-23 (MR20) (CBCS)
(Effective for the students admitted into I year from the Academic Year 2022-23 and onwards)

The M. Tech. Degree of Sri Indu College of Engineering and Technology, Ibrahimpatnam shall be conferred on candidates who are admitted to the program and who fulfill all the requirements for the award of the Degree.

1.0 Post-Graduate Degree Programmes in Engineering & Technology (PGP in E & T) Sri Indu College of Engineering and Technology, Ibrahimpatnam offers **Two** Years (**Four** Semesters) full-time Master of Technology (M. Tech.) Degree programmes, under Choice Based Credit System (CBCS).

2.0 Eligibility for Admissions

2.1 Admission to the PGPs shall be made subject to eligibility, qualification and specializations prescribed by the University from time to time, for each specialization under each M.Tech programme.

2.2 Admission to the post graduate programme shall be made on the basis of either the merit rank or Percentile obtained by the qualified student in the relevant qualifying GATE Examination/ the merit rank obtained by the qualified student in an entrance test conducted by Telangana State Government (PGECET) for M.Tech. programmes / an entrance test conducted by JNTUH/ on the basis of any other exams approved by the University, subject to reservations as laid down by the Govt. from time to time.

2.3 The medium of instructions for all PG Programmes will be **ENGLISH** only.

3.0 M.Tech. Programme (PGP in E & T) Structure

3.1 The M.Tech. Programs in E & T of JNTUH are of Semester pattern, with **Four** Semesters consisting of **Two** academic years, each academic year having **Two** Semesters (First/Odd and Second/Even Semesters). Each Semester shall be of 22 weeks duration (inclusive of Examinations), with a minimum of 90 instructional days per Semester.

3.2 The two-year M.Tech. program consists of **68** credits and the student has to register for all **68** creditsand earn all **68** credits for the award of M.Tech. degree. There is **NO** exemption of credits in any case.

3.3 The student shall not take more than four academic years to fulfill all the academic requirements for the award of M.Tech. degree from the date of commencement of first year first semester, failing which thestudent shall forfeit the seat in M.Tech. programme.

3.4 **UGC/AICTE** specified definitions/descriptions are adopted appropriately for various terms and abbreviations used in these PG academic regulations, as listed below:

3.4.1 Semester Scheme

Each Semester shall have 'Continuous Internal Evaluation (CIE)' and 'Semester End Examination (SEE)'. Choice Based Credit System (CBCS) and Credit Based Semester System (CBSS) are taken as 'references' for the present set of Regulations. The terms 'SUBJECT' and 'COURSE' imply the same meaning here and refer to 'Theory Subject', or 'Lab Course', or 'Design/Drawing Subject', or 'Mini Project with Seminar', or 'Dissertation', as the case may be.

3.4.2 Credit Courses

All subjects/courses are to be registered by the student in a semester to earn credits which shall be assigned to each subject/course in an L: T: P: C (Lecture Periods: Tutorial Periods: Practical Periods:Credits) structure based on the following general pattern:

- One credit for one hour/week/semester for theory/lecture (L) courses
- One credit for two hours/ week/semester for laboratory/ practical (P) courses or tutorials (T)

Other student activities like study tour, guest lecture, conference/workshop participations, technical paper presentations and mandatory courses (***Non-credit Audit Courses***) will not carry any credits.

3.4.3 Subject Course Classification

All subjects/courses offered for the Post-Graduate Programme in E & T (M.Tech. Degree Programme) are broadly classified as follows. The University has followed in general the guidelines issued by AICTE/UGC.

S. No.	Broad Course Classification	Course Group/ Category	Course Description
1	Core Courses (CoC)	PC-Professional Core	Includes subjects related to the parent discipline/department/ branch of Engineering
		Dissertation	M.Tech. Project or PG Project or Major Project
		Mini Project with Seminar	Seminar based on core contents related to Parent Discipline/ Department/ Branch of Engineering
2	Elective Courses (EE)	PE-Professional Electives	Includes elective subjects related to the parent discipline/department/branch of Engineering
		OE-Open Electives	Elective subjects which include inter-disciplinary subjects or subjects in an area outside the parent discipline/department/ branch of Engineering
3	***Mandatory Courses***	--	***Non-Credit Audit Courses***

4.0 Course Registration

4.1 A 'Faculty Advisor or Counselor' shall be assigned to each specialization, who will advise on the Post Graduate Programme (PGP), its Course Structure and Curriculum, Choice/Option for Subjects/ Courses, based on his competence, progress, pre-requisites and interest.

4.2 The Academic Section of the College invites 'Registration Forms' from students within 15 days from the commencement of class work through 'ON-LINE SUBMISSIONS', ensuring 'DATE and TIME Stamping'. The ON-LINE Registration Requests for any 'CURRENT SEMESTER' shall be completed BEFORE the commencement of SEEs (Semester End Examinations) of the 'PRECEDING SEMESTER'.

4.3 A Student can apply for ON-LINE Registration, ONLY AFTER obtaining the 'WRITTEN APPROVAL' from his Faculty Advisor, which should be submitted to the College Academic Section through the Head of Department (a copy of it being retained with Head of Department, Faculty Advisor and the Student).

4.4 If the Student submits ambiguous choices or multiple options or erroneous entries during ON-LINE Registration for the Subject(s) / Course(s) under a given/ specified Course Group/ Category as listed in the Course Structure, only the first mentioned Subject/ Course in that Category will be taken into consideration.

4.5 Subject/ Course Options exercised through ON-LINE Registration are final and CANNOT be changed, nor can they be inter-changed; further, alternate choices also will not be considered. However, if the Subject/ Course that has already been listed for Registration by the University in a Semester could not be offered due to unforeseen or unexpected reasons, then the Student will be allowed to have alternate choice either for a new Subject, if it is offered, or for another existing Subject (subject to availability of seats). Such alternate arrangements will be made by the Head of Department, with due notification and time-framed schedule, within the FIRST WEEK from the commencement of Class-work for that Semester.

5.0 Attendance Requirements

The programmes are offered based on a unit system with each subject being considered a unit. Attendance is calculated separately for each subject.

5.1 Attendance in all classes (Lectures/Laboratories) is compulsory. The minimum required attendance in each theory subject (***also mandatory Audit Courses***) including the attendance of mid-term examination/Laboratory etc. is 75%. Two periods of attendance for each theory subject shall be considered, if the student appears for the mid-term examination of that subject. ***This attendance should also be included in the attendance uploaded every fortnight in the University Website. The attendance of mandatory Audit Courses should be uploaded separately to the University.*** A student shall not be permitted to appear for the Semester End Examinations (SEE), if his attendance is less than 75%.

5.2 A student's Seminar report and presentation on Mini Project shall be eligible for evaluation, only if he ensures a minimum of 75% of his attendance in Seminar presentation classes on Mini Project during that Semester.

5.3 **Condoning of shortage of attendance** (between 65% and 75%) up to a maximum of 10% (considering the days of attendance in sports, games, NCC, NSS activities and Medical grounds) in each subject (Theory/Lab/Mini Project with Seminar) of a semester shall be granted by the College Academic Committee on genuine reasons.

5.4 A prescribed fee per subject shall be payable for condoning shortage of attendance after getting the approval of College Academic Committee for the same. The College Academic Committee shall maintain relevant documents along with the request from the student.

5.5 Shortage of Attendance below 65% in any subject shall in **no case be condoned.**

5.6 A Student, whose shortage of attendance is not condoned in any Subject(s) (Theory/Lab/Mini Project with Seminar) in any Semester, is considered as 'Detained in that Subject(s), and is not eligible to write Semester End Examination(s) of such Subject(s), (in case of Mini Project with Seminar, his/her Mini Project with Seminar Report or Presentation are not eligible for evaluation) in that Semester; and he/she has to seek re-registration for those Subject(s) in subsequent Semesters, and attend the same as and when offered.

5.7 A student fulfills the attendance requirement in the present semester, shall not be eligible for readmission into the same class.

5.8 **a)** A student shall put in a minimum required attendance in at least **three theory subjects (excluding *mandatory (non-credit audit)* course)** in first Year I semester for promotion to first Year II Semester.

b) A student shall put in a minimum required attendance in at least **three theory subjects (excluding *mandatory (non-credit audit)* course)** in first Year II semester for promotion to second Year I Semester.

6.0 Academic Requirements

The following academic requirements must be satisfied, in addition to the attendance requirements mentioned in item no. 5. The performance of the candidate in each semester shall be evaluated subject- wise, with a maximum of 100 marks per subject / course (theory / practical), based on Internal Evaluation and Semester End Examination.

6.1 A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/course, if he secures not less than:

- 40% of Marks (24 out of 60 marks) in the Semester End Examination;
- 40% of Marks (Average of 10 out of 25 marks) from two mid-term examinations;
- 40% of Marks in the internal examinations (16 out of 40 marks allotted for CIE); and
- A minimum of 50% of marks in the sum total of CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together; in terms of Letter Grades this implies securing **'B'** Grade or above in a subject.

6.2 A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to Mini Project with seminar, if student secures not less than 50% marks (i.e. 50 out of 100 allotted marks). The student would be treated as failed, if student (i) does not submit a seminar report on Mini Project or does not make a presentation of the same before the evaluation committee as per schedule or (ii) secures less than 50% marks in Mini Project with seminar evaluation. The failed student shall reappear for the above evaluation when the notification for supplementary examination is issued.

6.3 A student shall register for all subjects for total of **68** credits as specified and listed in the course structure for the chosen specialization, put in the required attendance and fulfill the academic requirements for securing **68** credits obtaining a minimum of 'B' Grade or above in each subject, and all **68** credits securing Semester Grade Point Average **(SGPA) ≥ 6.0** (in each semester) and final Cumulative Grade Point Average **(CGPA)** (i.e., CGPA at the end of PGP**) ≥ 6.0**, and shall ***pass all the mandatory Audit Courses*** to complete the PGP successfully.

Note: (1) ***The SGPA will be computed and printed on the marks memo only if the candidate passes in all the subjects offered and gets minimum B grade in all the subjects.***

(2) ***CGPA is calculated only when the candidate passes in all the subjects offered in all these semesters***

6.4 Marks and Letter Grades obtained in all those subjects covering the above specified **68** credits alone shall be considered for the calculation of final CGPA, which will be indicated in the Grade Card /Marks Memo of second year second semester.

6.5 If a student registers for extra subject(s) (in the parent department or other departments/ branches of Engineering) other than those listed subjects totaling to **68** credits as specified in the course structure, the performance in extra subject(s) (although evaluated and graded using the same procedure as that of the required **68** credits) will not be considered while calculating the SGPA and CGPA. For such extra subject(s) registered, percentage of marks and Letter Grade alone will be indicated in the Grade Card/Marks Memo, as a performance measure, subject to completion of the attendance and academic requirements as stated in items 5 and 6.1 - 6.3.

6.6 When a student is detained due to shortage of attendance in any subject(s) in any semester, no Grade allotment will be made for such subject(s). However, he is eligible for re-registration of such subject(s) in the subsequent semester(s), as and when next offered, with the academic regulations of the batch into which he is re-registered, by paying the prescribed fees per subject. In all these re-registration cases, the student shall have to secure a fresh set of internal marks and Semester End Examination marks for performance evaluation in such subject(s), and SGPA/CGPA calculations.

6.7 A student eligible to appear for the Semester End Examination in any subject, but absent from it or failed (failing to secure 'B' Grade or above), may reappear for that subject at the supplementary examination as and when conducted. In such cases, his Internal Marks assessed earlier for that subject will be carried over, and added to the marks secured in the supplementary examination, for the purpose of evaluating his performance in that subject.

A Student who fails to earn **68** credits as per the specified course structure, and as indicated at within **four** academic years from the date of commencement of his first year first semester, shall f his seat in M.Tech. programme and his admission **shall stand cancelled.**

7.0 Evaluation - Distribution and Weightage of Marks

The performance of a student in each semester shall be evaluated subject- wise (irrespective of credits assigned) for a maximum of 100 marks.

7.1 The performance of a student in every subject/course (including practicals and Project) will be evaluated for 100 marks each, with 40 marks allotted for CIE (Continuous Internal Evaluation) and 60 marks for SEE (Semester End-Examination). The Continuous Internal Evaluation shall be made based on the average of the marks secured in the two Mid-Term Examinations conducted, first Mid-Term examinations in the middle of the Semester and second Mid-Term examinations

during the last weekof instruction.

7.2 In CIE, for theory subjects, during a semester, there shall be two mid-term examinations. Each Mid- Term examination consists of two parts i) **Part – A** for 10 marks, ii) **Part – B** for 15 marks with a totalduration of 2 hours as follows:

1. Mid-Term Examination for 25 marks:
   a. Part - A: Objective/quiz paper for 10 marks.
   b. Part – B: Descriptive paper for 15 marks.

The objective/quiz paper is set with multiple choice, fill-in the blanks and match the following type of questions for a total of 10 marks. The descriptive paper shall contain 5 full questions out of which, thestudent has to answer 3 questions, each carrying 5 marks. Student shall have to earn 40%, i.e 10 marks out of 25 marks from average of two mid-term examinations (I Mid-Term & II Mid-Term).

The remaining 15 marks of Continuous Internal Assessment (out of 40) are distributed as:

2. Assignment for 5 marks. (Average of 2 Assignments each for 5 marks)
3. Subject Viva-Voce/PPT/Poster Presentation/ Case Study on a topic in the concerned subject for 10 marks.

- The student has to get minimum of 40% of Marks in the internal examinations (16 out of 40 marks allotted for CIE).

While the first mid-term examination shall be conducted on 50% of the syllabus, the second mid-termexamination shall be conducted on the remaining 50% of the syllabus.

Five (5) marks are allocated for assignments (as specified by the subject teacher concerned). The firstassignment should be submitted before the conduct of the first mid-term examination, and the second assignment should be submitted before the conduct of the second mid-term examination. The average of the two assignments shall be taken as the final marks for assignment (for 5 marks).

Subject Viva-Voce/PPT/Poster Presentation/ Case Study on a topic in the concerned subject for 10 marks before II Mid-Term Examination.

The details of the end semester question paper pattern are as follows:

7.3 The Semester End Examinations (SEE), for theory subjects, will be conducted for 60 marks consistingof two parts viz. i) **Part- A** for 10 marks, ii) **Part - B** for 50 marks.

- Part-A is a compulsory question which consists of ten sub-questions from all units carrying equalmarks.
- Part-B consists of five questions (numbered from 2 to 6) carrying 10 marks each. Each of thesequestions is from each unit and may contain sub-questions. For each question there will be an "either" "or" choice, which means that there will be two questions from each unit and the student should answer either of the two questions.
- The duration of Semester End Examination is 3 hours.

7.4 For practical subjects there shall be a Continuous Internal Evaluation (CIE) during the semester for 40 marks and 60 marks for semester end examination. Out of the 40 marks for internal evaluation:

1. A write-up on day-to-day experiment in the laboratory (in terms of aim, components/procedure, expected outcome) which shall be evaluated for 10 marks
2. 10 marks for viva-voce (or) tutorial (or) case study (or) application (or) poster presentation of thecourse concerned.
3. Internal practical examination conducted by the laboratory teacher concerned shall be evaluatedfor 10 marks.
4. The remaining 10 marks are for Laboratory Project, which consists of the Design (or) Software / Hardware Model Presentation (or) App Development (or) Prototype Presentation submission which shall be evaluated after completion of laboratory course and before semester end practical examination.

The Semester End Examination shall be conducted with an external examiner and the laboratory teacher. The external examiner shall be appointed from the cluster / other colleges which will be decided by the examination branch of the University.

In the Semester End Examination, held for 3 hours, total 60 marks are divided and allocated as shownbelow:

1. 10 marks for write-up
2. 15 for experiment/program
3. 15 for evaluation of results
4. 10 marks for presentation on another experiment/program in the same laboratory course
5. 10 marks for viva-voce on concerned laboratory course

7.5 For conducting laboratory end examinations of all PG Programmes, one internal examiner and one external examiner are to be appointed by the Principal of the College and this is to be informed to theDirector of Evaluation within two weeks, before commencement of the lab end examinations. The external examiner should be selected from outside the College concerned but within the cluster. Noexternal examiner should be appointed from any other College in the same cluster/any other clusterwhich is run by the same Management.

7.6 There shall be Mini Project with Seminar during I year II semester for internal evaluation of 100 marks. The Departmental Academic Committee (DAC) will review the progress of the mini project during theseminar presentations and evaluate the same for 50 marks. Mini Project Viva Voce will be evaluatedby the DAC for another 50 marks before the semester end examinations. Student shall carryout the mini project in consultation with the mini project supervisor which may include critically reviewing the literature, project implementation and submit it to the department in the form of a report and shall make an oral presentation before the DAC consisting of Head of the Department, Mini Project supervisor and two other senior faculty members of the department. The student has to secure a minimum of 50% of marks in i) seminar presentation and ii) mini project viva voce, to be declared successful. If he fails toobtain the minimum marks, he has to reappear for the same as and when scheduled.

7.7 Every candidate shall be required to submit a dissertation on a topic approved by the Dissertation Review Committee.

7.8 A Dissertation Review Committee (DRC) shall be constituted with the Head of the Department as Chairperson, Dissertation Supervisor and one senior faculty member of the Department offering the M.Tech. programme.

7.9 Registration of Dissertation Work: A candidate is permitted to register for the Dissertation Work aftersatisfying the attendance requirement in all the subjects, both theory and laboratory.

7.10 After satisfying 7.9, a candidate must present in ***Dissertation Work Review - I***, in consultation with his Dissertation Supervisor, the title, objective and plan of action of his Dissertation work to the Dissertation Review Committee (DRC) for approval ***within four weeks*** from the commencement of **Second year First Semester**. Only after obtaining the approval of the DRC can the student initiate the Dissertation work.

7.11 If a candidate wishes to change his supervisor or topic of the Dissertation, he can do so with the approval of the DRC. However, the DRC shall examine whether or not the change of topic/supervisorleads to a major change of his initial plans of Dissertation proposal. If yes, his date of registration forthe project work starts from the date of change of Supervisor or topic as the case may be.

7.12 A candidate shall submit his Dissertation progress report in two stages at least with a gap of **three** months between them.

7.13 The work on the Dissertation shall be initiated at the beginning of the II year and the duration of the Dissertation is two semesters. A candidate is permitted to submit Dissertation Thesis only after successful completion of all theory and practical courses with the approval of DRC ***not***

earlier than 40 weeks from the date of approval of the Dissertation work. For the approval of DRC, the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the DRC.

7.14 ***The Dissertation Work Review - II*** in II Year I Semester carries 100 internal marks. Evaluation should be done by the DRC for 50 marks and the Supervisor will evaluate the work for the other 50 marks. The Supervisor and DRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain and progress of the Dissertation Work. A candidate has to secure a minimum of 50% of marks to be declared successful in Dissertation Work Review - II. If he fails to obtain the minimum required marks, he has to reappear for Dissertation Work Review - II as and when conducted.

7.15 ***The Dissertation Work Review - III*** in II Year II Sem. carries 100 internal marks. Evaluation should be done by the DRC for 50 marks and the Supervisor will evaluate it for the other 50 marks. The DRC will examine the overall progress of the Dissertation Work and decide whether or not the Dissertation is eligible for final submission. A candidate has to secure a minimum of 50% of marks to be declared successful in Dissertation Work Review - III. If he fails to obtain the required minimum marks, he has to reappear for Dissertation Work Review - III as and when conducted. For Dissertation Evaluation (Viva Voce) in II Year II Semester there are external marks of 100 and it is evaluated by the external examiner. The candidate has to secure a minimum of 50% marks in Dissertation Evaluation (Viva- Voce) examination.

7.16 Dissertation Work Reviews - II and III shall be conducted in phase I (Regular) and Phase II (Supplementary). Phase II will be conducted only for unsuccessful students in Phase I. The unsuccessful students in Dissertation Work Review - II (Phase II) shall reappear for it at the time of Dissertation Work Review - III (Phase I). These students shall reappear for Dissertation Work Review- III in the next academic year at the time of Dissertation Work Review - II only after completion of Dissertation Work Review - II, and then Dissertation Work Review - III follows. The unsuccessful students in Dissertation Work Review - III (Phase II) shall reappear for Dissertation Work Review - III in the next academic year only at the time of Dissertation Work Review - II (Phase I).

7.17 After approval from the DRC, a soft copy of the thesis should be submitted for ANTI-PLAGIARISM check and the plagiarism report should be submitted to the University and be included in the final thesis.The Thesis will be accepted for submission, if the similarity index is less than **30%**. If the similarity index has more than the required percentage, the student is advised to modify accordingly and re- submit the soft copy of the thesis after one month. The maximum number of re-submissions of thesis after plagiarism check is limited to ***TWO***. The candidate has to register for the Dissertation work and work for two semesters. After three attempts, the admission is liable to be cancelled. The college authorities are advised to make plagiarism check of every soft copy of theses before submissions.

7.18 Three copies of the Dissertation Thesis certified by the supervisor shall be submitted to the College/School/Institute, after submission of a research paper related to the Dissertation work in a UGC approved journal. A copy of the submitted research paper shall be attached to thesis.

7.19 The thesis shall be adjudicated by an external examiner selected by the University. For this, the Principal of the College/School/Institute shall submit a panel of **three** examiners from among the list of experts in the relevant specialization as submitted by the supervisor concerned and Head of the Department.

7.20 If the report of the external examiner is unsatisfactory, the candidate shall revise and resubmit the Thesis. If the report of the examiner is unsatisfactory again, the thesis shall be summarily rejected. Subsequent actions for such dissertations may be considered, only on the specific recommendations of the external examiner and /or Dissertation Review Committee. No further correspondence in this matter will be entertained, if there is no specific recommendation for resubmission.

7.21 If the report of the examiner is satisfactory, the Head of the Department shall coordinate and make arrangements for the conduct of Dissertation Viva-Voce examination. The Dissertation Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who adjudicated the Thesis. The candidate has to secure a minimum of 50% of marks in Dissertation Evaluation (Viva-Voce) examination.

7.22 If he fails to fulfill the requirements as specified in 7.21, he will reappear for the Dissertation Viva-Voce examination ***only after three months***. In the reappeared examination also, if he fails to fulfill the requirements, he will not be eligible for the award of the degree, unless he is asked to revise and resubmit his Dissertation Work by the board within a specified time period (within ***four*** years from the date of commencement of his first year first semester).

7.23 The Dissertation Viva-Voce External examination marks must be submitted to the University on the day of the examination.

7.24 For mandatory non-credit Audit courses, a student has to secure 40 marks out of 100 marks (i.e. 40% of the marks allotted) in the continuous internal evaluation for passing the subject/course. These marks should also be uploaded along with the internal marks of other subjects.

7.25 No marks or letter grades shall be allotted for mandatory non-credit Audit Courses. Only Pass/Fail shall be indicated in Grade Card.

8.0 Re-Admission/Re-Registration

8.1 Re-Admission for Discontinued Student

A student, who has discontinued the M.Tech. degree programme due to any reason whatsoever, may be considered for '**readmission**' into the same degree programme (with the same specialization) with the academic regulations of the batch into which he gets readmitted, with prior permission from the authorities concerned, subject to item 6.6.

8.2 If a student is detained in a subject (s) due to shortage of attendance in any semester, he may be permitted to **re-register** for the same subject(s) in the same category (core or elective group) or equivalent subject, if the same subject is not available, as suggested by the Board of Studies of that department, as and when offered in the subsequent semester(s), with the academic regulations of the batch into which he seeks re-registration, with prior permission from the authorities concerned, subject to item 3.2

8.3 A candidate shall be given one chance to re-register and attend the classes for a maximum of two subjects, if the internal marks secured by a candidate are less than 50% and failed in those subjects but fulfilled the attendance requirement. A candidate must re-register for failed subjects within four weeks of commencement of the class work and secure the required minimum attendance. In the event of the student taking this chance, his Continuous Internal Evaluation (internal) marks and Semester End Examination marks obtained in the previous attempt stand cancelled.

9.0 Examinations and Assessment - The Grading System

9.1 Grades will be awarded to indicate the performance of each student in each Theory Subject, or Lab/Practicals, or Mini Project with Seminar, Dissertation, etc., based on the percentage of marks obtained in CIE + SEE (Continuous Internal Evaluation + Semester End Examination, both taken together) as specified in Item 7 above, and a corresponding Letter Grade shall be given.

9.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be followed:

Marks Secured in a subject/Course ss Intervals)	**r Grade (UGC lelines)**	**le Points**
and above (□ 90%, ≤ 100%)	utstanding)	10
w 90% but not less than 80% %, <90%)	Excellent)	9
w 80% but not less than 70% %, <80%)	ery Good)	8
w 70% but not less than 60% %, <70%)	Good)	7
w 60% but not less than 50% %, <60%)	bove Average)	6
w 50% (< 50%)	AIL)	0
nt		**0**

9.3 A student obtaining **'F'** Grade in any Subject is deemed to have 'failed' and is required to reappear as 'Supplementary Candidate' for the Semester End Examination (SEE), as and when conducted. In such cases, his Internal Marks (CIE Marks) in those subjects will remain as obtained earlier.

9.4 If a student has not appeared for the examinations, '**Ab**' Grade will be allocated to him for any subject and shall be considered 'failed' and will be required to reappear as 'Supplementary Candidate' for the Semester End Examination (SEE), as and when conducted.

9.5 A Letter Grade does not imply any specific marks percentage; it is only the range of percentage of marks.

9.6 In general, a student shall not be permitted to repeat any Subject/ Course (s) only for the sake of 'Grade Improvement' or 'SGPA/ CGPA Improvement'.

9.7 A student earns Grade Point (GP) in each Subject/ Course, on the basis of the Letter Grade obtained by him in that Subject/ Course. The corresponding 'Credit Points' (CP) are computed by multiplying the Grade Point with Credits for that particular Subject/ Course.

Credit Points (CP) = Grade Point (GP) x Credits …. For a Course

9.8 The student passes the Subject/ Course only when he **gets GP ≥ 6 (B Grade or above).**

9.9 The Semester Grade Point Average (SGPA) is calculated by dividing the Sum of Credit Points (CP) secured from ALL Subjects/ Courses registered in a Semester, by the Total Number of Credits registered during that Semester. SGPA is rounded off to TWO Decimal Places. SGPA is thus computed as

$$\textbf{SGPA} = \{ \sum_{i=1}^{N} C_i G_i \} / \{ \sum_{i=1}^{N} C_i \} \textbf{ …. For each Semester,}$$

where 'i' is the Subject indicator index (taking into account all Subjects in a Semester), 'N' is the no. of Subjects 'REGISTERED' for the Semester (as specifically required and listed under the Course Structure of the parent Department), C_i is the no. of Credits allotted to the i^{th} Subject, and G_i represents the Grade Points (GP) corresponding to the Letter Grade awarded for that i^{th} Subject.

9.10 The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student over all Semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in ALL registered Courses in ALL Semesters, and the Total

Number of Credits registered in ALL the Semesters. CGPA is rounded off to TWO Decimal Places. CGPA is thus computed from the I Year Second Semester onwards, at the end of each Semester, as per the formula

$$\text{CGPA} = \{ \sum_{j=1}^{M} C_j G_j \} / \{ \sum_{j=1}^{M} C_j \}$$ **… for all S Semesters registered (ie., up to and inclusive of S Semesters, S ≥ 2),**

where 'M' is the TOTAL no. of Subjects (as specifically required and listed under the Course Structure of the parent Department) the Student has 'REGISTERED' for from the 1st Semester onwards upto and inclusive of the Semester S (obviously M > N), 'j' is the Subject indicator index (taking into account all Subjects from 1 to S Semesters), C_j is the no. of Credits allotted to the j^{th} Subject, and G_j represents the Grade Points (GP) corresponding to the Letter Grade awarded for that j^{th} Subject. After registration and completion of I Year I Semester however, the SGPA of that Semester itself may be taken as the CGPA, as there are no cumulative effects.

Illustration of calculation of SGPA

Course/Subject	Credits	Letter Grade	Grade points	Credit Points
Course 1	4	A	8	= 32
Course 2	4	O	10	= 40
Course 3	4	B	6	= 24
Course 4	3	B	6	= 18
Course 5	3	A+	9	= 27
Course 6	3	B	6	= 18
	21			159

SGPA = 159/21 = 7.57

Illustration of calculation of CGPA

Semester	Credits	SGPA	Credits * SGPA
Semester I	24	7	24*7 = 168
Semester II	24	6	24*6 = 144
Semester III	24	6.5	24*6.5 = 156
Semester IV	24	6	24*6 = 144
	96		612

CGPA = 612/96 = 6.37

10.0 Award of Degree and Class

10.1 If a student who registers for all the specified Subjects/ Courses as listed in the Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme (PGP), and secures the required number of **68** Credits (with CGPA 6.0), shall be declared to have 'QUALIFIED' for the award of the M.Tech. Degree in the chosen Branch of Engineering and Technology with the specialization that he was admitted into.

10.2 Award of Class

After a student has earned the requirements prescribed for the completion of the programme and is eligible for the award of M.Tech. Degree, he shall be placed in one of the following three classes based on the CGPA:

Class Awarded	CGPA
First Class with Distinction	≥ 7.75
First Class	6.75≤ CGPA < 7.75
Second Class	6.00≤ CGPA < 6.75

A student with final CGPA (at the end of the **PGP) < 6.00** shall not be eligible for the Award of Degree.

11.0 Withholding of Results

If the student has not paid the dues, if any, to the University or if any case of indiscipline is pending against him, the result and degree of the student will be withheld and he will not be allowed into the next semester.

12.0 General

12.1 **Credit**: A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (lecture or tutorial) or two hours ofpractical work/field work per week.

12.2 **Credit Point:** It is the product of grade point and number of credits for a course.

12.3 Wherever the words "he", "him", "his", occur in the regulations, they shall include "she", "her".

12.4 The academic regulation should be read as a whole for the purpose of any interpretation.

12.5 In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Universityis final.

12.6 The University may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by theUniversity.

*****

MALPRACTICES RULES
DISCIPLINARY ACTION FOR IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/ Improper conduct	*Punishment*
	If the candidate :	
1.(a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered a[g]ainst him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing,	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the University.
3.	Impersonates any other candidate in connection with the examination,	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case

4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from classwork and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6.	Refuses to obey the orders of the Chief Superintendent/Asst.– Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate

		is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examination and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and projectwork and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny,	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment.	

Note : Students are advised to read the above regulations thoroughly. Ignorance with regards to the regulations will not be excused

Frequently asked Questions and Answers about autonomy

1. Who grants Autonomy? UGC, Govt., AICTE or University

In case of Colleges affiliated to a university and where statutes for grant of autonomy are ready, it is the respective University that finally grants autonomy.

2. Shall SICET award its own Degrees?

No. Degree will be awarded by Jawaharlal Nehru Technological University, Hyderabad with a mention of the name SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY on the Degree Certificate.

3. What is the difference between a Deemed University and an Autonomy College?

A Deemed University is fully autonomous to the extent of awarding its own Degree. A Deemed University is usually a Non-Affiliating version of a University and has similar responsibilities like any University. An Autonomous College enjoys Academic Autonomy alone. The University to which an autonomous college is affiliated will have checks on the performance of the autonomous college.

4. How will the Foreign Universities or other stake – holders know that we are an Autonomous College?

Autonomous status, once declared, shall be accepted by all the stake holders. Foreign Universities and Indian Industries will know our status through our college website.

5. What is the change of Status for Students and Teachers if we become Autonomous?

An autonomous college carries a prestigious image. Autonomy is actually earned out of continued past efforts on academic performances, capability of self-governance and the kind of quality education we offer.

6. **Who will check whether the academic standard is maintained / improved after Autonomy? How will it be checked?**

There is a built in mechanism in the autonomous working for this purpose. An Internal Committee called Academic Programme Evaluation Committee is a Non – Statutory body, which will keep a watch on the academics and keep its reports and recommendations every year. In addition to Academic Council, the highest academic body also supervises the academic matters. At the end of three years, there is an external inspection by the University for this purpose. The standards of our question papers, the regularity of academic calendar, attendance of students, speed and transparency of result declaration and such other parameters are involved in this process.

7. **Will the students of SICET as an Autonomous College qualify for University Medals and Prizes for academic excellence?**

No, SICET has instituted its own awards, medals, etc. for the academic performance of the students. However for all other events like sports, cultural and co-curricular organized by the University the students shall qualify.

8. Can SICET have its own Convocation?

No, since the University awards the Degree the Convocation will be that of the University.

9. Can SICET give a provisional degree certificate?

Since the examinations are conducted by SICET and the results are also declared by SICET, the college sends a list of successful candidates with their final percentage of marks to the University. Therefore with the prior permission of the University the college will be entitled to give the provisional certificate.

10. Will Academic Autonomy make a positive impact on the Placements or Employability?

Certainly. The number of students qualifying for placement interviews is expected to improve, due to rigorous and repetitive classroom teaching and continuous assessment, besides the autonomous status is more responsive to the needs of the industry. As a result, there will be a lot of scope for industry oriented skill development built-in into the system. The graduates from an autonomous college will therefore represent better employability.

11. What is the proportion of Internal and External Assessment as an Autonomous College?

Presently, it is 40 % for internal assessment and 60 % for external assessment. As the autonomy matures the internal assessment component shall be increased at the cost of external assessment.

12. Will there be any Revaluation or Re-Examination System?

No, there will not be any Revaluation system or Re-examination.

13. How fast Syllabi can be and should be changed?

Autonomy allows us the freedom to change the syllabi as often as we need.

14. Will the Degree be awarded on the basis of only final year performance?

No. The Degree will be awarded basing on the performance in CGPA. With more than 6.0 points in CGPA from all the semesters.

15. Who takes Decisions on Academic matters?

The Academic Council of College is the top academic body and is responsible for all the academic decisions. Many decisions are also taken at the lower level like the BOS which are like Boards of Studies of the University.

16. What is the role of Examination committee?

The Exam Committee is responsible for the smooth conduct of inter and external examinations. All matters involving the conduct of examinations, spot valuations, tabulations, preparation of Memorandum of Marks etc fall within the duties of the Examination Committee.

17. Is there any mechanism for Grievance Redressal?

Yes, the college has grievance redressal committee, headed by a senior faculty member of the college.

18. How many attempts are permitted for obtaining a Degree?

All such matters are defined in Rules & Regulations.

19. Who declares the result?

The result declaration process is also defined. After tabulation work the entire result is reviewed by Result Processing Committee Nominee appointed by JNTUH. Any unusual deviations or gross level discrepancies are deliberated and removed. The entire result is discussed in the College Academic Council for its approval. The result is then declared on the college notice boards as well put on the web site of the college. It is eventually sent to the University.

20. What is our relationship with the Jawaharlal Nehru Technological University, Hyderabad?

We remain an affiliated college of the Jawaharlal Nehru Technological University, Hyderabad. The University has the right to nominate its members on the academic bodies of the college.

21. Shall we require University approval if we want to start any New Courses?

Yes, It is expected that approvals or such other matters from an autonomous college will receive priority.

22. Shall we get autonomy for PG and Doctoral Programmes also?

Yes, presently our PG programmes are also enjoying autonomous status.

23. How many exams will be there as an autonomous college?

This is defined in the Rules & Regulations.

******

SRI INDU COLLEGE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

Choice Based Credit System (CBCS)

REGULATIONS – MR22

M.Tech. (EMBEDDED SYSTEMS)

COURSE STRUCTURE AND SYLLABUS

I Year- I Semester **COURSE STRUCTURE**

Sl.No.	Course Code	Course Title	L	T	P	Credits
1	R22ES1501	Digital System Design with FPGAs	3	0	0	3
2	R22ES1502	System Design with Embedded Linux	3	0	0	3
3	**ProfessionalElective - I**					
	R22ES1503	CMOS VLSI Design	3	0	0	3
	R22ES1504	Pattern Recognition and Machine Learning				
	R22ES1505	Wireless Sensor Networks				
4	**ProfessionalElective - II**					
	R22ES1506	Communications Buses & Interfaces	3	0	0	3
	R22ES1507	Advanced Computer Architecture				
	R22ES1508	CMOS Analog IC Design				
5	R22ES1601	Digital system Design with FPGAs Lab	0	0	4	2
6	R22ES1602	System Design with Embedded Linux Lab	0	0	4	2
7	R22ES1509	Research Methodology & IPR	2	0	0	2
8	**Audit Course – I**		2	0	0	0
	R22ES1701	English for Research Paper Writing				
	R22ES1702	Disaster Management				
	R22ES1703	Value Education				
		Total	**16**	**0**	**8**	**18**

I Year- II Semester **COURSE STRUCTURE**

Sl.No.	Course Code	Course Title	L	T	P	Credits
1	R22ES1510	ARM Microcontrollers	3	0	0	3
2	R22ES1511	Digital Control Systems	3	0	0	3
3	**ProfessionalElective - III**		3	0	0	3
	R22ES1512	IoT Architectures and System Design				
	R22ES1513	Design for Testability				
	R22ES1514	SoC Design				
4	**ProfessionalElective - IV**		3	0	0	3
	R22ES1515	Hardware and Software Co-Design				
	R22ES1516	Secure Networks				
	R22ES1517	Physical Design Automation				
5	R22ES1603	ARM Microcontrollers Lab	0	0	4	2
6	R22ES1604	Advanced Digital Signal Processing Lab	0	0	4	2
7	R22ES1605	Seminar	0	0	4	2
8	**Audit Course – II**		2	0	0	0
	R22ES1704	Constitution of India				
	R22ES1705	Pedagogy Studies				
	R22ES1706	Stress Management by yoga				
		Total	**14**	**0**	**12**	**18**

SRI INDU COLLEGE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

Choice Based Credit System (CBCS)

REGULATIONS – MR22

M.Tech. (EMBEDDED SYSTEMS)

COURSE STRUCTURE AND SYLLABUS

II Year- I Semester **COURSE STRUCTURE**

Sl.No.	Course Code	Course Title	L	T	P	Credits
1	**ProfessionalElective - V**		3	0	0	3
	R22ES1518	Embedded Networks				
	R22ES1519	CMOS Mixed Signal Design				
	R22ES1520	Human -Machine Interface				
2	**Open Elective**		3	0	0	3
	R22ES1521	Business Analytics				
	R22ES1522	Industrial Safety				
	R22ES1523	Operations Research				
	R22ES1524	Cost Management of Engineering Projects				
	R22ES1525	Composite Materials				
3	R22ES1606	Dissertation Work Review - II	0	0	12	6
		Total	**6**	**0**	**12**	**12**

II Year- II Semester **COURSE STRUCTURE**

Sl.No.	Course Code	Course Title	L	T	P	Credits
1	R22ES1607	Dissertation Work Review - III	0	0	12	6
2	R22ES1608	Dissertation Viva-Voce	0	0	28	14
		Total	**0**	**0**	**40**	**20**

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – I Semester

L	T	P	C
3	0	0	3

(R22ES1501) DIGITAL SYSTEM DESIGN WITH FPGAS

Course Objectives:

1. To provide extended knowledge of digital logic circuits in the form of state model approach.
2. To provide an overview of system design approach using programmable logic devices.
3. To provide and understand of fault models and test methods.
4. To get exposed to the various architectural features of CPLDS and FPGAS.
5. To learn the methods and techniques of CPLD & FPGA design with EDA tools.
6. To expose software tools used for design process with the help of case studies.

Course Outcomes:

1. To exposes the design approaches using FPGAs.
2. To provide in depth understanding of Fault models.
3. To understands test pattern generation techniques for fault detection.
4. To design fault diagnosis in sequential circuits.
5. To provide understanding in the design of flow using case studies.

UNIT - I

Programmable Logic Devices: The concept of programmable Logic Devices, SPLDs, PAL devices, PLA devices, GAL devices, CPLD-Architecture, FPGAs-FPGA technology, architecture, virtex CLB and slice, FPGA Programming Technologies, Xilinx XC2000, XC3000, XC4000 Architectures, Actel ACT1, ACT2 and ACT3 Architectures. [TEXTBOOK-1]

UNIT - II

Analysis and derivation of clocked sequential circuits with state graphs and tables: A sequential parity checker, Analysis by signal tracing and timing charts-state tables and graphs-general models for sequential circuits, Design of a sequence detector, More Complex design problems, Guidelines for construction of state graphs, serial data conversion, Alphanumeric state graph notation. Need and Design stratagies for multi-clock sequential circuits. [TEXTBOOK-2]

UNIT - III

Sequential circuit Design: Design procedure for sequential circuits-design example, Code converter, Design of Iterative circuits, Design of a comparator, Controller (FSM) – Metastability, Synchronization, FSM Issues, Pipelining resources sharing, Sequential circuit design using FPGAs, Simulation and testing of Sequential circuits, Overview of computer Aided Design. [TEXTBOOK-2]

UNIT - IV

Fault Modeling and Test Pattern Generation: Logic Fault Model, Fault detection & redundancy, Fault equivalence and fault location, Fault dominance, Single stuck at fault model, multiple Stuck at Fault models, Bridging Fault model.

Fault diagnosis of combinational circuits by conventional methods, path sensitization techniques, Boolean difference method, KOHAVI algorithm, Test algorithms-D algorithm, Random testing, transition count testing, signature analysis and test bridging faults. [TEXTBOOK-3 & Ref.1]

UNIT - V

Fault Diagnosis in sequential circuits: Circuit Test Approach, Transition check Approach, State identification and fault detection experiment, Machine identification, Design of fault detection experiment. [Ref.3]

TEXT BOOKS

1. Digital Electronics and design with VHDL- Volnei A. Pedroni, Elsevier publications.
2. Fundamentals of Logic Design-Charles H.Roth, Jr. -5th Ed., Cengage Learning.
3. Digital Circuits and Logic Design-Samuel C. LEE, PHI, 2008.

REFERENCE BOOKS

1. Logic Design Theory-N.N. Biswas, PHI.
2. Digital System Design using programmable logic devices- Parag K. Lala, BS publications.
3. Switching and Finite Automata Theory - Zvi Kohavi & Niraj K. Jha, 3rd Edition, Cambridge, 2010.

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – I Semester

L	T	P	C
3	0	0	3

(R22ES1502) SYSTEM DESIGN WITH EMBEDDED LINUX

Course Objectives:

1. To know the difference between Embedded Linux and Desktop Linux
2. To understand the kernel concepts of Embedded Linux
3. To learn the debugging, writing, profile applications and drivers in embedded Linux.

Course Outcomes: At the end of this course, students will be able to

1. Familiarity of the embedded Linux development model.
2. Write, debug, and profile applications and drivers in embedded Linux.
3. Create Linux BSP for a hardware platform

UNIT- I

Introduction to Real Time Operating Systems: Characteristics of RTOS, Tasks Specifications and types, Real-Time Scheduling Algorithms, Concurrency, Inter-process Communication and Synchronization mechanisms, Priority Inversion, Inheritance and Ceiling. Embedded Linux Vs Desktop Linux, Embedded Linux Distributions, System calls, Static and dynamic libraries, Cross toolchains

UNIT- II

Embedded Linux Architecture, Kernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and Networking subsystem, IPC, User space, Start-up sequence

UNIT- III

Board Support Package Embedded Storage: MTD, Architecture, Drivers, Embedded File System Embedded Device Drivers: Communication between user space and kernel space drivers, Character and Block Device Drivers, Interrupt handling, Kernel modules
Embedded Drivers: Serial, Ethernet, I2 C, USB, Timer, Kernel Modules

UNIT- IV

Porting Applications Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux

UNIT- V

Building and Debugging: Bootloaders, Kernel, Root file system, Device Tree

TEXT BOOKS:

1. Chris Simmonds, “Mastering Embedded Linux Programming” - Second Edition, PACKTPublications Limited.
2. Karim Yaghmour, “Building Embedded Linux Systems”, O'Reilly & Associates
3. P Raghvan, Amol Lad, Sriram Neelakandan, “Embedded Linux System Design andDevelopment”, Auerbach Publications

REFERENCE BOOKS:

1. Christopher Hallinan, “Embedded Linux Primer: A Practical Real-World Approach”, PrenticeHall, 2nd Edition, 2010.
2. Derek Molloy, “Exploring Beagle Bone: Tools and Techniques for Building with EmbeddedLinux”, Wiley, 1st Edition, 2014

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – I Semester

L	T	P	C
3	0	0	3

ProfessionalElective - I
(R22ES1503) CMOS VLSI DESIGN

Course Objectives:

1. To understand the concepts of MOS Design and transient response
2. To know the design of combinational MOS logic circuits
3. To know the design of sequential MOS logic circuits
4. To understand the dynamic logic and also memory designing

Course Outcomes: Students will be able to:

1. Design of combinational MOS logic and sequential MOS logic circuits
2. Design of different Memories using MOS transistors
3. Design a circuits based on dynamic logic
4. Use CMOS transmission gates in various applications

UNIT – I : MOS Design:

Pseudo NMOS logic- Inverter, Inverter threshold voltage, output high voltage, Output lowvoltage, gain at gate threshold voltage, transient response, rise time, fall time, pseudo NMOS logic gates, transistor equivalency, CMOS inverter logic.

UNIT – II: Combinational MOS logic circuits:

MOS logic circuits with NMOS loads, Primitive CMOS logic gates- NOR and NAND gates, Complex logic circuits design- realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full-adder, CMOS transmission gates, designing with transmission gates.

UNIT – III: Sequential MOS logic circuits:

Behavior of bistable elements, SR Latch, Clocked Latch and Flip-flop circuits, CMOS D Latch and edge triggered flip-flop.

UNIT – IV: Dynamic Logic Circuits:

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, high performance dynamic CMOS circuits.

UNIT – V: Semiconductor Memories:

Types, RAM array Organization, DRAM- types, operation, leakage currentsin DRAM cell and refresh operation, SRAM - operation, leakage currents in SRAM cells, Flash memory-NOR flash and NAND flash.

TEXT BOOKS:

1. Digital Integrated Circuit Design- Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuit Analysis and Design – Sung Mo Kang, YusufLeblebici,TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective- Ming Bo Lin,CRC Press, 2011.
2. Digital Integrated Circuits: A Designs Perspective -Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – I Semester

L	T	P	C
3	0	0	3

ProfessionalElective - I

(R22ES1504) PATTERN RECOGNITION AND MACHINE LEARNING

Course Objectives:

1. The student will be able to understand the mathematical formulation of patterns.
2. To study the various linear models.
3. Understand the basic classifiers.
4. Can able to distinguish different models.

Course Outcomes: On completion of this course student will be able to

1. Familiar the basics of pattern classes and functionality.
2. Construct the various linear models.
3. Use the different kernel methods.
4. Design the Markov and Mixed models.

UNIT-I

Introduction to Pattern recognition: Mathematical Formulation and Basic Functional Equation, Reduction of Dimensionality, Experiments in Pattern Classification, Backward Procedure for Both Feature Ordering- and Pattern Classification, Suboptimal Sequential Pattern Recognition, Nonparametric Design of Sequential Pattern Classifiers, Analysis of Optimal Performance and a Multiclass Generalization

UNIT-II

Linear Models: Linear Basis Function Models -Maximum likelihood and least squares, Geometry of least squares , Sequential learning, Regularized least squares, Multiple outputs , The Bias-Variance Decomposition, Bayesian Linear Regression -Parameter distribution, Predictive, Equivalent, Bayesian Model Comparison, Probabilistic Generative Models-Continuous inputs, Maximum likelihood solution, Discrete features, Exponential family, Probabilistic Discriminative Models -Fixed basis functions, Logistic regression, Iterative reweighted least squares, Multiclass logistic regression, Probit regression, Canonical link functions

UNIT-III

Kernel Methods: Constructing Kernels, Radial Basis Function Networks - Nadaraya-Watson model, Gaussian Processes -Linear regression revisited, Gaussian processes for regression, Learning the hyper parameters, Automatic relevance determination, Gaussian processes for classification, Laplace approximation, Connection to neural networks, Sparse Kernel Machines- Maximum Margin Classifiers, Overlapping class distributions, Relation to logistic regression, Multiclass SVMs, SVMs for regression, Computational learning theory, Relevance Vector Machines- RVM for regression, Analysis of sparsity, RVM for classification

UNIT-IV

Graphical Models: Bayesian Networks, Example: Polynomial regression, Generative models, Discrete variables, Linear-Gaussian models, Conditional Independence- Three example graphs, D-separation, Markov Random Fields -Conditional independence properties, Factorization properties, Illustration: Image de-noising, Relation to directed graphs, Inference in Graphical Models- Inference on a chain, Trees, Factor graphs, The sum-product algorithm, The max-sum algorithm, Exact inference in generalgraphs, Loopy belief propagation, Learning the graph structure.

UNIT-V

Mixture Models and EM algorithm: K-means Clustering-Image segmentation and compression, Mixtures of Gaussians-Maximum likelihood, EM for Gaussian mixtures, An Alternative View of EM-Gaussian mixtures revisited, Relation to K-means, Mixtures of Bernoulli distributions, EM for Bayesian linear regression, The EM Algorithm in General, Combining Models- Tree-based Models, Conditional Mixture Models- Mixtures of linear regression models, Mixtures of logistic models, Mixtures of experts.

TEXT BOOKS:

1. Sequential methods in Pattern Recognition and Machine Learning-K.S.Fu, Academic Press, volume no.52.
2. Pattern Recognition and Machine Learning- C. Bishop-Springer,2006.

REFERENCE BOOKS:

1. Pattern Classification- Richard o. Duda, Peter E. hart, David G. Stork, John Wiley& Sons, 2nd Ed., 2001.
2. The elements of Statistical Learning- Trevor Hastie, Robert Tibshirani, Jerome H. Friedman, Springer, 2nd Ed., 2009.

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – I Semester

L	T	P	C
3	0	0	3

ProfessionalElective - I

(R22ES1505) WIRELESS SENSOR NETWORKS

Course Objectives

1. To acquire the knowledge about various architectures and applications of Sensor Networks
2. To understand issues, challenges and emerging technologies for wireless sensor networks
3. To learn about various routing protocols and MAC Protocols
4. To understand various data gathering and data dissemination methods
5. To Study about design principals, node architectures, hardware and software required for implementation of wireless sensor networks.

Course Outcomes: Upon completion of the course, the student will be able to:

1. Analyze and compare various architectures of Wireless Sensor Networks
2. Understand Design issues and challenges in wireless sensor networks
3. Analyze and compare various data gathering and data dissemination methods.
4. Design, Simulate and Compare the performance of various routing and MAC protocol

UNIT -I:

Introduction to Sensor Networks, unique constraints and challenges, Advantage of Sensor Networks, Applications of Sensor Networks, Types of wireless sensor networks

UNIT –II

Mobile Ad-hoc Networks (MANETs) and Wireless Sensor Networks, Enabling technologies for WirelessSensor Networks. Issues and challenges in wireless sensor networks

UNIT –III

Routing protocols, MAC protocols: Classification of MAC Protocols, S-MAC Protocol, B-MAC protocol,IEEE 802.15.4 standard and ZigBee

UNIT -IV

Dissemination protocol for large sensor network. Data dissemination, data gathering, and data fusion; Quality of a sensor network; Real-time traffic support and security protocols.

UNIT -V

Design Principles for WSNs, Gateway Concepts Need for gateway, WSN to Internet Communication, and Internet to WSN Communication. Single-node architecture, Hardware components & design constraints, Operating systems and execution environments, introduction to TinyOS and nesC.

TEXT BOOKS:

1. Ad-Hoc Wireless Sensor Networks- C. Siva Ram Murthy,B. S. Manoj, Pearson
2. Principles of Wireless Networks – Kaveh Pah Laven and P. Krishna Murthy, 2002, PE

REFERENCE BOOKS:

1. Wireless Digital Communications – Kamilo Feher, 1999, PHI.
2. Wireless Communications-Andrea Goldsmith, 2005 Cambridge University Press.
3. Mobile Cellular Communication – Gottapu Sasibhushana Rao, Pearson Education, 2012.
4. Wireless Communication and Networking – William Stallings, 2003, PHI.

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – I Semester

L	T	P	C
3	0	0	3

ProfessionalElective - II

(R22ES1506) COMMUNICATIONS BUSES & INTERFACES

Course Objectives:

1. To know how to select the suitable Buses for different applications
2. To know the architecture of CAN and applications
3. To understand the use of PCIe, USB etc.,
4. To know the serial communication protocol

Course Outcomes: At the end of the course, students will be able to:

1. Select a particular serial bus suitable for a particular application.
2. Develop APIs for configuration, reading and writing data onto serial bus.
3. Design and develop peripherals that can be interfaced to desired serial bus.

UNIT - I

Serial Busses - Physical interface, Data and Control signals, features, limitations and applications of RS232, RS485, I2C, SPI

UNIT - II

CAN - Architecture, Data transmission, Layers, Frame formats, applications

UNIT - III

PCIe - Revisions, Configuration space, Hardware protocols, applications

UNIT - IV

USB - Transfer types, enumeration, Descriptor types and contents, Device driver

UNIT - V

Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fiber optic and copper cable

TEXT BOOKS:

1. Jan Axelson, “Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems”, Lakeview Research, 2nd Edition
2. Jan Axelson, “USB Complete”, Penram Publications
3. Mike Jackson, Ravi Budruk, “PCI Express Technology”, Mindshare Press
4. Wilfried Voss, “A Comprehensible Guide to Controller Area Network”, Copperhill MediaCorporation, 2nd Edition, 2005.
5. Serial Front Panel Draft Standard VITA 17.1 –200x
6. Technical references onwww.can-cia.org, http://www.pcisig.com/www.pcisig.com, http://www.usb.org/www.usb.org

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – I Semester

L	T	P	C
3	0	0	3

ProfessionalElective - II

(R22ES1507) ADVANCED COMPUTER ARCHITECTURE

Course Objectives:

1. To understand the fundamental of computer design
2. To know the pipelines and parallelism concepts
3. To know the issues in interconnect networks

Course Outcomes: At the end of the course, students will be able to:

1. Familiarize the instruction set, memory addressing of Computer
2. Handle the issues in pipelining and parallelism
3. Familiarize the practical issues in inter network

UNIT - I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT - II

Pipelines: Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT - III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT - IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT - V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOK:

1. John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rdEdition, Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti, “Modern Processor Design: Fundamentals of Super Scalar Processors”, 2002, Beta Edition, McGraw-Hill
2. Kai Hwang, Faye A.Brigs., “Computer Architecture and Parallel Processing”, Mc Graw Hill.
3. DezsoSima, Terence Fountain, Peter Kacsuk, “Advanced Computer Architecture - A Design Space Approach”, Pearson Education.

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – I Semester

L	T	P	C
3	0	0	3

ProfessionalElective - II

(R22ES1508) CMOS ANALOG IC DESIGN

Course Objectives: Analog circuits play a very crucial role in all electronic systems and due to continued miniaturization, many of the analog blocks are not getting realized in CMOS technology.

1. To understand most important building blocks of all CMOS analog Ics.
2. To study the basic principle of operation, the circuit choices and the tradeoffs involved intheMOS transistor level design common to all analog CMOS ICs.
3. To understand specific design issues related to single and multistage voltage,current anddifferential amplifiers, their output and impedance issues, bandwidth, feedback and stability.
4. To understand the design of differential amplifiers, current amplifiers and OP AMPs.

Course Outcomes: After studying the course, each student is expected to be able to

1. Design basic building blocks of CMOS analog ICs.
2. Carry out the design of single and two stage operational amplifiers and voltage references.
3. Determine the device dimensions of each MOSFETs involved.
4. Design various amplifiers like differential, current and operational amplifiers.

UNIT – I : MOS Devices and Modeling

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small- Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT- II: Analog CMOS Sub-Circuits

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors- Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT – III: CMOS Amplifiers

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT – IV: CMOS Operational Amplifiers

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps,Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques ofOP Amp.

UNIT – V: Comparators

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, OxfordUniversityPress, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – I Semester

L	T	P	C
0	0	4	2

(R22ES1601) DIGITAL SYSTEM DESIGN WITH FPGAs LAB

Part –I:

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of Full Adder, Serial Binary Adder, Multi Precession Adder, CarryLook Ahead Adder.
3. Design of Combinational circuit using Decoders.
4. Design of Combinational circuit using encoder (without and with parity).
5. Design of Combinational circuit using multiplexer.
6. Design of 4 bit binary to gray converter using MUX or Decoders.
7. Design of Multiplexer/ Demultiplexer, comparator in all 3 styles.
8. Modelling of an Edge triggered and Level triggered FFs : D, SR, JK
9. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
10. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel inSerial out and Parallel in Parallel Out using different FFs.
11. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
12. Design of 4- Bit Multiplier, Divider.
13. Design of ALU to Perform – ADD, SUB, AND-OR, 1’s and 2’s Compliment,
14. Implementing the above designs on FPGA kits.

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – I Semester

L	T	P	C
0	0	4	2

(R22ES1602) SYSTEM DESIGN WITH EMBEDDED LINUX LAB

List of Experiments:

1. **Functional Testing Of Devices:** Flashing the OS on to the device into a stable functional state by porting desktop environment with necessary packages.
2. **Exporting Display On To Other Systems:** Making use of available laptop/desktop displays as a display for the device using SSH client & X11 display server.
3. **GPIO Programming:** Programming of available GPIO pins of the corresponding device using native programming language. Interfacing of I/O devices like LED/Switch etc., and testing the functionality.
4. **Interfacing Chronos eZ430:** Chronos device is a programmable texas instruments watch which can be used for multiple purposes like PPT control, Mouse operations etc., Exploit the features of the device by interfacing with devices.
5. **ON/OFF Control Based On Light Intensity:** Using the light sensors, monitor the surroundinglight intensity & automatically turn ON/OFF the high intensity LED's by taking some pre-definedthreshold light intensity value.
6. **Battery Voltage Range Indicator:** Monitor the voltage level of the battery and indicating the same using multiple LED's (for ex: for 3V battery and 3 led's, turn on 3 led's for 2-3V, 2 led's for1-2V, 1 led for 0.1-1V & turn off all for 0V)
7. **Dice Game Simulation:** Instead of using the conventional dice, generate a random value similar to dice value and display the same using a 16X2 LCD. A possible extension could be toprovide the user with option of selecting single or double dice game.
8. **Displaying RSS News Feed On Display Interface:** Displaying the RSS news feed headlines on a LCD display connected to device. This can be adapted to other websites like twitter or other information websites. Python can be used to acquire data from the internet.
9. **Porting Openwrt To the Device:** Attempt to use the device while connecting to a wifi network using a USB dongle and at the same time providing a wireless access point to the dongle.
10. **Hosting a website on Board:** Building and hosting a simple website(static/dynamic) on the device and make it accessible online. There is a need to install server (eg: Apache) and thereby host the website.
11. **Webcam Server:** Interfacing the regular usb webcam with the device and turn it into fully functional IP webcam & test the functionality.
12. **FM Transmission:** Transforming the device into a regular fm transmitter capable of transmitting audio at desired frequency (generally 88-108 Mhz)

Note: Devices mentioned in the above lists include Arduino, Raspbery Pi, Beaglebone

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – I Semester

L	T	P	C
2	0	0	2

(R22ES1509) RESEARCH METHODOLOGY & IPR

Course Objectives:

- To understand the research problem
- To know the literature studies, plagiarism and ethics
- To get the knowledge about technical writing
- To analyze the nature of intellectual property rights and new developments
- To know the patent rights

Course Outcomes: At the end of this course, students will be able to

1. Understand research problem formulation.
2. Analyze research related information
3. Follow research ethics
4. Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
5. Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
6. Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT- I:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem.
Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT- II:

Effective literature studies approaches, analysis, Plagiarism, Research ethics

UNIT- III:

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT- IV:

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT- V:

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

REFERENCE BOOKS:

1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
3. Mayall, "Industrial Design", McGraw Hill, 1992.
4. Niebel, "Product Design", McGraw Hill, 1974.
5. Asimov, "Introduction to Design", Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
7. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – I Semester

L	T	P	C
2	0	0	0

AUDIT COURSE – I

(R22ES1701) ENGLISH FOR RESEARCH PAPER WRITING

Course objectives: Students will be able to:

- Understand that how to improve your writing skills and level of readability
- Learn about what to write in each section
- Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission

UNIT-I:

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT-II:

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction

UNIT-III:

Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT-IV:

key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature,

UNIT-V:

skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions. useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

TEXT BOOKS/ REFERENCES:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book.
4. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – I Semester

L	T	P	C
2	0	0	0

AUDIT COURSE – I
(R22ES1702) DISASTER MANAGEMENT

Course Objectives: Students will be able to

- learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- critically understand the strengths and weaknesses of disaster management approaches,
- planning and programming in different countries, particularly their home country or the countries they work in

UNIT-I:

Introduction:

Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Disaster Prone Areas in India:

Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

UNIT-II:

Repercussions of Disasters and Hazards:

Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT-III:

Disaster Preparedness and Management:

Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT-IV:

Risk Assessment Disaster Risk:

Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT-V:

Disaster Mitigation:

Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

TEXT BOOKS/ REFERENCES:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company.
2. Sahni, Pardeep Et. Al. (Eds.)," Disaster Mitigation Experiences and Reflections", Prentice Hall of India, New Delhi.
3. Goel S. L., Disaster Administration and Management Text and Case Studies", Deep &Deep Publication Pvt. Ltd., New Delhi.

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – I Semester

L	T	P	C
2	0	0	0

AUDIT COURSE – I
(R22ES1703) VALUE EDUCATION

Course Objectives: Students will be able to

- Understand value of education and self- development
- Imbibe good values in students
- Let the should know about the importance of character

Course outcomes: Students will be able to

- Knowledge of self-development
- Learn the importance of Human values
- Developing the overall personality

UNIT-I:

Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements

UNIT-II:

Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline

UNIT-III:

Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline, Punctuality, Love and Kindness.

UNIT-IV:

Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature

UNIT-V:

Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation, Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively

TEXT BOOKS/ REFERENCES:

1. Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – II Semester

L	T	P	C
3	0	0	3

(R22ES1510) ARM MICROCONTROLLERS

Course Objectives:

1. Explore the architecture and instruction set of ARM processor.
2. To provide a comprehensive understanding of various programs of ARM Processors.
3. Learn the programming on ARM Cortex M.

Course Outcomes: After completing this course the student will be able to:

1. Explore the selection criteria of ARM processors by understanding the functional level trade offissues.
2. Explore the ARM development towards the functional capabilities.
3. Work with ASM level program using the instruction set.
4. Programming the ARM Cortex M.

UNIT - I

ARM Embedded Systems: RISC design philosophy, ARM design philosophy, Embedded system hardware, Embedded system software.

ARM Processor Fundamentals: Registers, Current Program Status Register, Pipeline, Exceptions, Interrupts and Vector Table, Core Extensions, Architecture Revisions, ARM Processor Families.

Architecture of ARM Processors: Introduction to the architecture, Programmer's model- operation modes and states, registers, special registers, floating point registers, Behaviour of the application program status register(APSR)-Integer status flags, Q status flag, GE bits, Memory system-Memory system features, memory map, stack memory, memory protection unit (MPU), Exceptions and Interrupts-what are exceptions, nested vectored interrupt controller(NVIC), vector table, Fault handling, System control block (SCB), Debug, Reset and reset sequence.

UNIT - II

Introduction to the Arm Instruction Set: Data processing instructions, branch instructions, load-store instructions, software interrupt instructions, program status register instructions, loading constants, ARMv5E extensions, Conditional execution.

Introduction to the Thumb Instruction Set: Thumb Register Usage, ARM-Thumb Interworking, Other Branch Instructions, Data Processing Instructions, Single-Register Load-Store Instructions, Multiple-Register Load-Store Instructions, Stack Instructions, Software Interrupt Instruction.

UNIT - III

Technical Details of ARM Cortex M Processors General information about Cortex-M3 and cortex M4 processors-Processor type, processor architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors- Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility.

UNIT - IV

Instruction SET of ARM Cortex M Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set, Cortex-M4-specific instructions, Barrel shifter, Accessing special instructions and special registers in Programming.

UNIT -V

Floating Point Operations About Floating Point Data,Cortex-M4 Floating Point Unit (FPU)- overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU- > FPCAR, FPU->FPDSCR, FPU->MVFR0, FPU->MVFR1. ARM Cortex-M4 and DSP Applications: DSP on a microcontroller, Dot Product example, writing optimized DSP code for the CortexM4-Biquad filter, Fast Fourier transform, FIR filter.

TEXT BOOKS:

1. Andrew N. SLOSS, Dominic SYMES, Chris WRIGHT- ARM System Developer's Guide Designing and Optimizing System Software, Elsevier Publications, 2004.
2. Joseph Yiu, The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors by Elsevier Publications, 3rd Ed.,

REFERENCE BOOKS:

1. Steve Furber - Arm System on Chip Architectures –Edison Wesley, 2000.
2. David Seal - ARM Architecture Reference Manual, Edison Wesley, 2000.

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – II Semester

L	T	P	C
3	0	0	3

(R22ES1511) DIGITAL CONTROL SYSTEMS

Course Objectives:

1. To understand the fundamentals of digital control systems representations, z-transforms
2. To understand analysis of discrete complex domain: Z-Transforms
3. To understand the concepts of state variables analysis for discrete LTIV systems.
4. To understand the concepts of controllability and observability of discrete time systems
5. To get exposed the design aspects of controllers and for discrete time systems
6. To understand the concepts of the stability for discrete LTIV systems
7. To understand the design aspects of observers for discrete time systems.

Course Outcomes: At the end of this course, students will demonstrate the ability to

1. Obtain discrete representation of LTI systems.
2. Find the state space analysis of discrete time systems.
3. Test and analyze the controllability and observability for discrete time systems
4. Analyze stability of discrete time systems using various methods
5. Design and analyze digital controllers.
6. Design state feedback controllers and observers.

UNIT- I: REPRESENTATION OF DISCRETE TIME SYSTEMS

Basics of Digital Control Systems. Discrete representation of continuous systems. Sample and hold circuit. Mathematical Modeling of sample and hold circuit. Effects of Sampling and Quantization. Choice of sampling frequency. ZOH equivalent.

Z-Transforms, Mapping from s-plane to z plane, Properties of Z-Transforms and Inverse Z Transforms. Pulse Transfer function: Pulse transfer function of closed loop systems. Solution of Discrete time systems. Time response of discrete time system, Steady State errors.

UNIT- II: DISCRETE TIME STATE SPACE ANALYSIS

State space representation of discrete time systems, Conversion of pulse transfer function to state space models and vice-versa, Solving discrete time state space equations, State Transition Matrix, Pulse Transfer Function Matrix. Discretization of continuous time state space equations. Concept of Controllability, stabilizability, observability, reachability – Controllability and observability tests. Effect of pole zero cancellation on the controllability & observability.

UNIT- III: STABILITY ANALYSIS OF DISCRETE TIME SYSTEM

Concept of stability in z-domain, Stability analysis discrete time system: by Jury test, using bilinear transformation.Stability Analysis of discrete time systems using Lyapunov methods.

UNIT- IV: DESIGN OF DIGITAL CONTROL SYSTEM BY CONVENTIONAL METHODS

Design and realization of digital PID Controller, Design of discrete time controllers with bilinear transformation,Design of digital control system with dead beat response, Practical issues with dead beat response design.

UNIT-V: DESIGN STATE FEEDBACK CONTROLLERS AND OBSERVERS

Design of discrete state feedback controllers through pole placement, Design of Discrete Observer for LTI System:Design of full order and reduced observers, Design of observer-based controllers.

TEXT BOOKS:

1. K. Ogata, "Digital Control Engineering", Prentice Hall, Englewood Cliffs, 1995.
2. M. Gopal, "Digital Control Engineering", Wiley Eastern, 1988.
3. V, I, George and C. P. Kurian, Digital Control Systems, CENGAGE Learning, 2012

REFERENCE BOOKS:

1. G. F. Franklin, J. D. Powell and M. L. Workman, "Digital Control of Dynamic Systems", Addison-Wesley,1998.
2. B.C. Kuo, "Digital Control System", Holt, Rinehart and Winston, 1980.

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – II Semester

L	T	P	C
3	0	0	3

Professional Elective - III

(R22ES1512) IOT ARCHITECTURES AND SYSTEM DESIGN

Course Objectives

1. To Know the definition and basic concepts of IoT
2. Learn the interfacing the IoT and M2M
3. To understand the Architecture of IoT

Course Outcomes: Students will be able to:

1. Integrate the sensors and actuator depending on the applications
2. Interface the IoT and M2M with value chains
3. Write Python programming for Arduino, Raspberry Pi devices
4. Design IoT based systems such as Agricultural IoT, Vehicular IoT etc.,

UNIT - I

IoT introduction: Introduction and definition of IoT, Evolution of IoT, IoT growth, Application areas of IoT, Characteristics of IoT, IoT stack, Enabling technologies, IoT levels, IoT sensing and actuation, Sensing types, Actuator types.

UNIT - II

IoT and M2M: M2M to IoT – A Basic Perspective– Introduction, Differences and similarities between M2M and IoT, SDN and NFV for IoT.M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT, The international driven global value chain and global information monopolies.

UNIT - III

IoT Hands-on: Introduction to Arduino Programming, Integration of Sensors and Actuators with Arduino. Introduction to Python programming, Introduction to Raspberry Pi, Interfacing Raspberry Pi with basic peripherals, Implementation of IoT with Raspberry Pi.

UNIT - IV

IoT Architecture: IoT Architecture components, Comparing IoT architectures, A simplified IoTarchitecture, The core IoT functional stack, IoT data management and compute stack

UNIT - V

IoT System design: Challenges associated with IoT, Emerging pillors of IoT, Agricultural IoT, VehicularIoT, Healthcare IoT, Smart cities, Transportation and logistics.

TEXT BOOKS:

1. Sudip Misra, Anandarup Mukherjee, Arijit Roy "Introduction to IOT", Cambridge UniversityPress.
2. David Hanes, Gonzalo salgueiro, Patrick Grossetete, Rob barton, Jerome henry "IoTFundamentals Networking technologies, protocols, and use cases for IoT", Cisco Press

REFERENCE BOOKS:

1. Cuno pfister, "Getting started with the internet of things", O Reilly Media, 2011
2. Francis daCosta, "Rethinking the Internet of Things: A Scalable Approach to ConnectingEverything", 1 st Edition, Apress Publications.
3. "Internet of Things concepts and applications", Wiley
4. Arshdeep Bahga,Vijay Madisetti "Internet of Things A Hands on approach", Universities Press
5. Shriram K Vasudevan, RMD Sundaram, Abhishek S Nagarajan, "Internet of things" John Wileyand Sons.
6. Massimo Banzi, Michael Shiloh Make: Getting Started with the Arduino, Shroff Publisher/MakerMedia Publishers.

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – II Semester

L	T	P	C
3	0	0	3

Professional Elective - III
(R22ES1513) DESIGN FOR TESTABILITY

Course Objectives:

1. To acquire the knowledge of fundamental concepts of testing
2. To provide broad understanding the fault simulation.
3. To illustrate the framework of Built-in-self test and Boundary scan methods.

Course Outcomes: Students will be able to

1. Acquire verification knowledge and test evaluation
2. Design for testability rules and techniques.
3. Utilize the scan architectures for different digital circuits.
4. Acquire the knowledge of design of built-in-self test.

UNIT - I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT - II

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuitsfor Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT - III

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations ofScan.

UNIT - IV

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per- Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT - V

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOK:

1. M.L. Bushnell, V. D. Agrawal, “Essential of Electronic Testing for Digital, Memory and MixedSignal VLSI Circuits”, Kluwer Academic Publishers.

REFERENCE BOOKS:

1. M. Abramovici, M. A. Breuer and A.D Friedman, Digital Systems and Testable Design”, Jaico Publishing House.
2. P. K. Lala, “Digital Circuits Testing and Testability”, Academic Press.

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – II Semester

L	T	P	C
3	0	0	3

ProfessionalElective - III
(R22ES1514) SOC DESIGN

Course Objectives:

1. To learn ASIC design concepts and strategies
2. To know the NISC applications and advantages
3. To familiar with simulation and synthesis process

Course Outcomes: At the end of the course, students will be able to:

1. Identify and formulate a given problem in the framework of SoC based design approaches
2. Design SoC based system for engineering applications
3. Realize impact of SoC on electronic design philosophy and Macro-electronics thereby incline towards entrepreneurship & skill development.

UNIT - I

ASIC: Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP)concepts.

UNIT - II

NISC: NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction- set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

UNIT - III

Simulation: Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

UNIT - IV

Low power SoC design / Digital system Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

UNIT - V

Synthesis: Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report, analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

TEXT BOOKS:

1. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.
2. B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006

REFERENCE BOOKS

1. Rochit Rajsuman, "System-on- a-chip: Design and test", Advantest America R & D Center, 2000
2. P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008
3. Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip". Wiley, 2011

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – II Semester

L	T	P	C
3	0	0	3

ProfessionalElective - IV

(R22ES1515) HARDWARE AND SOFTWARE CO-DESIGN

Course Objectives:

1. To Know the Co-design Issues, prototype and emulation techniques
2. To learn Architecture specific techniques
3. To know the different tool for design

Course Outcomes: Students will be able to:

1. Acquire the knowledge on various models of Co-design.
2. Explore the interrelationship between Hardware and software in a embedded system
3. Acquire the knowledge of firmware development process and tools during Co-design.
4. Implement validation methods and adaptability.

UNIT - I

Co-Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. **Co-Synthesis Algorithms:** Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT - II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT - III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT - IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT - V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

TEXT BOOKS

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf –Springer, 2009.

REFERENCE BOOKS

1. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, Kluwer Academic Publishers, 2002.
2. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont, Springer,2010

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – II Semester

L	T	P	C
3	0	0	3

ProfessionalElective - IV
(R22ES1516) SECURE NETWORKS

Course Objectives:

1. To underlying principles and techniques for network and communication security.
2. To learn practical examples of security problems and principles for countermeasures
3. To provide cryptographic methods, protocols and applications.

Course Outcomes: At the end of the course, students will be able to:

1. Identify and utilize different forms of cryptography techniques.
2. Incorporate authentication and security in the network applications.
3. Distinguish among different types of threats to the system and handle the same.

UNIT -I:

Security: Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques.

UNIT -II

Number Theory: Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

UNIT -III

Private-Key (Symmetric) Cryptography: Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

UNIT -IV

Public-Key (Asymmetric) Cryptography: RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

UNIT -V

Authentication and System Security: IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer, Secure Electronic Transaction Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Trusted Systems.

TEXT BOOKS:

1. William Stallings, "Cryptography and Network Security, Principles and Practices", PearsonEducation, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, PrivateCommunication in a Public World", Prentice Hall, 2nd Edition

REFERENCE BOOKS:

1. Christopher M. King, Ertem Osmanoglu, Curtis Dalton, "Security Architecture, DesignDeployment and Operations", RSA Press,
2. Stephen Northcutt, Leny Zeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education, 2nd Edition
3. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding IncidentDetection and Response", William Pollock Publisher, 2013.

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – II Semester

L	T	P	C
3	0	0	3

ProfessionalElective - IV

(R22ES1517) PHYSICAL DESIGN AUTOMATION

Course Objectives:

1. To understand the concepts of Physical Design Process (partitioning, Floor planning etc.,)
2. To know the concepts of design optimization algorithms and their application
3. To understand the clock and power design concepts

Course Outcomes: At the end of the course, students will be able to:

1. Implement automation process for VLSI System design.
2. Familiarize to use various physical design CAD tools.
3. Develop and enhance the existing algorithms and computational techniques for physical design process of VLSI systems.

UNIT - I

Introduction to VLSI Physical Design Automation: Design Representation, VLSI Design Styles, and VLSI Physical Design automation.

UNIT - II

Partitioning, Floor planning, Pin Assignment, Standard cell, Performance issues in circuit layout, delay models, Layout styles.

UNIT - III

Placement: Problem formulation, classification, Simulation based placement algorithms, Partitioning based placement algorithms, Time driven and performance driven placement.

UNIT - IV

Global routing: Problem formulation, classification of global routing, Maze routing algorithms, Line-Probe algorithms, and shortest path based algorithms, Steiner Tree based algorithms, Integer programming based approach, Performance driven routing.

Detailed Routing: Problem formulation, classification, Single layer, two layer, three layer and Multi-Layer channel routing, Algorithms, Switch box routing.

UNIT - V

Over the Cell Routing - Single layer and two-layer routing: Over the cell routing, Two Layer, Three Layer and Multi-Layer OTC Routing.

Via Minimization: Constraint and Unconstrained via minimization.

Clock and Power Routing: Clocking schemes, design considerations for the clock, Problem formulation, Clock routing algorithms, Skew and Delay reduction by Pin Assignment, Multiple clock routing, Power and Ground Routing

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rd Ed., 2005,
2. Algorithms for VLSI Design Automation, S.H.Gerez, 1999, WILEY Student Edition, John wiley&Sons (Asia) Pvt. Ltd.

REFERENCE BOOKS:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, 1993, Wiley.
2. Modern VLSI Design: Systems on silicon – Wayne Wolf, 2nd ed., 1998, Pearson EducationAsia

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – II Semester

L	T	P	C
0	0	4	2

(R22ES1603) ARM MICROCONTROLLERS LAB

Course Outcomes: At the end of the laboratory work, students will be able to:

1. Install, configure and utilize tool sets for developing applications based on ARM processorcore SoC.
2. Develop prototype codes using commonly available on and off chip peripherals on the ARM development boards.

List of Assignments:

Part A) Experiments to be carried out on ARM development boards

1. Blink an LED with software delay, delay generated using the SysTicktimer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED onceevery five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – II Semester

L	T	P	C
0	0	4	2

(R22ES1604) Advanced Digital Signal Processing Lab

Note: Minimum of 10 Experiments have to be conducted

List of Experiments:

1. Basic Operations on Signals, Generation of Various Signals and finding its FFT.
2. Program to verify Decimation and Interpolation of a given Sequences.
3. Program to Convert CD data into DVD data
4. Generation of Dual Tone Multiple Frequency (DTMF) Signals
5. Plot the Periodogram of a Noisy Signal and estimate PSD using Periodogram and Modified Periodogram methods
6. Estimation of Power Spectrum using Bartlett and Welch methods
7. Verification of Autocorrelation Theorem
8. Parametric methods (Yule-Walker and Burg) of Power Spectrum Estimation
9. Estimation of data series using Nth order Forward Predictor and comparing to the Original Signal
10. Design of LPC filter using Levinson-Durbin Algorithm
11. Computation of Reflection Coefficients using Schur Algorithm
12. To study Finite Length Effects using Simulink
13. ECG signal compression
14. Design and Simulation of Notch Filter to remove 60 Hz Hum/any unwanted frequency component of given Signal (Speech/ECG)

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – II Semester		L	T	P	C
		0	0	4	2

(R22ES1605) SEMINAR

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – II Semester

L	T	P	C
2	0	0	0

AUDIT COURSE – II

(R22ES1704) CONSTITUTION OF INDIA

Course Objectives: Students will be able to:

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

Course Outcomes: Students will be able to:

- Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
- Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
- Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
- Discuss the passage of the Hindu Code Bill of 1956.

UNIT-I:

History of Making of the Indian Constitution: History Drafting Committee, (Composition &Working), **Philosophy of the Indian Constitution:** Preamble**,** Salient Features.

UNIT-II:

Contours of Constitutional Rights & Duties: Fundamental Rights Right to Equality**,** Right to Freedom**,** Right against Exploitation**,** Right to Freedom of Religion**,** Cultural and Educational Rights**,** Right to Constitutional Remedies, Directive Principles of State Policy**,** Fundamental Duties.

UNIT-III:

Organs of Governance: Parliament**,** Composition**,** Qualifications and Disqualifications**,** Powers and Functions**,** Executive**,** President**,** Governor**,** Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualification, Powers and Functions.

UNIT-IV:

Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

UNIT-V:

Election Commission: Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

TEXT BOOKS/ REFERENCES:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – II Semester

L	T	P	C
2	0	0	0

AUDIT COURSE – II

(R22ES1705) PEDAGOGY STUDIES

Course Objectives: Students will be able to:

- Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.

Course Outcomes: Students will be able to understand:

- What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
- What is the evidence on the effectiveness of these pedagogical practices, in what conditions,and with what population of learners?
- How can teacher education (curriculum and practicum) and the school curriculum andguidance materials best support effective pedagogy?

UNIT-I:

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions**.** Overview of methodology and Searching.

UNIT-II:

Thematic overview: Pedagogical practices are being used by teachers in formal and informalclassrooms in developing countries. Curriculum, Teacher education.

UNIT-III:

Evidence on the effectiveness of pedagogical practices, Methodology for the indepth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the scho curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT-IV:

Professional development: alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large class sizes

UNIT-V:

Research gaps and future directions: Research design**,** Contexts**,** Pedagogy**,** Teacher education**,** Curriculum and assessment**,** Dissemination and research impact.

TEXT BOOKS/ REFERENCES:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31(2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher educationresearch project (MUSTER) country report 1. London: DFID.

4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - I Year – II Semester

L	T	P	C
2	0	0	0

AUDIT COURSE – II

(R22ES1706) STRESS MANAGEMENT BY YOGA

Course Objectives:

- To achieve overall health of body and mind
- To overcome stress

Course Outcomes: Students will be able to:

- Develop healthy mind in a healthy body thus improving social health also
- Improve efficiency

UNIT-I:

Definitions of Eight parts of yog. (Ashtanga)

UNIT-II:

Yam and Niyam.

UNIT-III:

Do`s and Don't's in life.

i) Ahinsa, satya, astheya, bramhacharya and aparigraha

ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan

UNIT-IV:

Asan and Pranayam

UNIT-V:

i) Various yog poses and their benefits for mind & body

ii) Regularization of breathing techniques and its effects-Types of pranayam

TEXT BOOKS/ REFERENCES:

1. 'Yogic Asanas for Group Tarining-Part-I": Janardan Swami Yogabhyasi Mandal, Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - II Year – I Semester

L	T	P	C
3	0	0	3

Professional Elective - V

(R22ES1518) EMBEDDED NETWORKS

Course Objectives:

1. To elaborate on the conceptual frame work of physical layer and topological issues ofnetworking in Embedded Systems.
2. To emphasis on issues related to guided and unguided media with specific reference toEmbedded device level connectivity.

Course Outcomes: Student will be able to

1. Acquire knowledge on communication protocols of connecting Embedded Systems.
2. Master the design level parameters of USB and CAN bus protocols.
3. Design Ethernet in Embedded networks considering different issues.
4. Acquire the knowledge of wireless protocols in Embedded domain.

UNIT –I

Embedded Communication Protocols: Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

UNIT –II

USB and CAN Bus: USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT –III

Ethernet Basics: Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers –Using the internet in local and internet communications – Inside the Internet protocol.

UNIT –IV

Embedded Ethernet: Exchanging messages using UDP and TCP – Serving web pages with DynamicData – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT –V

Wireless Embedded Networking: Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

TEXT BOOKS

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, TonyGivargis, John & Wiley Publications, 2002
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - JanAxelson, Penram Publications, 1996.

REFERENCE BOOKS

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series -DoganIbrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - Bhaskar Krishnamachari, Cambridge press 2005.

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - II Year – I Semester

L	T	P	C
3	0	0	3

Professional Elective - V

(R22ES1519) CMOS Mixed Signal Design

Course Objectives: The objectives of this course are to

1. Introduce circuit design concepts for basic building blocks used in mixed-signal integratedcircuit designs.
2. Provide students with the skills to design mixed-signal integrated circuits with these buildingblocks.
3. Understand design and operation of basic analog circuits.
4. Know mixed signal circuits like DAC, ADC, PLL etc.
5. Design and analysis of switched capacitor circuits
6. Analysis basic data conversion algorithms and circuits.

Course Outcomes: At the completion of this course, each student will have demonstrated proficiencyin:

1. Designing CMOS analog circuits to achieve performance specifications.
2. Analyzing CMOS based switched capacitor circuits.
3. Designing data converters and know how to use these in specific applications
4. Design a mixed-signal circuits with understanding design flow.

UNIT – I : Switched Capacitor Circuits

Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT – II : Phased Lock Loop (PLL)

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT – III : Data Converter Fundamentals

DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

UNIT – IV : Nyquist Rate A/D Converters

Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT – V : Oversampling Converters

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A.

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002.
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford UniversityPress, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013.

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van DePlassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - II Year – I Semester

L	T	P	C
3	0	0	3

Professional Elective - V

(R22ES1520) HUMAN -MACHINE INTERFACE

Course Objectives:

1. To learn the guidelines for user interface
2. To learn the foundations of Human Computer Interaction
3. To become familiar with the design technologies for individuals and persons with disabilities
4. To learn about different HCI models
5. To become familiar with the features of windows and interactive devices

Course Outcomes: Upon completion of the course, the students will be able to:

1. Design effective dialog for HCI
2. Design effective HCI for individuals and persons with disabilities
3. Assess the importance of user feedback.
4. Explain the HCI implications for designing multimedia/ e-learning Web sites
5. Develop meaningful user interface.

UNIT – I : Basics of User Interface

Importance of user interface- Definition, importance of good design, benefits of good design, brief history of human-computer interface, Graphical User Interface, Popularity of Graphics, Concept of Direct Manipulation, Graphical Systems, Characteristics of GUI, Web user interface popularity, Characteristics and Principles of user interface

UNIT – II : Foundations of Human Computer Interface

The Human: I/O channels – Memory – Reasoning and problem solving; The Computer: Devices – Memory – processing and networks; Interaction: Models – frameworks – Ergonomics – styles – elements – interactivity- Paradigms. - Case Studies

UNIT – III : Design Process

Interactive Design: Basics – process – scenarios – navigation – screen design – Iteration and prototyping. HCI in software process: Software life cycle – usability engineering – Prototyping in practice
– design rationale. Design rules: principles, standards, guidelines, rules. Evaluation Techniques – Universal Design

UNIT – IV: Models and Theories

HCI Models: Cognitive models: Socio-Organizational issues and stakeholder requirements, Communication and collaboration models-Hypertext, Multimedia and WWW.

UNIT – V: Windows and Interaction Devices

Window characteristics, Components of window, Window Presentation Style, Types of windows, Organizing window functions, Characteristics of input devices, Selection of proper input devices,Output devices

TEXT BOOKS:

1. Wilbert O. Galitz - The essential Guide to User Interface Design, 3rd Ed., Wiley, 2007 (Unit I & V)
2. Alan Dix, Janet Finlay, Gregory Abowd, Russell Beale, ―Human Computer Interaction‖, 3rd Ed., Pearson Education, 2004 (UNIT II, III & IV)

REFERENCE BOOKS:

1. Daniel Newman, Olivier Blanchard – Human/Machine: The Future of our partnership withmachine,
2. Paul R. Daugherty, H. James Wilson – Human+Machine: Reimagining work in the Age of AIHardcover, Kindle Ed.,

SRI INDU COLLEGE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - II Year – I Semester

L	T	P	C
3	0	0	3

(R22ES1521) Business Analytics
(Open Elective)

Course objectives:

- Understand the role of business analytics within an organization.
- Analyze data using statistical and data mining techniques and understand relationships between the underlying business processes of an organization.
- To gain an understanding of how managers use business analytics to formulate and solve business problems and to support managerial decision making.
- To become familiar with processes needed to develop, report, and analyze business data.
- Use decision-making tools/Operations research techniques.
- Mange business process using analytical and management tools.
- Analyze and solve problems from different industries such as manufacturing, service, retail, software, banking and finance, sports, pharmaceutical, aerospace etc.

Course Outcomes:

- Students will demonstrate knowledge of data analytics.
- Students will demonstrate the ability of think critically in making decisions based on data and deep analytics.
- Students will demonstrate the ability to use technical skills in predicative and prescriptive modeling to support business decision-making.
- Students will demonstrate the ability to translate data into clear, actionable insights.

Unit- I:

Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organisation, competitive advantages of Business Analytics.

Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modelling, sampling and estimation methods overview.

Unit - II:

Trendiness and Regression Analysis: Modelling Relationships and Trends in Data, simple Linear Regression.Important Resources, Business Analytics Personnel, Data and modelsfor Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology

Unit- III:

Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes.Descriptive Analytics, predictive analytics, predicative Modelling, Predictive analytics analysis,DataMining,Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modelling, nonlinear Optimization.

Unit- IV:

Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models.

Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation

Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.

Unit - V:

Decision Analysis: Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, The Value of Information, Utility and Decision Making. Recent Trends in : Embedded and collaborative business intelligence,Visual data recovery, Data Storytelling and Data journalism

Text Books:

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FTPress.
2. Business Analytics by James Evans, personsEducation.

SRI INDU COLLEGE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - II Year – I Semester

L	T	P	C
3	0	0	3

(R22ES1522) Industrial Safety
(Open Elective)

Course Objectives:

- To provide information regarding different elements of industrial water pollution and Methods of treatment.
- To expose to the various industrial applications, maintenance, preventive measures taken against wear and tear.

Course Outcomes: At the end of the course, student will be able to:

- Know how to take safety measures in executing works
- Identify the need for maintenance (or) replacement of equipment
- Understand the need for periodic and preventive maintenance

Unit-I:

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

Unit-II:

Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

Unit-III :

Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications,

i. Screw down grease cup,
ii. Pressure grease gun,
iii. Splash lubrication,
iv. Gravity lubrication,
v. Wick feed lubrication
vi. Side feed lubrication,
vii. Ring lubrication,

Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

Unit-IV:

Fault tracing: Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment‟s like,

i. Any one machine tool,
ii. Pump
iii. Air compressor,
iv. Internal combustion engine,

v. Boiler,
vi. Electrical motors, Types of faults in machine tools and their general causes.

Unit-V:

Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of:

i. Machine tools,
ii. Pumps,
iii. Air compressors,
iv. Diesel generating (DG) sets,

Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

Reference Books:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.
3. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication.
4. Foundation Engineering Handbook, Winterkorn, Hans, Chapman &HallLondon

SRI INDU COLLEGE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - II Year – I Semester

L	T	P	C
3	0	0	3

(R22ES1523) Operations Research
(Open Elective)

Course Outcomes: At the end of the course, the student should be able to

1. Students should able to apply the dynamic programming to solve problems of discreet and continuous variables.
2. Students should able to apply the concept of non-linear programming
3. Students should able to carry out sensitivity analysis
4. Student should able to model the real world problem and simulate it.

Unit-I:

Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models

Unit-II:

Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming

Unit-III:

Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT

Unit-IV:

Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

Unit-V: Competitive Models, Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation

Text Books / Reference Books:

1. H.A. Taha, Operations Research, An Introduction, PHI, 2008
2. H.M. Wagner, Principles of Operations Research, PHI, Delhi, 1982.
3. J.C. Pant, Introduction to Optimisation: Operations Research, Jain Brothers, Delhi, 2008
4. Hitler Libermann Operations Research: McGraw Hill Pub. 2009
5. Pannerselvam, Operations Research: Prentice Hall of India 2010
6. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India 2010

SRI INDU COLLEGE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - II Year – I Semester

L	T	P	C
3	0	0	3

(R22ES1524) COST MANAGEMENT OF ENGINEERING PROJECTS

(Open Elective)

COURSE OBJECTIVES: The course should enable the students to:

1. Establish systems to help streamline the transactions between corporate support departments and the operating units.
2. Devise transfer pricing systems to coordinate the buyer-supplier interactions between decentralized organizational operating units.
3. Use pseudo profit centers to create profit maximizing behavior in what were formerly cost centers.

COURSE OUTCOMES:

1. Understand the concept of strategic cost management, strategic cost analysis – target costing, life cycle costing and Kaizen costing and the cost drive concept.
2. Describe the decision-making; relevant cost, differential cost, incremental cost and opportunity cost, objectives of a costing system.
3. Understand the meaning and different types of project management and project execution, detailed engineering activities.
4. Understand the project contracts, cost behaviour and profit planning types and contents, Bar charts and Network diagram.
5. Analyse by using quantitative techniques for cost management like PERT/CPM.

UNIT-I INTRODUCTION

Introduction and Overview of the Strategic Cost Management Process.

UNIT -II COST CONCEPTS

Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision Making.

UNIT-III PROJECT MANAGEMENT

Project: meaning, Different types, why to manage, cost overruns centers, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and nontechnical activities. Detailed Engineering activities. Pre project execution main clearances and documents. Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process.

UNIT-IV COST BEHAVIOR AND PROFIT PLANNING

Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard Costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement, Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints. Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis. Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing.

UNIT-V QUANTITATIVE TECHNIQUES

Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation Problems, Assignment problems, Simulation, Learning Curve Theory.

Text Books:

1.Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting.
2. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd.

Reference Books:

1. Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi.
2. Charles T. Horngren and George Foster Advanced Management Accounting.
3. Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler publisher.

SRI INDU COLLEGE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - II Year – I Semester

L	T	P	C
3	0	0	3

(R22ES1525) COMPOSITE MATERIALS
(Open Elective)

Course objectives:

- Develop understanding of the structure of ceramic materials on multiple length scales.
- Develop knowledge of point defect generation in ceramic materials, and their impact on transport properties.
- To describe key processing techniques for producing metal, ceramic-, and polymer-matrix composites.
- To demonstrate the relationship among synthesis, processing, and properties in composite materials.

Course Outcomes:

1. Knowledge of the crystal structures of a wide range of ceramic materials and glasses.
2. Able to explain how common fibers are produced and how the properties of the fibers are related to the internal structure.
3. Able to select matrices for composite materials in different applications.
4. Able to describe key processing methods for fabricating composites.

UNIT - I

Introduction: Definition, Classification of Composite materials based on structure, based on matrix, Advantages of composites, Applications of composites, Functional requirements of reinforcement and matrix.

UNIT - II

Types of reinforcements and their properties: Fibers: Carbon, Boron, Glass, Aramid, Al2O3, SiC, Nature and manufacture of glass, carbon and aramid fibres, Comparison of fibres. Role of interfaces: Wettability and Bonding, The interface in Composites, Interactions and Types of bonding at the Interface, Tests for measuring Interfacial strength.

UNIT - III

Fabrication of Polymeric Matrix Composites, Structure and properties of Polymeric Matrix Composites, Interface in Polymeric Matrix Composites, Applications; Fabrication of Ceramic Matrix Composites, Properties of Ceramic Matrix Composites, Interface in Ceramic Matrix Composites, Toughness of Ceramic Matrix Composites Applications of Ceramic Matrix Composites.

UNIT - IV

Fabrication of Metal Matrix Composites: Solid state fabrication, Liquid state fabrication and In-situ fabrication techniques; Interface in Metal Matrix Composites: Mechanical bonding, Chemical bonding and Interfaces in In-situ Composites; Discontinuously reinforced Metal Matrix Composites, Properties and Applications. Fabrication of Carbon fiber composites, properties, interface and applications.

UNIT - V

Micromechanics of Composites: Density, Mechanical Properties: Prediction of Elastic constants, Micro mechanical approach, Halpin-Tsai equations, Transverse stresses; Thermal properties: Hydrothermal stresses and Mechanics of Load transfer from matrix to fiber.

TEXTS BOOKS:

1. Composite Materials – Science & Engineering, K.K. Chawla, Springer-Verlag, New York, 1987.
2. An Introduction to Composite Materials, Hull, Cambridge, 2nd Edt. 1997.

REFERENCE BOOKS:

1. Composites, Engineered Materials Handbook, Vol. 1, ASM International, Ohio, 1988.
2. Structure and Properties of Composites, Materials Science and Technology, Vol. 13, VCH, Weinheim, Germany, 1993
3. Composite Materials: Engineering and Science, F.L. Matthews and R.D. Rawlings, Chapman & Hall, London, 1994

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

M.Tech. - II Year – I Semester		L	T	P	C
		0	0	12	6

(R22ES1606) Dissertation Work Review – II

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY					
(An Autonomous Institution under UGC, New Delhi)					
M.Tech. - II Year – II Semester		**L**	**T**	**P**	**C**
		0	**0**	**12**	**6**
(R22ES1607) Dissertation Work Review – III					

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY					
(An Autonomous Institution under UGC, New Delhi)					
M.Tech. - II Year – II Semester		**L**	**T**	**P**	**C**
		0	**0**	**28**	**14**
(R22ES1608) Dissertation Viva-Voce					