# Time Table (Off-Line Mode Only)

## I M.Tech I Semester - (Regular and Supplementary) End Examination - March-2024.

(Admitted batches: 2023-24 (Regular) and 2022-23 (Suppl.), MR-22 Regulation.)

## Time of Examination: FN - 10:00 AM to 01:00 PM

<table>
<thead>
<tr>
<th>SL. NO.</th>
<th>BRANCH</th>
<th>04.03.2024</th>
<th>06.03.2024</th>
<th>09.03.2024</th>
<th>12.03.2024</th>
<th>14.03.2024</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CSE</td>
<td>Mathematical Foundations of Computer Science R22CSE1501</td>
<td>Advanced Data Structures R22CSE1502</td>
<td>Deep Learning R22CSE1504</td>
<td>Software Quality Engineering R22CSE1507</td>
<td>Research Methodology &amp; IPR R22CSE1605</td>
</tr>
</tbody>
</table>

* [Students must affix latest photo with date printed (Not taken earlier than a Month) on Hall Ticket]*

**Note:**

(i) Any omissions or clashes in this time table may please be informed to the Dean of Examinations immediately.

(ii) In case the Government declares a holiday on any of the above dates, the examination scheduled on that day will be conducted after the last day of the examination.

(iii) The examinations will be conducted off-line, all the students must attend to college and appear for the examination.

**Controller of Examination**
Sri Indu College of Engineering & Technology (An Autonomous Institution Under UGC)
Sheriguda (V), Ibrahimpatnam, R.R. Dist. 501510.

**Principal**
Sri Indu College of Engineering & Technology (An Autonomous Institution Under UGC)
Sheriguda (V), Ibrahimpatnam, R.R. Dist. 501510.
## TIME TABLE (OFF-LINE MODE)

**I.M.TECH - I SEMESTER - (SUPPLEMENTARY) END EXAMINATION - MAR-2024**

ADMITTED BATCHES: 2021-22 and 2020-21, MR-20 (SUPPL.)

**TIME OF EXAMINATION: FN - 10:00 AM to 01:00 PM**

<table>
<thead>
<tr>
<th>SL.NO.</th>
<th>BRANCH</th>
<th>04.03.2024</th>
<th>06.03.2024</th>
<th>09.03.2024</th>
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<th>14.03.2024</th>
<th>16.03.2024</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CSE</td>
<td>Advanced Data Structures and Algorithms (R20CSE1501)</td>
<td>Computer Networking (R20CSE1502)</td>
<td>Advanced Operating Systems (R20CSE1503)</td>
<td>Artificial Intelligence (R20CSE1504)</td>
<td>Software Process and Project Management (R20CSE1505)</td>
<td>Internet of Things (R20CSE1510)</td>
</tr>
<tr>
<td>2</td>
<td>ES</td>
<td>Micro Controllers And Programmable Digital Signal Processors (R20ES1501)</td>
<td>System Design With Embedded Linux (R20ES1502)</td>
<td>Programming Languages For Embedded Software (R20ES1503)</td>
<td>Communications Buses And Interfaces (R20ES1506)</td>
<td>Research Methodology And IPR (R20ES1509)</td>
<td>——</td>
</tr>
</tbody>
</table>

* [STUDENTS MUST AFFIX LATEST PHOTO WITH DATE PRINTED (Not taken earlier than a Month) ON HALL TICKET]

**NOTE:**

(i) ANY OMISSIONS OR CLASHES IN THIS TIME TABLE MAY PLEASE BE INFORMED TO THE DEAN OF EXAMINATIONS IMMEDIATELY.

(ii) IN CASE THE GOVERNMENT DECLARES A HOLIDAY ON ANY OF THE ABOVE DATES, THE EXAMINATION SCHEDULED ON THAT DAY WILL BE CONDUCTED AFTER THE LAST DAY OF THE EXAMINATION.

(iii) THE EXAMINATIONS WILL BE CONDUCTED OFF-LINE. ALL THE STUDENTS MUST ATTEND TO COLLEGE AND APPEAR FOR THE EXAMINATIONS.

---

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(An Autonomous Institution Under UGC)
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DIRECTOR
Sri Indu College of Engineering & Technology
(An Autonomous Institution Under UGC)
Sheriguda (V), Ibrahimpatnam, R.R. Dist, Hyderabad - 501510.

PRINCIPAL
Sri Indu College of Engineering & Technology
(An Autonomous Institution Under UGC)
Sheriguda (V), Ibrahimpatnam, R.R. Dist, Hyderabad - 501510.
**TIME TABLE (OFF-LINE MODE)**

M.TECH: I YEAR - II SEMESTER (SUPPLEMENTARY) END EXAMINATION - MARCH-2024
ADMITTED BATCH - 2022-23 (MR-22 REGULATION)
(BRANCH :- COMPUTER SCIENCE & ENGINEERING)

**TIME OF EXAMINATION:** FN - 10:00 AM TO 01:00 PM

<table>
<thead>
<tr>
<th>SL.NO</th>
<th>DATE</th>
<th>SUBJECT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>05.03.2024</td>
<td>Advanced Algorithms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R22CSE1509</td>
</tr>
<tr>
<td>2</td>
<td>07.03.2024</td>
<td>Advanced Computer Architecture</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R22CSE1510</td>
</tr>
<tr>
<td>3</td>
<td>11.03.2024</td>
<td>Advanced Computer Networks</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R22CSE1512</td>
</tr>
<tr>
<td>4</td>
<td>13.03.2024</td>
<td>Robotic Process Automation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R22CSE1516</td>
</tr>
</tbody>
</table>

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# TIME TABLE (OFF-LINE MODE)

**I M.TECH - II SEMESTER - (SUPPLEMENTARY) END EXAMINATION - MARCH-2024**

**ADMITTED BATCHES - 2021-22 and 2020-21 (MR-20) REGULATION**

**TIME OF EXAMINATION: FN - 10:00 AM to 01:00 PM**

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</tr>
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<tbody>
<tr>
<td>1</td>
<td>CSE</td>
<td>Network Programming (R20CSE1513)</td>
<td>Database System concepts (R20CSE1514)</td>
<td>Web Services and Service Oriented Architecture (R20CSE1515)</td>
<td>Big Data Analytics (R20CSE1516)</td>
<td>Android Application Development (R20CSE1519)</td>
<td>Distributed Systems and Cloud Computing (R20CSE1523)</td>
</tr>
<tr>
<td>2</td>
<td>ES</td>
<td>RTL Simulation and Synthesis with PLDs (R20ES1510)</td>
<td>Advanced Digital Signal Processing (R20ES1511)</td>
<td>IOT and its Applications (R20ES1512)</td>
<td>Hardware and Software Co-Design (R20ES1515)</td>
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[Signatures]

**Controller of Examination**

**Director**

**Principal**