

ELECTRONIC DEVICES AND CIRCUITS

LAB MANUAL

Subject Code : **R22ECE1229**
Regulations : **R22**
Class : **I Year II Sem B.Tech**



Department of Electronics and Communication Engineering

SRI INDU INSTITUTE OF ENGINEERING AND TECHNOLOGY

Ibrahimpatnam - 501 510, Hyderabad

ELECTRONIC DEVICES AND CIRCUITS LAB
LIST OF EXPERIMENTS(Twelve Experiments to be done)

S. No	Name of the Experiment
1	P-N Junction Diode Characteristics A)Forward bias B)Reverse bias
2	Full Wave Rectifier With And Without Filters
3	Types of Clippers at different reference voltages
4	Types of Clampers at different reference voltages
5	The steady state output waveform of clampers for a square waveinput
6	Input and Output Characteristic Of Transistor In CB Configuration
7	Input and Output Characteristic Of Transistor In CE Configuration
8	Input and Output Characteristic Of Transistor In CC Configuration
9	Input and Output Characteristic Of FET In CS Configuration
10	Input and Output Characteristic Of FET In CD Configuration
11	Switching Characteristics of a Transistor
12	Zener Diode Characteristics and Zener as voltage regulator
13	Silicon-Controlled Rectifier (SCR) Characteristics
14	UJT characteristics and identify negative region
15	Photo diode characteristics
16	Solar cell characteristics
17	LED characteristics

Experiment-1

P-N Junction Diode Characteristics

AIM:

1. To observe and draw the Forward and Reverse bias V-I Characteristics of a P-N Junction diode.
2. To calculate static and dynamic resistance in both forward and Reverse Bias conditions.

APPARATUS:

- | | |
|-----------------------------------|---------|
| 1. P-N Diode 1N4007 | - 1No. |
| 2. Regulated Power supply (0-30V) | - 1No. |
| 3. Resistor 1K Ω | - 1No. |
| 4. Ammeter (0-200 mA) | - 1No. |
| 5. Ammeter (0-200 μ A) | - 1 No. |
| 6. Voltmeter (0-20V) | -2No. |
| 7. Bread board | |
| 8. Connecting wires | |

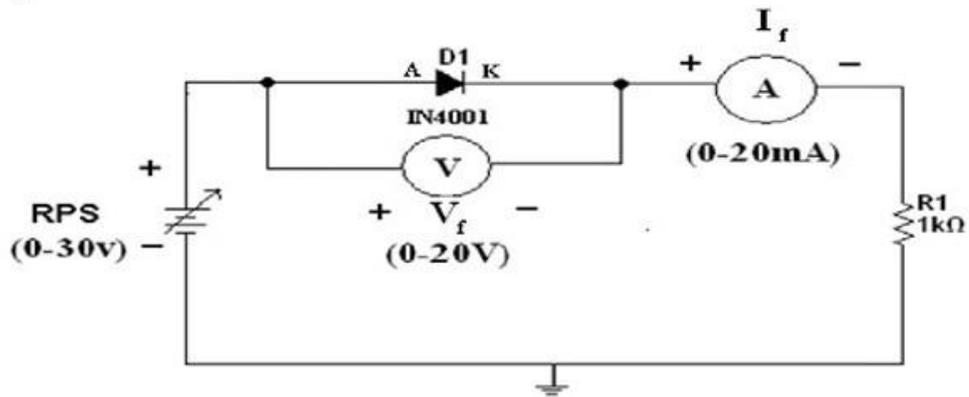
THEORY:

A p-n junction diode conducts only in one direction. The V-I characteristics of the diode are curve between voltage across the diode and current flowing through the diode. When external voltage is zero, circuit is open and the potential barrier does not allow the current to flow. Therefore, the circuit current is zero. When P-type (Anode) is connected to Positive terminal and n- type (cathode) is connected to Negative terminal of the supply voltage is known as forward bias. The potential barrier is reduced when diode is in the forward biased condition. At some forward voltage, the potential barrier altogether eliminated and current starts flowing through the diode and also in the circuit. Then diode is said to be in ON state. The current increases with increasing forward voltage.

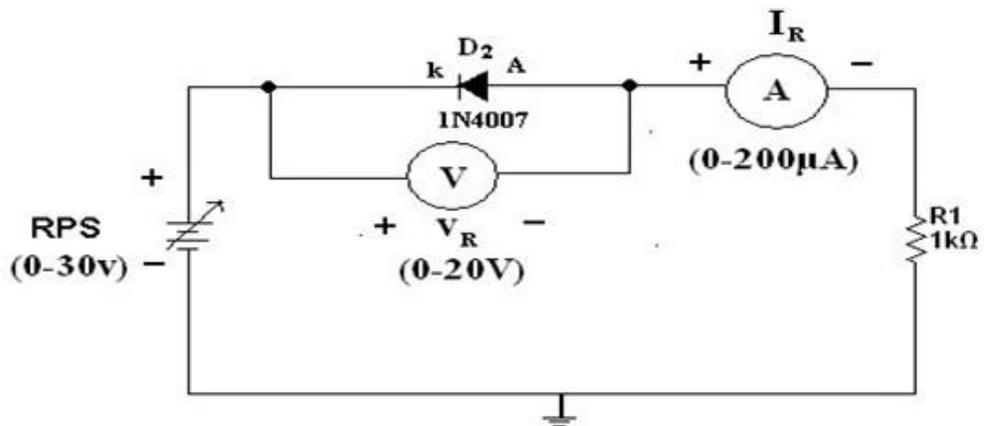
When N-type (cathode) is connected to Positive terminal and P- type (Anode) is connected to Negative terminal of the supply voltage is known as reverse bias and the potential barrier across the junction increases. Therefore, the junction resistance becomes very high and a very small current (reverse saturation current) flows in the circuit. Then diode is said to be in OFF state. The reverse bias current is due to minority charge carriers.

CIRCUIT DIAGRAM:

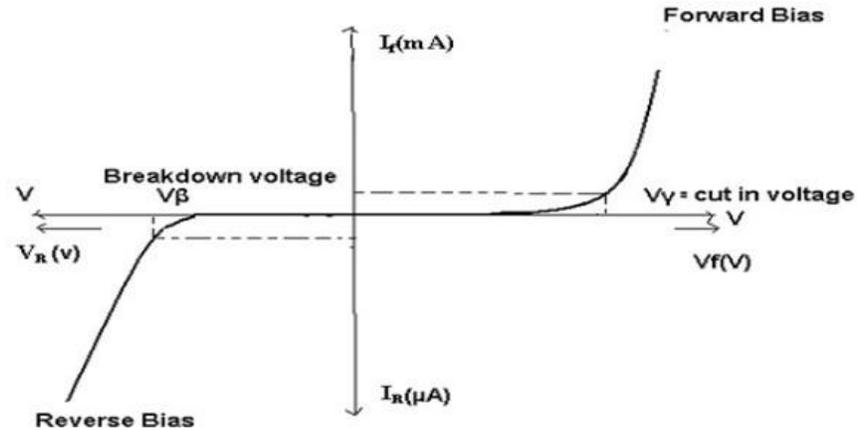
Forward bias



Reverse Bias:



MODEL GRAPH:



PROCEDURE:

A) FORWARD BIAS:

1. Connections are made as per the circuit diagram.
2. For forward bias, the RPS +ve is connected to the anode of the diode and RPS -ve is connected to the cathode of the diode
3. Switch on the power supply and increases the input voltage (supply voltage) in Steps of 0.1V
4. Note down the corresponding current flowing through the diode and voltage across the diode for each and every step of the input voltage.
5. The reading of voltage and current are tabulated.
6. Graph is plotted between voltage (V_f) on X-axis and current (I_f) on Y-axis.

B) REVERSE BIAS:

1. Connections are made as per the circuit diagram
2. For reverse bias, the RPS Positive is connected to the cathode of the diode and RPS Negative is connected to the anode of the diode.
3. Switch on the power supply and increase the input voltage (supply voltage) in Steps of 1V.
4. Note down the corresponding current flowing through the diode voltage across the diode for each and every step of the input voltage.
5. The readings of voltage and current are tabulated
6. Graph is plotted between voltage(V_R) on X-axis and current (I_R) on Y-axis.

OBSERVATIONS:

FORWARD BIAS

SL.NO.	APPLIED VOLTAGE (V)	FORWARD VOLTAGE(V_F)	FORWARD CURRENT (I_F)
1	0		
2	1		
3	2		
4	3		
5	4		
6	5		
7	6		
8	7		
9	8		
10	9		
11	10		
12	15		
13	20		
14	25		

REVERSE BIAS

Sl.No.	Applied Voltage(V)	Reverse Voltage(V_R)	Reverse Current($I_R(\mu A)$)
1	0		
2	1		
3	2		
4	3		
5	4		
6	5		
7	6		
8	7		
9	8		
10	9		
11	10		
12	15		
13	20		
14	25		
15	30		

PRECAUTIONS:

1. All the connections should be correct.
2. Parallax error should be avoided while taking the readings from the Analog meters

CALCULATIONS:

In Forward bias condition:

$$\text{Static Resistance } (R_s) = V_f / I_f =$$

$$\text{Dynamic Resistance } (R_d) = \Delta V_f / \Delta I_f =$$

In Reverse bias condition:

$$\text{Static Resistance } , R_s = V_R / I_R =$$

$$\text{Dynamic Resistance, } R_d = \Delta V_R / \Delta I_R =$$

RESULT:

Thus, we have calculated the static and dynamic resistance of P-N Junction diode from its characteristics.

VIVA QUESTIONS:

1. Define depletion region of a diode?
2. What is meant by transition & space charge capacitance of a diode?
3. Is the V-I relationship of a diode Linear or Exponential?
4. Define cut-in voltage of a diode and specify the values for Si and Ge diodes?
5. What are the applications of a p-n diode?
6. Draw the ideal characteristics of P-N junction diode?
7. What is the diode equation?
8. What is PIV?
9. What is the break down voltage?
10. What is the effect of temperature on PN junction diodes?

Experiment-10

Zener Diode Characteristics and Zener as voltage regulator

AIM:

- a) To observe and draw the static characteristics of a zener diode.
- b) To find the voltage regulation of a given zener diode.

APPARATUS:

- | | | |
|-----------------------------------|---|------|
| 1. Zener diode | - | 1No. |
| 2. Regulated Power Supply (0-30v) | - | 1No. |
| 3. Voltmeter (0-20v) | - | 1No. |
| 4. Ammeter (0-200mA) | - | 1No. |
| 5. Resistor (1K ohm) | | |
| 6. Bread Board | | |
| 7. Connecting wires | | |

THEORY:

A zener diode is heavily doped p-n junction diode, specially made to operate in the break down region. A p-n junction diode normally does not conduct when reverse biased. But if the reverse bias is increased, at a particular voltage it starts conducting heavily. This voltage is called Break down Voltage. High current through the diode can permanently damage the device.

To avoid high current, we connect a resistor in series with zener diode. Once the diode starts conducting it maintains almost constant voltage across the terminals whatever may be the current through it, i.e., it has very low dynamic resistance. It is used in voltage regulators.

PROCEDURE:

Static characteristics:

1. Connections are made as per the circuit diagram.
2. The Regulated power supply voltage is increased in steps.
3. The Forward current (I_f), and the forward voltage (V_f) are observed and then noted in the tabular form.
4. A graph is plotted between Forward current (I_f) on X-axis and the forward voltage (V_f) on Y-axis.

Regulation characteristics:

1. Connection are made as per the circuit diagram
2. The load is placed in full load condition and the zener voltage (V_Z), Zener current (I_Z), load current (I_L) are measured.
3. The above is repeated by decreasing the value of the load in steps.
4. All the readings are tabulated.
5. The percentage regulation is calculated using the below formula
6. The voltage regulation of any device is usually expressed as percentage regulation.

The percentage regulation is given by the formula

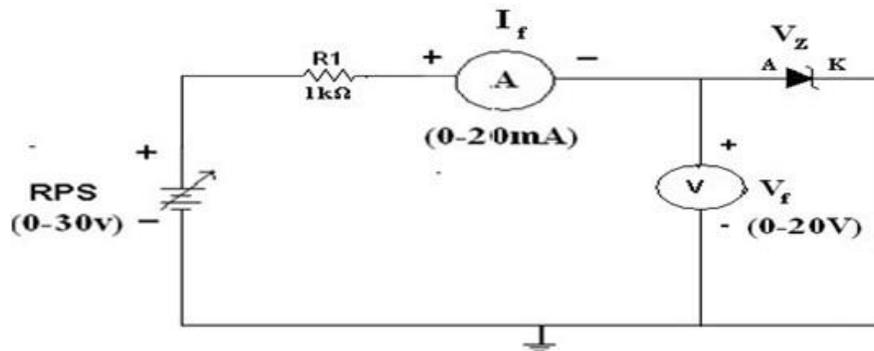
$$\frac{(V_{NL}-V_{FL})}{V_{FL}} \times 100$$

V_{NL} =Voltage across the diode, when no load is connected.

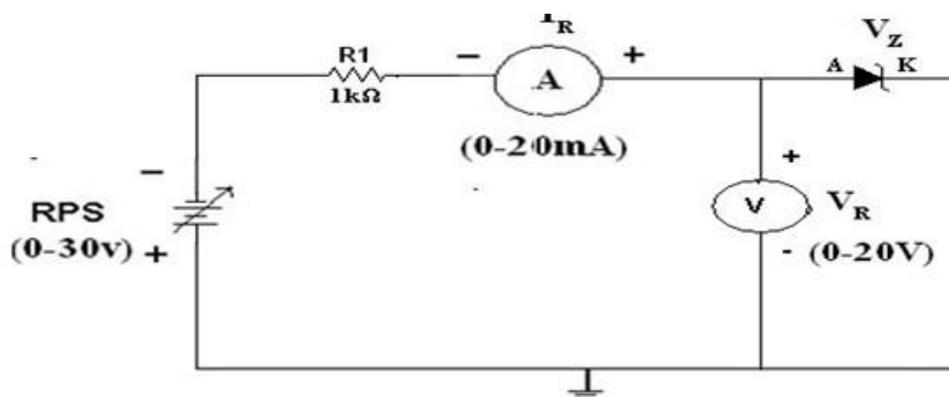
V_{FL} =Voltage across the diode, when load is connected.

CIRCUIT DIAGRAM:

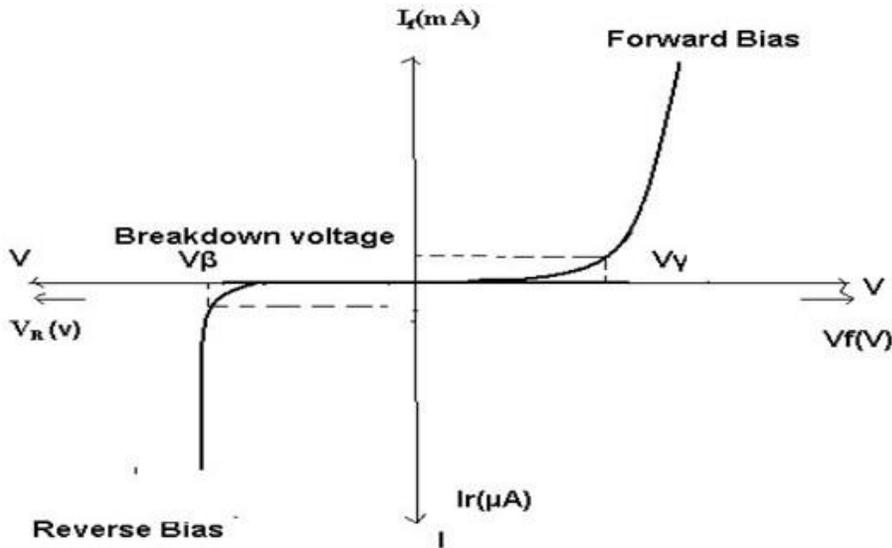
STATIC CHARACTERISTICS:



REGULATION CHARACTERISTICS:



Model Graph:



OBSERVATIONS:

Static characteristics

SL.NO.	APPLIED VOLTAGE (V)	FORWARD VOLTAGE(V _F)	FORWARD CURRENT (I _F)
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			

REVERSE BIAS:

Sl.No.	Applied Voltage(V)	Reverse Voltage(V _R)	Reverse Current(I _R (μA))
1	0		
2	1		
3	2		
4	3		
5	4		
6	5		
7	6		
8	7		
9	8		
10	9		
11	10		
12	15		
13	20		
14	25		
15	30		

PRECAUTIONS:

1. The terminals of the zener diode should be properly identified
2. While determined the load regulation, load should not be immediately shorted.
3. Should be ensured that the applied voltages & currents do not exceed the ratings of the diode.

RESULT:

Thus, we have drawn zener diode characteristics and also observed its regulation characteristics.

VIVAQUESTIONS:

1. What type of temperature Coefficient does the zener diode have?
2. If the impurity concentration is increased, how the depletion width effected?
3. Does the dynamic impedance of a zener diode vary?
4. Explain briefly about avalanche and zener breakdowns?
5. Draw the zener equivalent circuit?
6. Differentiate between line regulation & load regulation?
7. In which region zener diode can be used as a regulator?
8. How the breakdown voltage of a particular diode can be controlled?
9. What type of temperature coefficient does the Avalanche breakdown have?
10. By what type of charge carriers the current flows in zener and avalanche breakdown diodes?

Experiment-2

Full Wave Rectifier With and Without Filters

AIM:

To examine the input and output waveforms of Full Wave Rectifier and also calculate its load regulation and ripple factor.

1. with Filter
2. without Filter

APPARATUS:

- | | |
|--------------------------------------|--------------------|
| 1. Digital millimeter | - 1No. |
| 2. Transformer (6V-0-6V) | - 1No. |
| 3. Diode (1N4007) | - 2No. |
| 4. Capacitor 100 μ f/470 μ f | - 1No. |
| 5. Decade Resistance Box | - 1 No. Breadboard |
| 6. CRO and CRO probes | |
| 7. Connecting wires | |

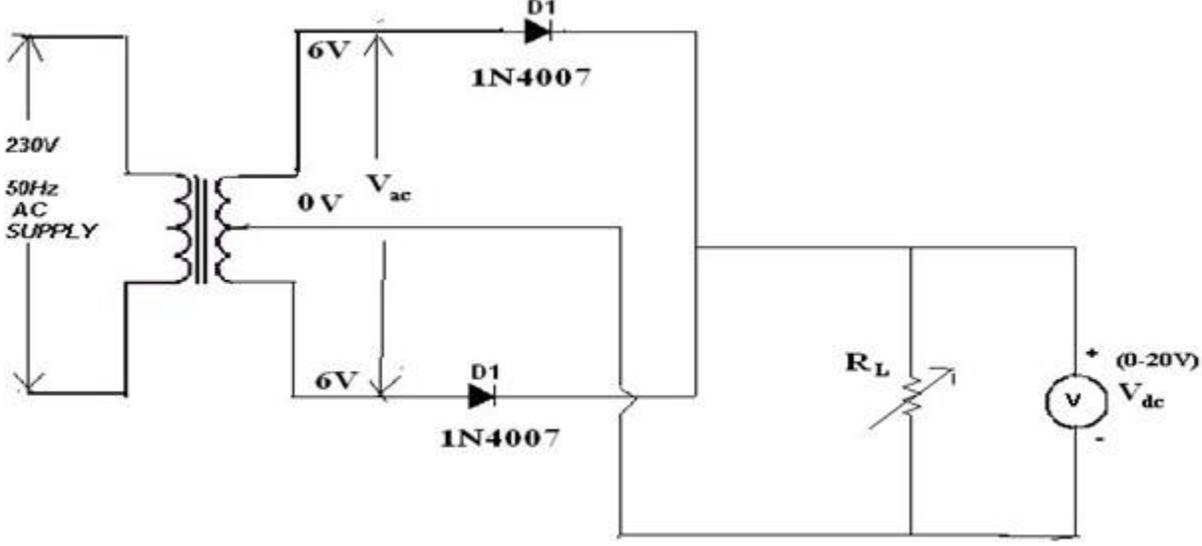
THEORY:

A Full Wave Rectifier is a circuit, which converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. It uses two diodes of which one conducts during one half cycle while the other conducts during the other half cycle of the applied ac voltage.

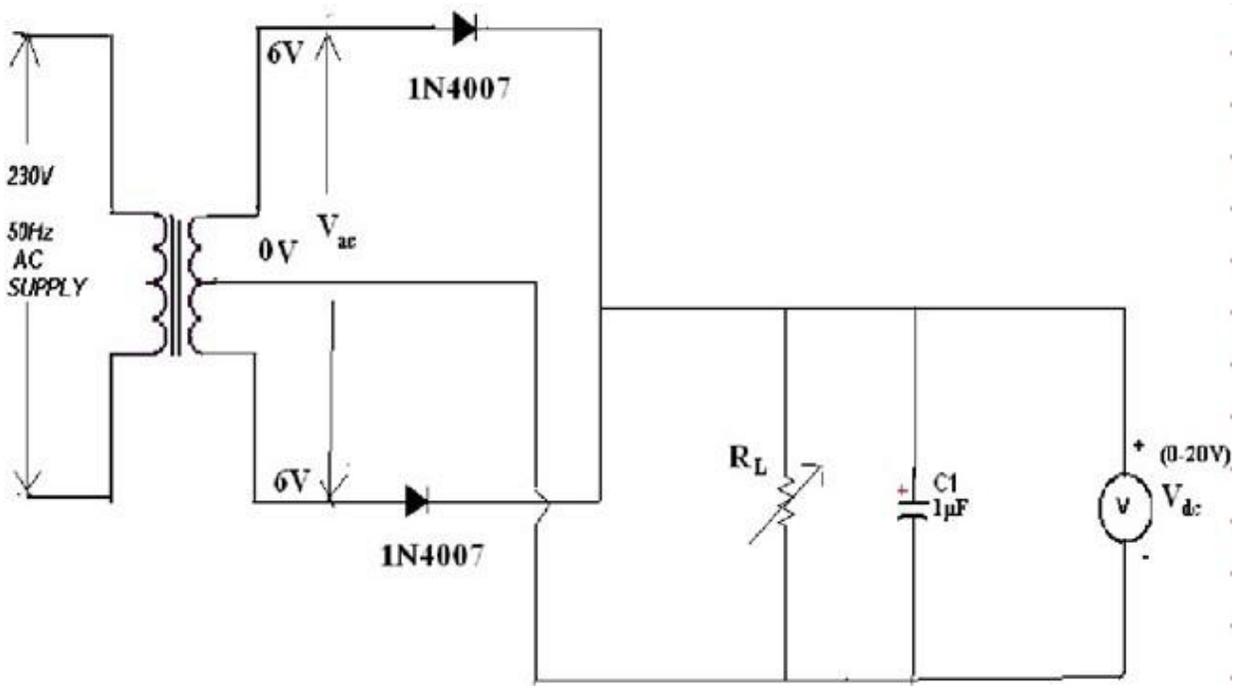
The output voltage across the resistor R is the pharos sum of the two waveforms, it is also known as a bi-phase circuit. The spaces between each half-wave developed by each diode are now being filled in by the other. The average DC output voltage across the load resistor is now double that of the single half-wave rectifier circuit and is about $0.637V_{max}$ of the peak voltage by assuming no losses. V_{MAX} is the maximum peak value in one half of the secondary winding and V_{RMS} is the rms value.

CIRCUIT DIAGRAM:

FULL WAVE RECTIFIER WITHOUT FILTER:



FULL WAVE RECTIFIER WITH FILTER:



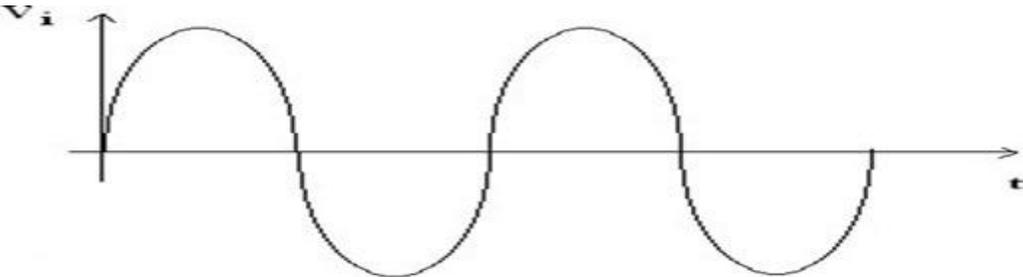
With filter:

$$\text{Ripple factor, } r = 1 / (4\sqrt{3} f C R_L)$$

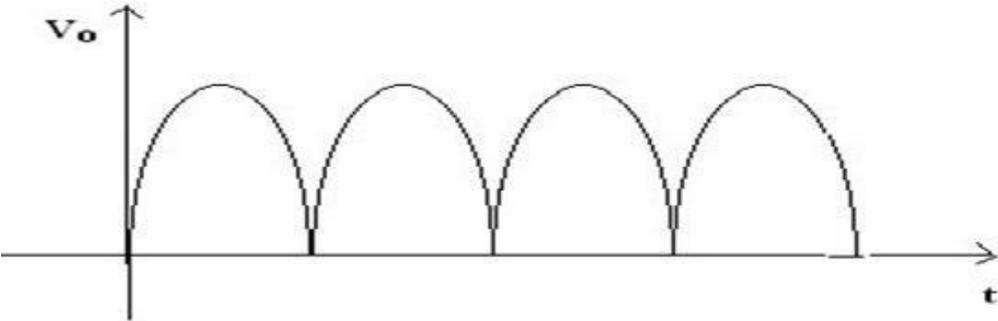
S.NO	RL	V ₁	V ₂	V _{dc}	V _{ac}	V _{rms}	Ripple factor	η/

MODEL WAVEFORMS:

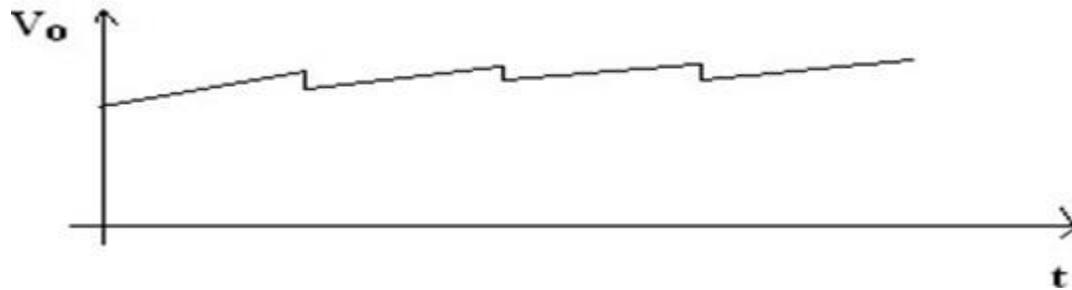
INPUT WAVEFORM



OUTPUT WAVEFORM WITHOUT FILTER:



OUTPUT WAVEFORM WITH FILTER:



PRECAUTIONS:

1. The primary and secondary side of the transformer should be carefully identified.
2. The polarities of all the diodes should be carefully identified.

RESULT:

We have examined the input and output waveforms of Full Wave Rectifier and also calculate its load regulation and ripple factor.

1. with Filter
2. without Filter

VIVA QUESTIONS:

1. Define peak inverse voltage (PIV)? And write its value for Full-wave rectifier?
2. If one of the diode is changed in its polarities what wave form would you get?
3. Does the process of rectification alter the frequency of the waveform?
4. What is ripple factor of the Full-wave rectifier?
5. What is the necessity of the transformer in the rectifier circuit?
6. What are the applications of a rectifier?
7. What is meant by ripple and define Ripple factor?
8. Explain how capacitor helps to improve the ripple factor?

Experiment-7

Input and output characteristic of Transistor in CE configuration

AIM:

1. To draw the input and output characteristics of transistor connected in CE configuration
2. To find β of the given transistor and also its input and output Resistances

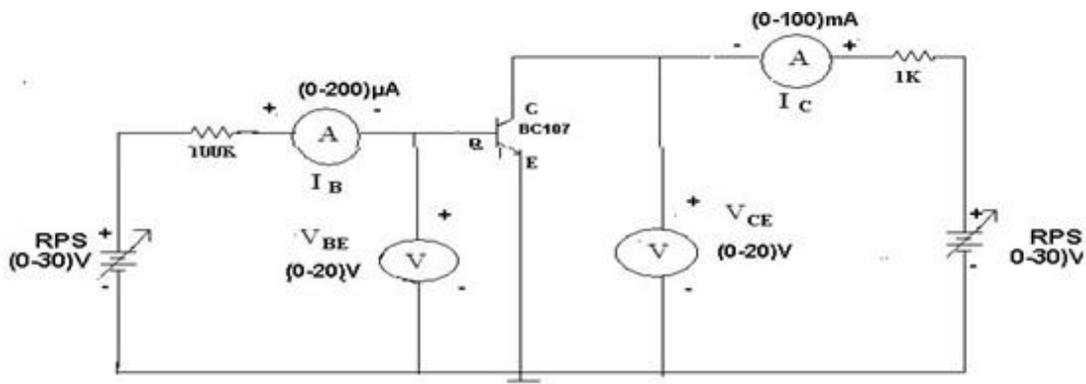
APPARATUS:

- | | |
|-----------------------------------|-------|
| 1. Transistor (BC107) | -1No. |
| 2. Regulated power supply (0-30V) | -1No. |
| 3. Voltmeter (0-20V) | -2No. |
| 4. Ammeters (0-20mA) | -1No. |
| 5. Ammeters (0-200 μ A) | -1No. |
| 6. Resistor (100 Ω) | -1No. |
| 7. Resistor (1K Ω) | -1No. |
| 8. Bread board | |
| 9. Connecting wires | |

THEORY:

The **common emitter (CE) configuration** is the most widely used transistor **configuration**. The **common emitter (CE)** amplifiers are used when large current gain is needed. The input signal is applied between the base and **emitter** terminals while the output signal is taken between the collector and **emitter** terminals.

CIRCUIT DIAGRAM:



PROCEDURE:

Input Characteristics:

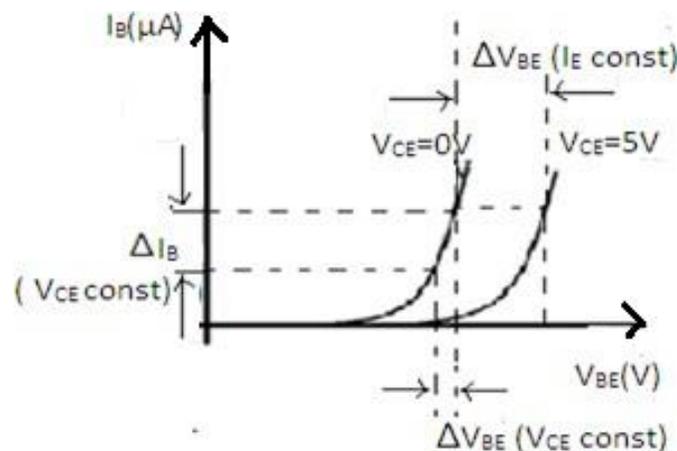
1. Connect the circuit as shown in the circuit diagram.
2. Keep output voltage $V_{CE} = 0V$ by varying V_{CC} .
3. Varying V_{BB} gradually, note down base current I_B and base-emitter voltage V_{BE} .
4. Step size is not fixed because of non linear curve. Initially vary V_{BB} in steps of $0.1V$. Once the current starts increasing vary V_{BB} in steps of $1V$ up to $12V$.
5. Repeat above procedure (step 3) for $V_{CE} = 5V$.

Output Characteristics:

1. Connect the circuit as shown in the circuit diagram.
2. Keep emitter current $I_B = 20\mu A$ by varying V_{BB} .
3. Varying V_{CC} gradually in steps of $1V$ up to $12V$ and note down collector current I_C and Collector-Emitter Voltage (V_{CE}).
4. Repeat above procedure (step 3) for $I_B = 60\mu A, 0\mu A$.

MODEL GRAPHS:

INPUT CHARACTERISTICS:



Calculations from Graph:

1. **Input Characteristics:** To obtain input resistance find ΔV_{BE} and ΔI_B for a constant V_{CE} on one of the input characteristics.

$$\text{Input impedance} = h_{ie} = R_i = \Delta V_{BE} / \Delta I_B \text{ (} V_{CE} \text{ is constant)}$$

$$\text{Reverse voltage gain} = h_{re} = \Delta V_{EB} / \Delta V_{CE} \text{ (} I_B = \text{constant)}$$

2. **Output Characteristics:** To obtain output resistance find ΔI_C and ΔV_{CB} at a constant I_B .

$$\text{Output admittance } 1/h_{oe} = R_o = \Delta I_C / \Delta V_{CE} \text{ (} I_B \text{ is constant)}$$

$$\text{Forward current gain} = h_{fe} = \Delta I_C / \Delta I_B \text{ (} V_{CE} = \text{constant)}$$

Precautions:

1. While performing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.
2. Connect voltmeter and ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base and collector terminals of the transistor.

Result:

Input and Output characteristics of a Transistor in Common Emitter Configuration are studied and find out the input resistance, output resistance, β .

Viva Questions:

1. Can transistor be replaced by two back to back connected diodes?
2. For amplification CE is preferred, why?
3. To operate a transistor as amplifier, emitter junction is forward biased and collector junction is reverse biased. Why?
4. Which transistor configuration provides a phase reversal between the input and output signals?
5. What is the range β of a BJT?

Experiment-8

Input and Output Characteristic of FET in CS Configuration

AIM:

1. To draw the drain and transfer characteristics of a given FET.
2. To find the drain resistance (r_d) amplification factor (μ) and Trans conductance (g_m) of the given FET.

APPARATUS:

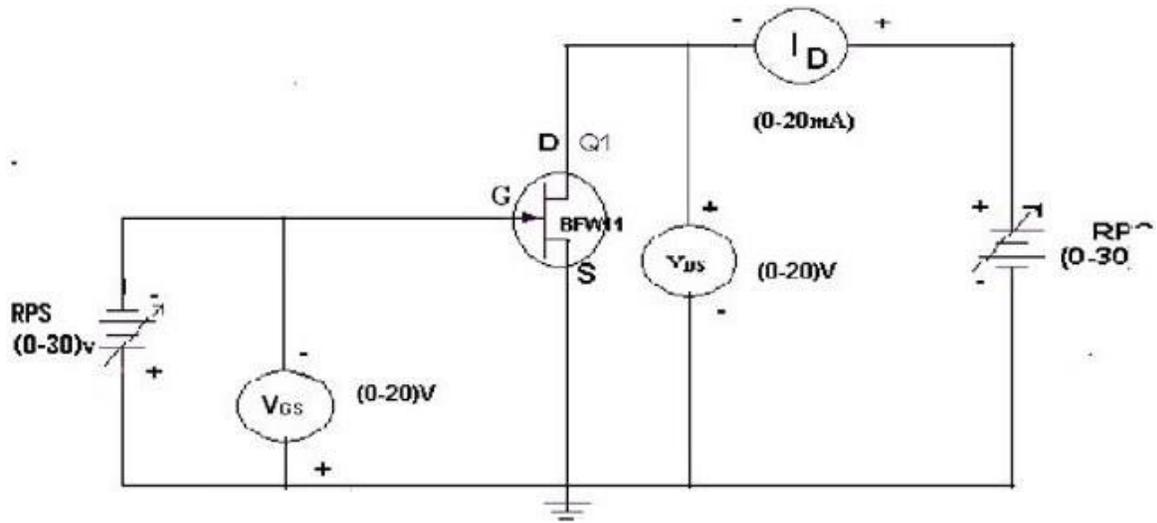
- | | |
|-----------------------------------|-------|
| 1. FET BFW10 | -1No. |
| 2. Regulated power supply (0-30V) | -1No. |
| 3. Voltmeter (0-20V) | -2No. |
| 4. Ammeter (0-20mA) | -1No. |
| 5. Bread board | |
| 6. Connecting wires | |

THEORY:

A FET is a three terminal device, in which current conduction is by majority carriers only. The flow of current is controlled by means of an Electric field. The three terminals of FET are Gate, Drain and Source. It is having the characteristics of high input impedance and less noise, the Gate to Source junction of the FETs always reverse biased. In response to small applied voltage from drain to source, the n-type bar acts as sample resistor, and the drain current increases linearly with V_{DS} . With increase in I_D the ohmic voltage drop between the source and the channel region reverse biases the junction and the conducting position of the channel begins to remain constant. The V_{DS} at this instant is called “pinch of voltage”. If the gate to source voltage (V_{GS}) is applied in the direction to provide additional reverse bias, the pinch off voltage will be decreased.

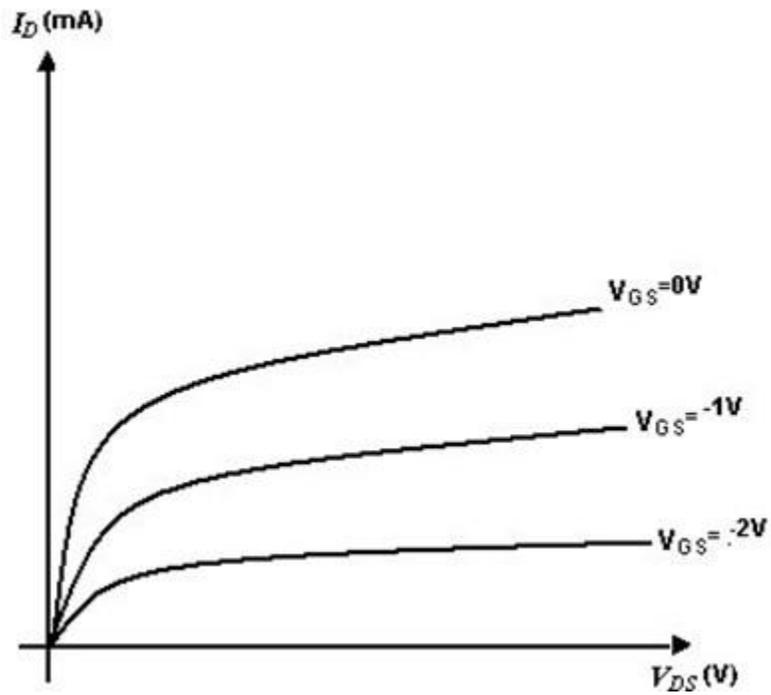
In amplifier application, the FET is always used in the region beyond the pinch-off.

CIRCUIT DIAGRAM:

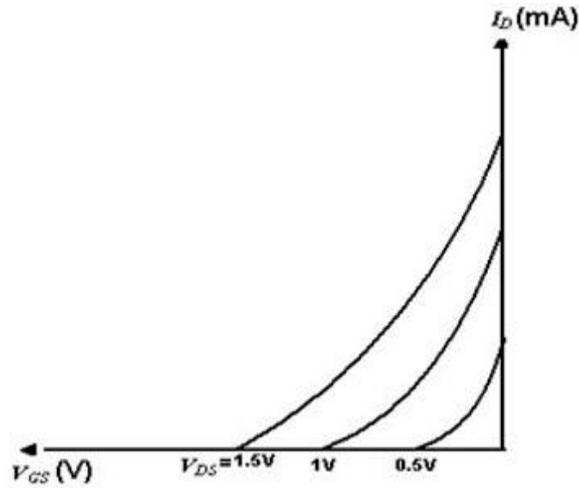


MODEL GRAPH:

DRAIN CHARACTERISTICS:



TRANSFER CHARACTERISTICS:



OBSERVATIONS:

DRAIN CHARACTERISTICS:

S.NO	$V_{GS}=0$		$V_{GS}= -1$		$V_{GS}= -2$	
	$V_{DS}(V)$	$I_D(mA)$	$V_{DS}(V)$	$I_D(mA)$	$V_{DS}(V)$	$I_D(mA)$

TRANSFER CHARACTERISTICS:

S.NO	$V_{DS}=0.5$		$V_{DS}= 1$		$V_{GS}= 1.5$	
	$V_{GS}(V)$	$I_D(mA)$	$V_{GS}(V)$	$I_D(mA)$	$V_{GS}(V)$	$I_D(mA)$

PROCEDURE:

1. All the connections are made as per the circuit diagram.
2. To plot the drain characteristics, keep V_{GS} constant at 0V.
3. Vary the V_{DD} and observe the values of V_{DS} and I_D .
4. Repeat the above steps 2, 3 for different values of V_{GS} at 0.1V and 0.2V.
5. All the readings are tabulated.
6. To plot the transfer characteristics, keep V_{DS} constant at 1V.
7. Vary V_{GG} and observe the values of V_{GS} and I_D .
8. Repeat steps 6 and 7 for different values of V_{DS} at 1.5 V and 2V.
9. The readings are tabulated
10. From drain characteristics, calculate the values of dynamic resistance (r_d)
11. From transfer characteristics, calculate the value of transconductance (g_m)
12. And also calculate Amplification factor (μ).

FET Parameters:

AC Drain Resistance, $r_d = \Delta V_{DS} / \Delta I_D$ at constant V_{GS}

Transconductance, $g_m = \Delta I_D / \Delta V_{GS}$ at constant V_{DS}

Amplification, $\mu = \Delta V_{DS} / \Delta V_{GS}$ at constant I_D

Relation between above parameters

$$\mu = r_d * g_m$$

The drain current is given by

$$I_D = I_{DSS} (1 - V_{GS}/V_P)^2$$

PRECAUTIONS:

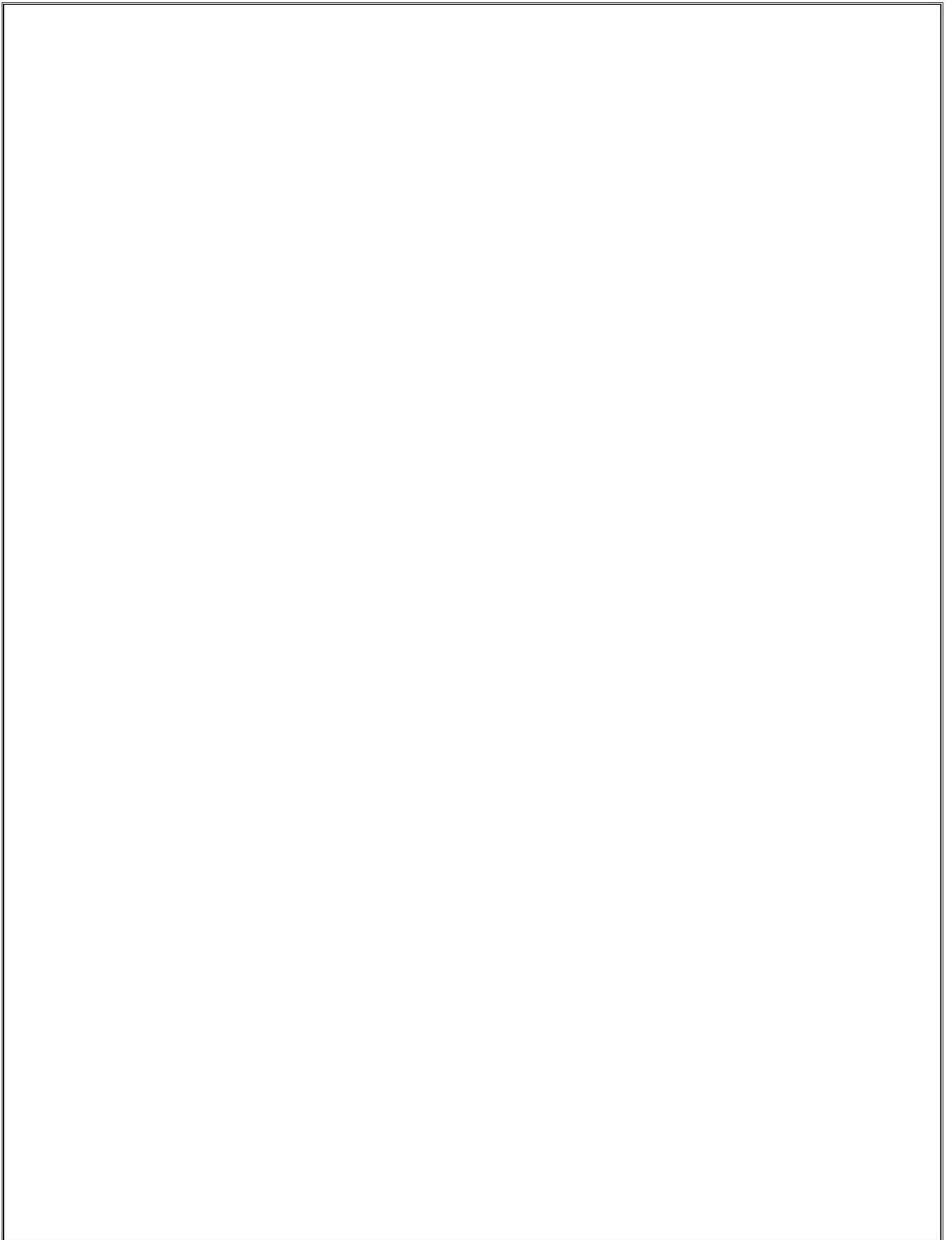
1. The three terminals of the FET must be carefully identified
2. Practically FET contains four terminals, which are called source, drain, Gate, substrate.
3. Source and case should be short circuited.
4. Voltages exceeding the ratings of the FET should not be applied.

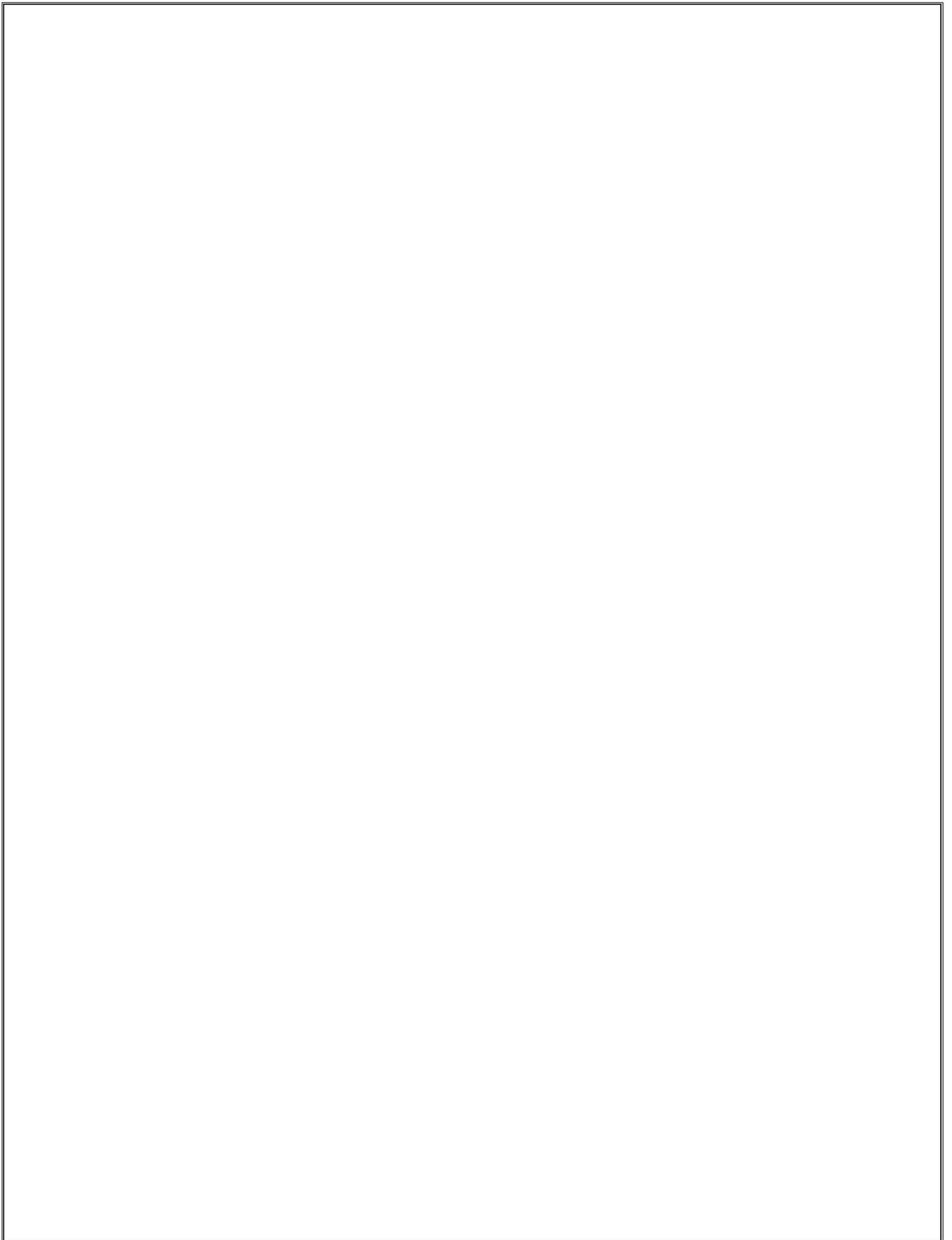
RESULT:

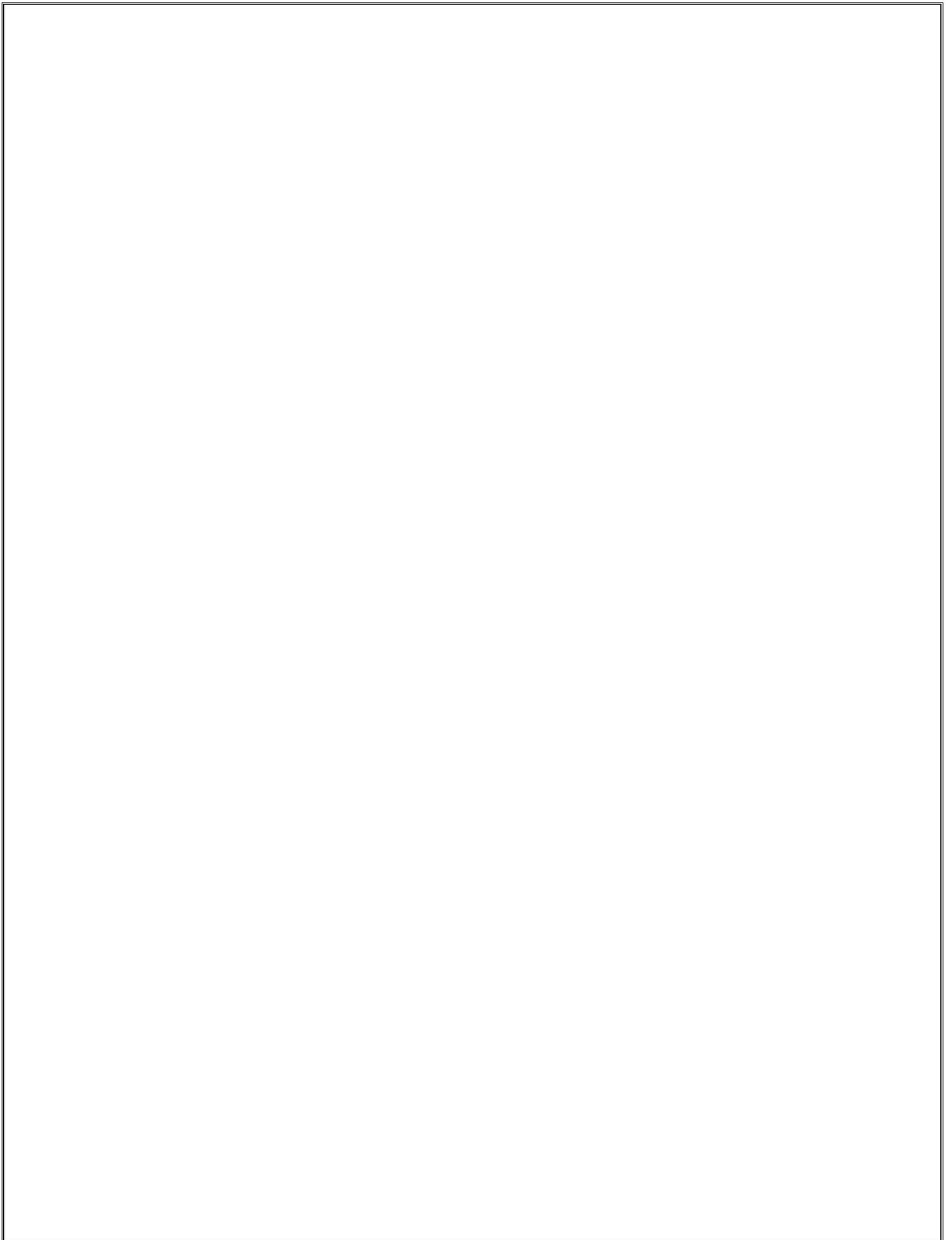
We have drawn the drain and transfer characteristics of a given FET. And We have found the drain resistance (r_d) amplification factor (μ) and Trans Conductance (g_m) of the given FET.

VIVA QUESTIONS:

1. What are the advantages of FET?
2. Different between FET and BJT?
3. Explain different regions of V-I characteristics of FET?
4. What are the applications of FET?
5. What are the types of FET?
6. Draw the symbol of FET.
7. What are the disadvantages of FET?







Experiment-9

Switching Characteristics of a Transistor

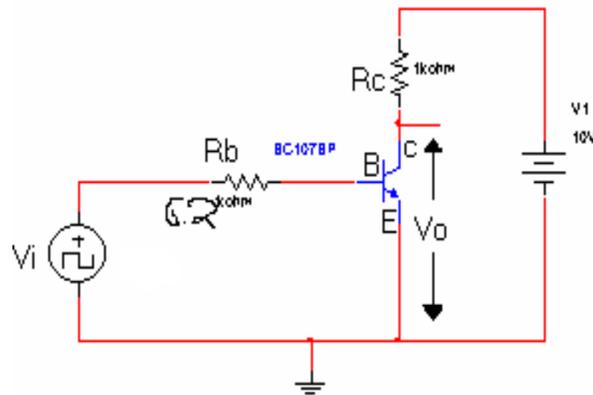
Aim:

1. To study the Switching characteristics of a transistor.
2. Design Transistor to act as a Switch and verify the operation. Choose $V_{CC} = 10V$, $I_{Cmax} = 10 \text{ mA}$, $h_{fe} = 50$, $V_{CESat} = 0.2V$, $V_{in} = 4V_{p-p}$, $V_{BESat} = 0.6 \text{ V}$.

Apparatus:

1.	CRO 0 – 20 MHz (Dual Channel)	1No.
2.	Function Generator 1Hz– 1 MHz	1No.
3.	Resistor (1kohm,8.2kohm)	1No. each
4.	Transistor (BC 107)	1No.
5.	D.C Power Supply 0-30V (dual)	1No.
6.	Connecting wires	
7.	Bread board	

Circuit diagram:



Theory:

The Transistor can act as a switch. To operate the transistor as a switch, it has to be operated in saturation region for **ON** state and to be operated in cut off region for **OFF** state.

When the Input voltage V_i is negative or zero, transistor is cut-off and no current flows through R_c . Hence V_o is approximately equal to V_{CC} . When Input Voltage V_i is changed to positive voltage, transistor will be driven into saturation. Then, $V_o = V_{CC} - I_c R_c \cong V_{CESat}$, which is a very small voltage.

Design procedure:

When Transistor is ON, $R_C = (V_{CC} - V_{CEsat})/I_{Cmax}$

$$= (10 - 0.2) / 10\text{mA}$$

$$= 1\text{K}\Omega$$

$$I_B \geq I_{Cmax} / h_{fe}$$

$$\geq 10\text{mA} / 50$$

$$I_B \geq 0.2\text{mA}$$

To keep transistor remain in ON, I_B should be greater then $I_{Bmin} = 0.2\text{mA}$

$$V_{in} = I_B R_B + V_{BEsat}$$

$$2\text{V} = 0.2\text{mA} \cdot R_B + 0.6\text{V}$$

$$R_B = 7\text{K}\Omega \text{ (Choose Practical values as } 8.2\text{K}\Omega)$$

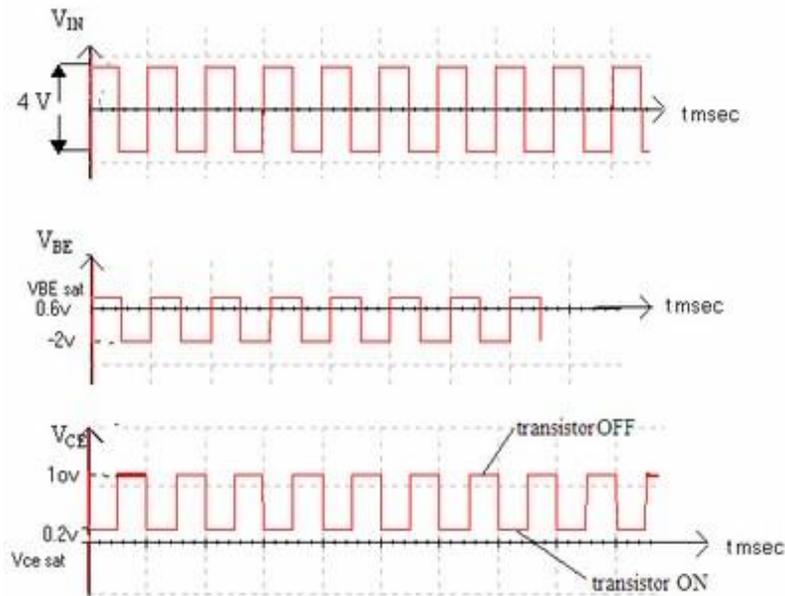
Procedure:

1. Connect the circuit as shown in the above figure.
2. Apply the Square wave of 4 Vp-p at frequency of 1 KHz
3. Observe the waveforms at Collector and Base of the transistor and plot it.

Precautions:

1. Keep the CRO in DC mode while measuring the Output waveform at collector and base,
2. For measuring $V_{BE\text{ Sat}}$ and $V_{CE\text{ Sat}}$ keep volts/div switch at either 0.2 or 0.5 position.
3. When the square wave is being applied, ensure that there is no DC voltage in that. This can be checked by CRO in either in AC or DC mode. There should not be any jumps/distortion in waveform on the screen.

Waveforms:



Result:

Transistor as a switch has been designed operated and Output waveforms are observed.

Viva Questions:

1. Mention typical values of $V_{BE Sat}$, $V_{CE Sat}$ for both Si, Ge Transistors?
2. Define ON time and OFF time of the transistor?
3. In which regions Transistor acts as a switch?
4. Define Rise time & fall time of a transistor switch?
5. Define Storage time and delay time?
6. What is the phase difference between the input and the output, when the transistor is conducting?

Experiment-11

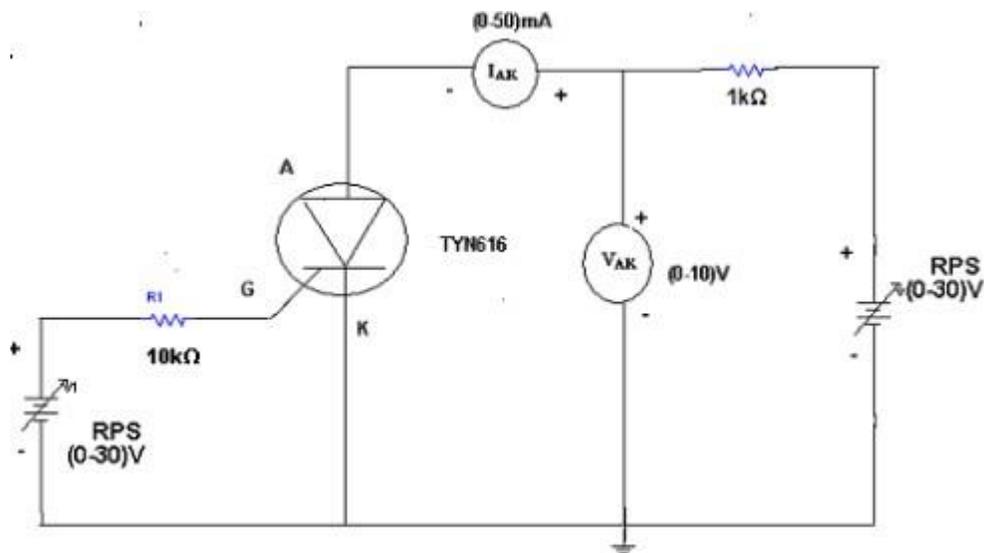
Silicon-Controlled Rectifier (SCR) Characteristics

Aim: To draw the V-I Characteristics of Silicon controlled rectifier.

Apparatus:

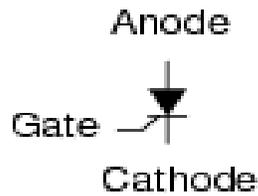
1. SCR (TYN616)
2. Regulated Power Supply (0-30V)
3. Resistors $10k\Omega$, $1k\Omega$
4. Ammeter (0-50)mA
5. Voltmeter (0-20V)
6. Breadboard
7. Connecting Wires.

Circuit Diagram:



Theory:

It is a four layer semiconductor device being alternate of P-type and N-type silicon. It consists of 3 junctions J_1 , J_2 , J_3 the J_1 and J_3 operate in forward direction and J_2 operates in reverse direction and three terminals called anode A, cathode K, and a gate G. The operation of SCR can be studied when the gate is open and when the gate is positive with respect to cathode.



Schematic symbol

When gate is open, no voltage is applied at the gate due to reverse bias of the junction J_2 no current flows through R_2 and hence SCR is at cutoff. When anode voltage is increased J_2 tends to breakdown.

When the gate positive, with respect to cathode J_3 junction is forward biased and J_2 is reverse biased. Electrons from N-type material move across junction J_3 towards gate while holes from P-type material moves across junction J_3 towards cathode. So gate current starts flowing, anode current increase is in extremely small current junction J_2 break down and SCR conducts heavily.

When gate is open the break over voltage is determined on the minimum forward voltage at which SCR conducts heavily. Now most of the supply voltage appears across the load resistance. The holding current is the maximum anode current gate being open, when break over occurs.

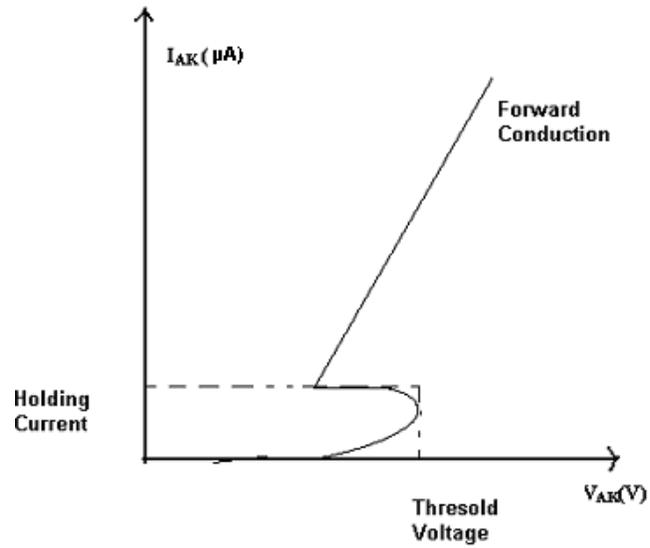
Procedure:

1. Connections are made as per circuit diagram.
2. Keep the gate supply voltage at some constant value
3. Vary the anode to cathode supply voltage and note down the readings of voltmeter and ammeter. Keep the gate voltage at standard value.
4. A graph is drawn between V_{AK} and I_{AK} .

Observation:

$V_{AK}(V)$	$I_{AK} (\mu A)$

Model Waveforms:



Result: SCR Characteristics are observed.

Viva questions:

1. What is an SCR?
2. What is the difference between SCR and TRIAC?
3. What are the applications of SCR?
4. Why is Peak Reverse Voltage Important?
5. What is asymmetrical SCR?

Experiment-3

Types of Clippers at different reference voltages

Aim:-

- a) To study the clipping circuits using diodes
- b) To observe the transfer characteristics of all the clipping circuits in CRO.

Apparatus:-

1. Signal Generator.
2. Bread board
3. Connecting patch cards.
4. CRO
5. DC power supply (dual)
6. Resistors (1 K Ω , 10K Ω)
7. Diodes (1N4007)

Theory:-

Clipping circuits basically limit the amplitude of the input signal either below or above certain voltage level. They are referred to as Voltage limiters, Amplitude selectors or Slicers. A clipping circuit is one, in which a small section of input waveform is missing or cut or truncated at the output section. Clipping circuits are classified based on the position of Diode.

1. Series Diode Clipper

2. Shunt Diode Clipper

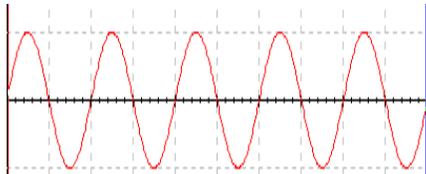
Procedure:-

1. Connect the circuit as shown in fig.1
2. In each case apply 10 V_{P-P}, 1KHz Sine wave I/P using a signal generator.
3. Observe the O/P waveform on the CRO in comparison with I/P waveform.
4. Sketch the I/P as well as O/P waveforms and mark the numerical values.
5. Note the changes in the O/P due to variations in the reference voltage $V_R = 2V, 3V$.
6. O/P is taken across the load R_L .
7. Obtain the transfer characteristics of Fig.1, by keeping CRO in X-Y plane.
8. Repeat the above steps for all the figures.

Precautions:

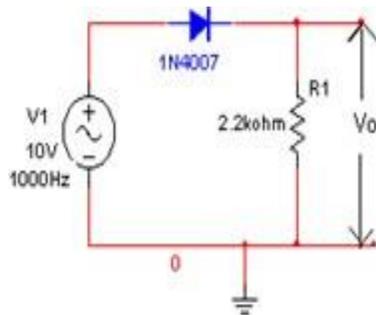
1. Set the CRO O/P channel in DC mode always.
2. Observe the waveform simultaneously by keeping common ground.
3. See that there is no DC component in the I/P.
4. To find transfer characteristics apply input to the X-Channel, OP to Y-Channel, adjust the dot at the center of the screen when CRO is in X-Y mode. Both the channels modes must be in ground, then remove ground and plot the transfer characteristics.

Input Waveform:

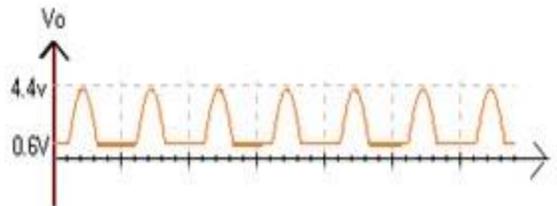


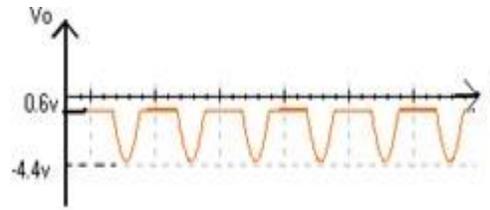
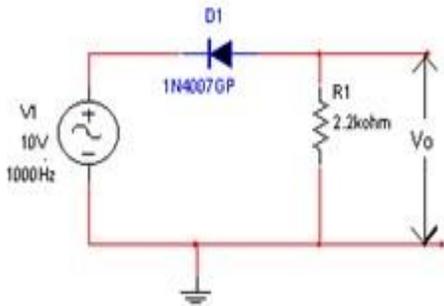
Series Diode clippers:

CIRCUIT DIAGRAM



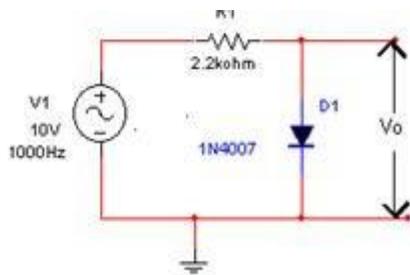
O/P WAVEFORMS



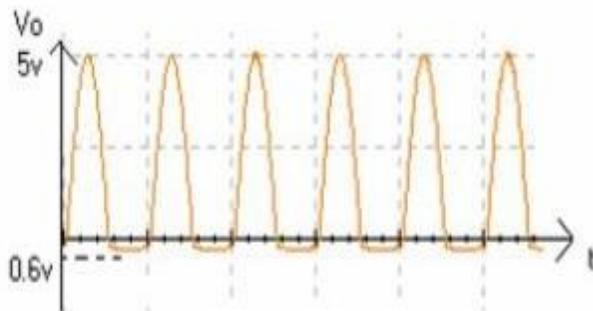
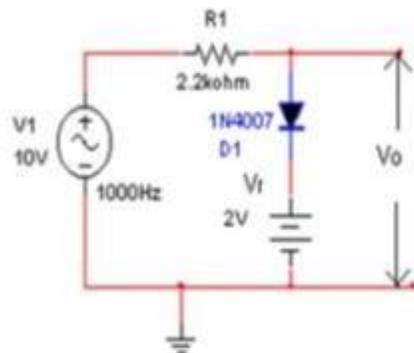
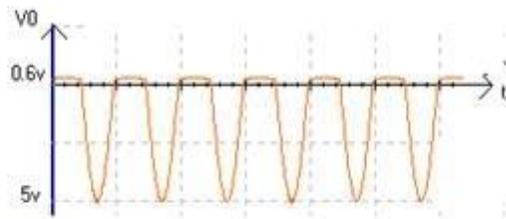


Shunt diode clippers:

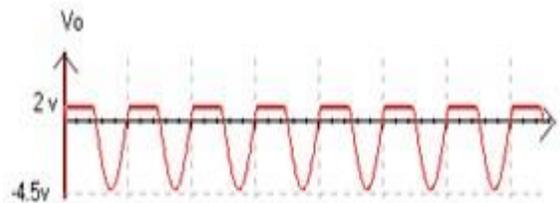
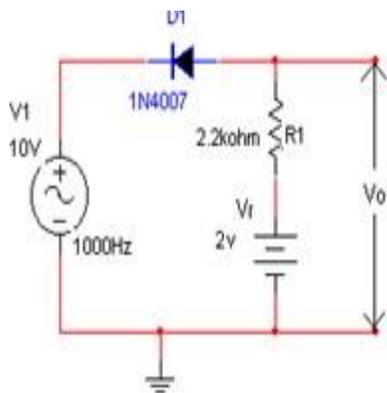
CIRCUIT DIAGRAM

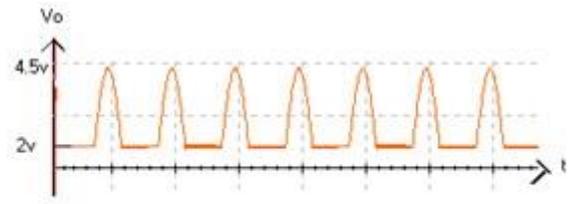
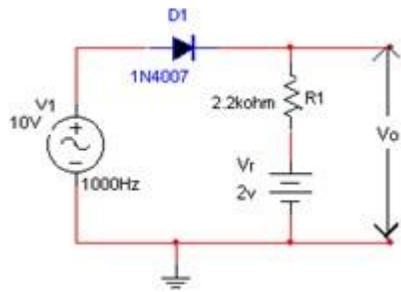


O/P WAVEFORMS

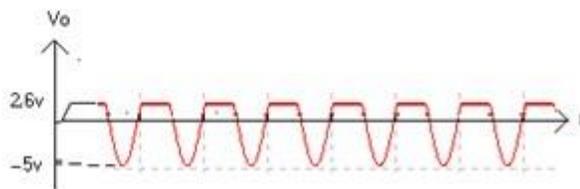
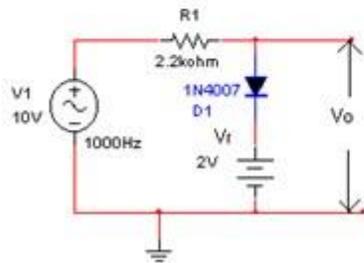
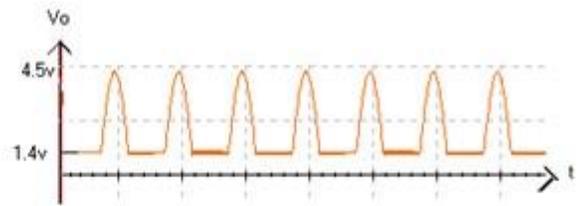
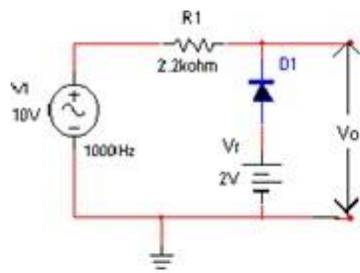


Series diode clipper with bias:

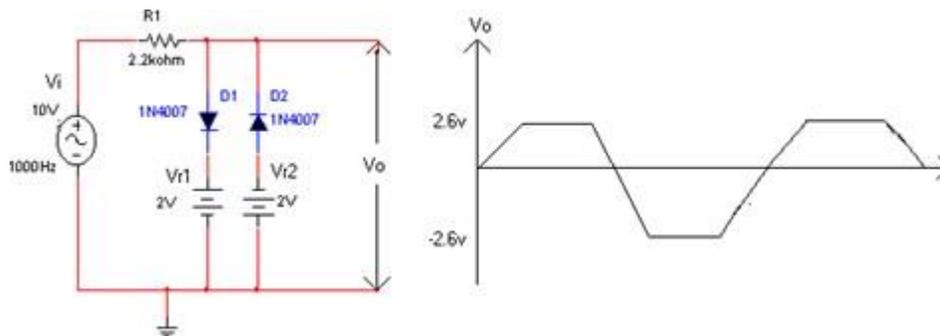




Shunt diode clipper with bias:



Slicer:



Result:-

Different types of clipping circuits have been studied and observed the responses for various combinations of V_R and clipping diodes.

Viva Questions:-

1. What is a clipping circuit?
 2. What is piecewise linear mode of a diode?.
 3. What is a break region?.
 4. What is the significance of zero slope?
 5. In a clipper circuit what is the function of non-linear device ?
- Compare the Series & Shunt Clippers.

Experiment-4

Types of Clampers at different reference voltages

Aim:-

To study the clamping circuits using diodes and capacitors.

Apparatus:-

1. Signal Generator.
2. Bread board
3. Connecting patch cards.
4. CRO
5. DC power supply (dual)
6. Resistors (100 K Ω)
7. Diodes (1N4007)
8. Capacitor (0.1 μ f)

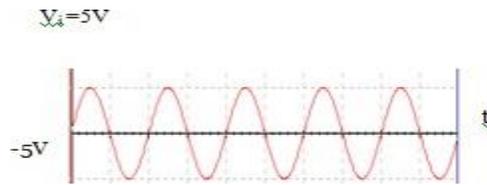
Theory:-

Clamping circuits add a DC level to an AC signal. A clamper is also refer to as DC restorer or DC re-inserter. The Clampers which clamp the given waveform either above or below the reference level, which are known as positive or negative clamping respectively.

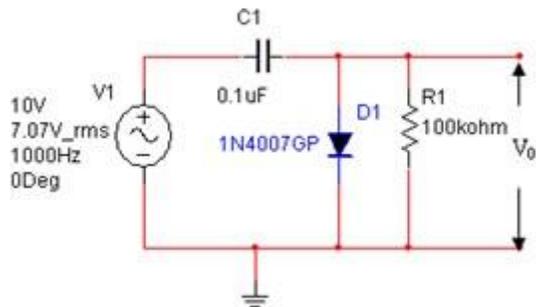
Procedure:-

1. Connect the circuit as shown in fig (1)
2. Apply a Sine wave of 10V_{P-P}, 1KHz at the input terminals with the help of Signal Generator.
3. Observe the I/P & O/P waveforms of CRO and plot the waveforms and mark the values with $V_R = 2\text{ V}, 3\text{V}$
4. O/P is taken across the load R_L .
5. Repeat the above steps for all clamping circuits as shown.
6. Waveforms are drawn assuming diode is ideal.

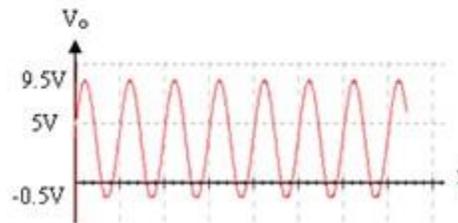
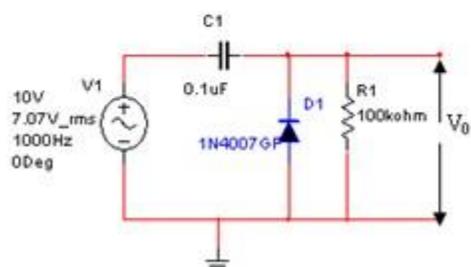
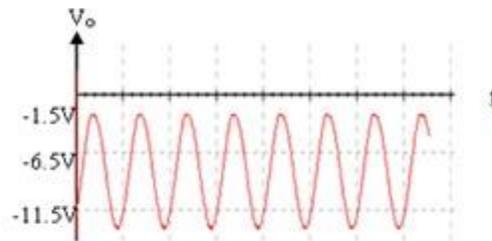
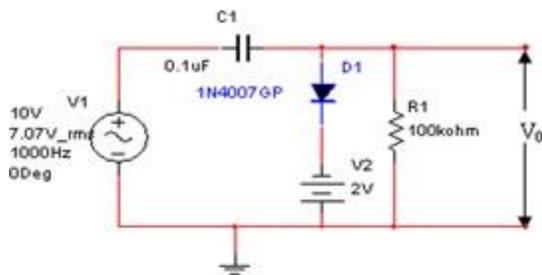
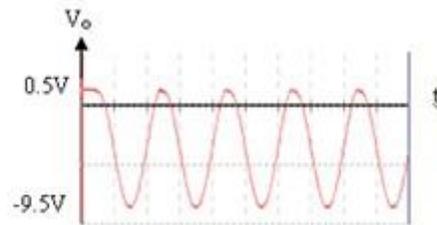
Input Waveform:-

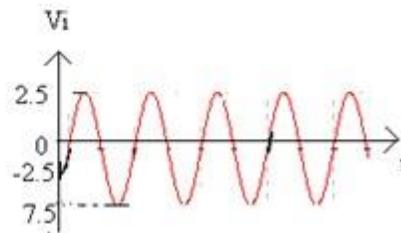
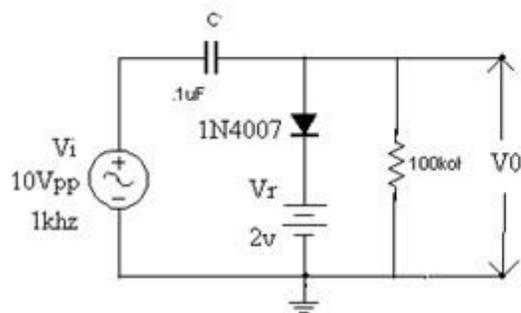
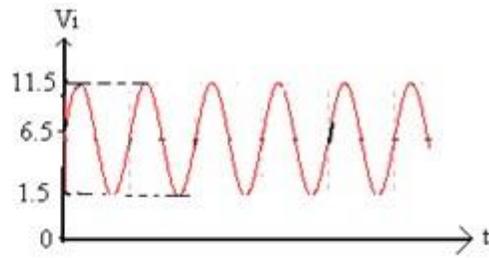
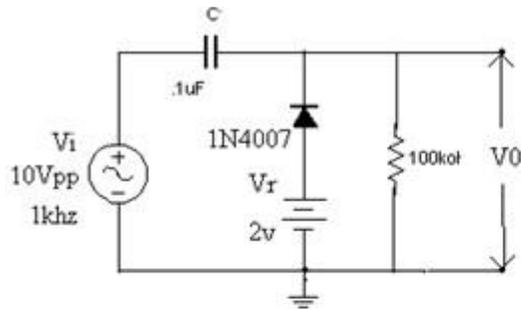


CIRCUIT DIAGRAM



O/P WAVEFORMS





Result:

Different types of clamping circuits are studied and observed the response for different combinations of V_R and diodes.

Viva Questions:-

1. What are the applications of clamping circuits?
2. What is the synchronized clamping?
3. Why a clamper is called a dc inserter?
4. What is modified clamping circuit theorem?
5. Differentiate -ve clamping circuit from +ve clamping circuits in the above circuits?.
6. Describe the charging and discharging of a capacitor in each circuit?

Experiment-5

The steady state output waveform of clampers for a square wave input

Aim:-

To study the clamping circuits using diodes and capacitors for a square wave input.

Apparatus:-

1. Signal Generator.
2. Bread board
3. Connecting patch cards.
4. CRO
5. DC power supply (dual)
6. Resistors (100 K Ω)
7. Diodes (1N4007)
8. Capacitor (0.1 μ f)

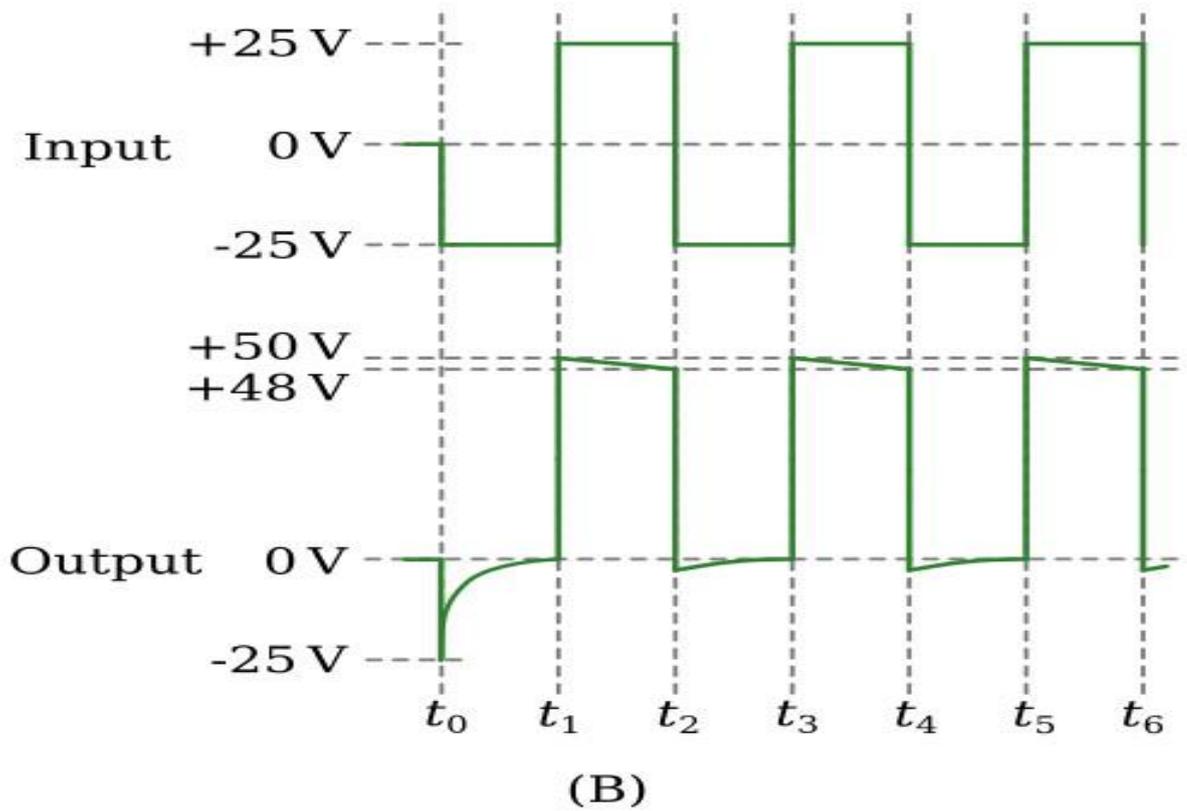
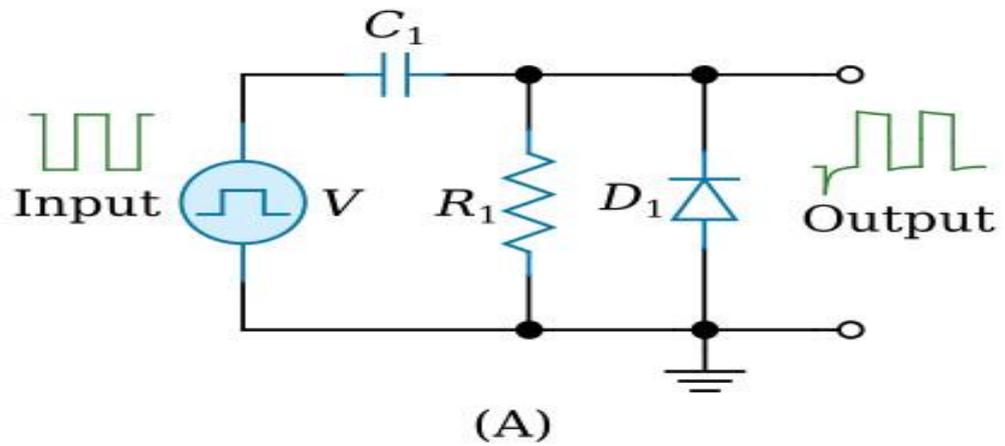
Theory:-

Clamping circuits add a DC level to an AC signal. A clamper is also refer to as DC restorer or DC re-inserter. The Clampers which clamp the given waveform either above or below the reference level, which are known as positive or negative clamping respectively.

Procedure:-

1. Connect the circuit as shown in fig (1)
2. Apply a Square wave of $2V_{P-P}$, 1KHz at the input terminals with the help of Signal Generator.
3. Observe the I/P & O/P waveforms of CRO and plot the waveforms and mark the values with $V_R = 2 V, 3V$
4. O/P is taken across the load R_L .
5. Repeat the above steps for all clamping circuits as shown.
6. Waveforms are drawn assuming diode is ideal.

CIRCUIT DIAGRAM:



Result:-

Different types of clamping circuits are studied and observed the response for different combinations of V_R and diodes.

Viva Questions:

1. What are the applications of clamping circuits?
2. What is the synchronized clamping?
3. Why a clamper is called a dc inserter?
4. What is modified clamping circuit theorem?
5. Differentiate -ve clamping circuit from +ve clamping circuits in the above circuits?.
6. Describe the charging and discharging of a capacitor in each circuit?

Experiment-12

UJT characteristics and identify negative region

AIM:

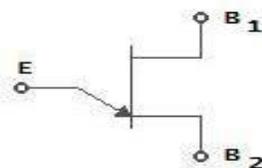
Demonstrate the Volt-ampere characteristics of silicon-controlled rectifier.

APPARATUS:

S. No.	Device	Range/ Rating	Quantity
1	UJT Trainer Board Containing a) DC Power Supply b) Resistor c) UJT	0-30V 100Ω 100KΩ	1 2 1 1
2	DC voltmeter	(0-20) V	2
3	DC ammeter	(0-200) mA (0-200)μA	1 1
4	Connecting wires	5A	10

THEORY

A Unijunction Transistor (UJT) is an electronic semiconductor device that has only one junction. The UJT Unijunction Transistor (UJT) has three terminals an emitter (E) and two bases (B1 and B2). The base is formed by lightly doped n-type bar of silicon. Two ohmic contacts B1 and B2 are attached at its ends. The emitter is of p-type and it is heavily doped. The resistance between B1 and B2, when the emitter is open-circuit is called interbase resistance. The original unijunction transistor, or UJT, is a simple device that is essentially a bar of N type semiconductor material into which P type material has been diffused somewhere along its length. The 2N2646 is the most commonly used version of the UJT.



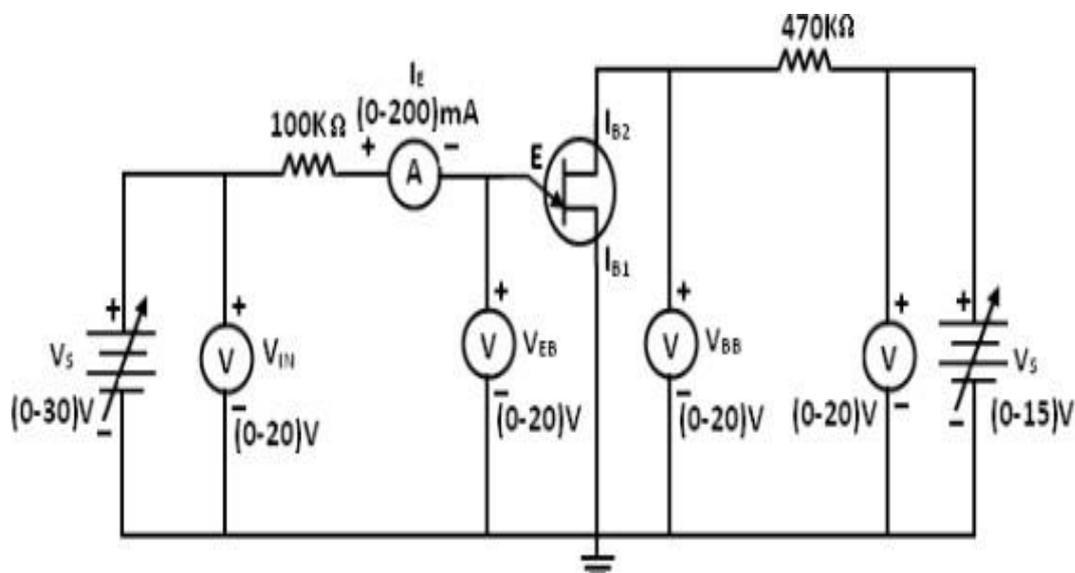
Circuit symbol

The UJT is biased with a positive voltage between the two bases. This causes a potential drop along the length of the device. When the emitter voltage is driven approximately one diode voltage above the voltage at the point where the P diffusion (emitter) is, current will begin to flow from the emitter into the base region. Because the base region is very lightly doped, the additional current (actually charges in the base region) causes (conductivity modulation) which reduces the resistance of the portion of the base between the emitter junction and the B2 terminal. This reduction in resistance means that the emitter junction is more forward biased, and so even more current is injected. Overall, the effect is a negative resistance at the emitter terminal. This is what makes the UJT useful, especially in simple oscillator circuits. When the emitter voltage reaches V_p , the current starts to increase and the emitter voltage starts to decrease. This is represented by negative slope of the characteristics which is referred to as the negative resistance region, beyond the valley point, R_{B1} reaches minimum value and this region, V_{EB} proportional to I_E .

PROCEDURE:

- Connection is made as per circuit diagram.
- Output voltage is fixed at a constant level and by varying input voltage corresponding emitter current values are noted down.
- This procedure is repeated for different values of output voltages.
- All the readings are tabulated and Intrinsic Stand-Off ratio is calculated using
 - $\eta = (V_p - V_D) / V_{BB}$
- A graph is plotted between V_{EE} and I_E for different values of V_{BE} .

CIRCUIT DIAGRAM:



CALCULATIONS:

1. $V_P = \eta V_{BB} + V_D$
2. $\eta = (V_P - V_D) / V_{BB}$
3. $\eta = (\eta_1 + \eta_2 + \eta_3) / 3$

RESULT:

The characteristics of UJT are observed and the values of Intrinsic Stand-Off Ratio are calculated.

Viva questions:

1. What is the difference between FET and UJT?
2. Is UJT is used an oscillator? Why?
3. What is the Resistance between B_1 and B_2 is called as?
4. What is its value of resistance between B_1 and B_2 ?
5. Draw the characteristics of UJT?
6. What is the symbol of UJT?
7. Draw the equivalent circuit of UJT?
8. What are the applications of UJT?
9. Formula for the intrinsic standoff ratio?
10. What does it indicates the direction of arrow in the UJT?

Experiment-6

Input output characteristics of BJT in CB configuration

AIM:

Plot the input and output characteristics of a transistor connected in Common Base configuration. Calculate the input resistance R_i at $I_e = 12 \text{ mA}$, output resistance R_o at $V_{CB} = 8\text{V}$ and current gain at $V_{CB} = 6\text{V}$.

APPARATUS:

S.No	Device	Range /Rating	Quantity (in No.s)
1.	Transistor CB trainer Board Containing a) DC Power Supply. b) PNP Transistor c) Carbon Film Resistor	(0-12) V CK100 470 Ω , 1/2 W	2 1 2
2.	a) DC Voltmeter b) DC Voltmeter	(0-1) V (0-20) V	1 1
3.	DC Ammeter	(0-50) mA	2
4.	Connecting wires	5A	12

THEORY:

A transistor is a three terminal active device. The terminals are emitter, base, collector. In CB configuration, the base is common to both input (emitter) and output (collector). For normal operation, the E-B junction is forward biased and C-B junction is reverse biased.

In CB configuration, I_E is +ve, I_C is -ve and I_B is -ve.

So, $V_{EB} = f_1(V_{CB}, I_E)$ and $I_C = f_2(V_{CB}, I_B)$

With an increasing the reverse collector voltage, the space-charge width at the output junction increases and the effective base width „W“ decreases. This phenomenon is known as “Early effect”. Then, there will be less chance for recombination within the base region. With increase of charge gradient within the base region, the current of minority carriers injected across the emitter junction increases. The current amplification factor of CB configuration is given by, $\alpha = \Delta I_C / \Delta I_E$

PROCEDURE

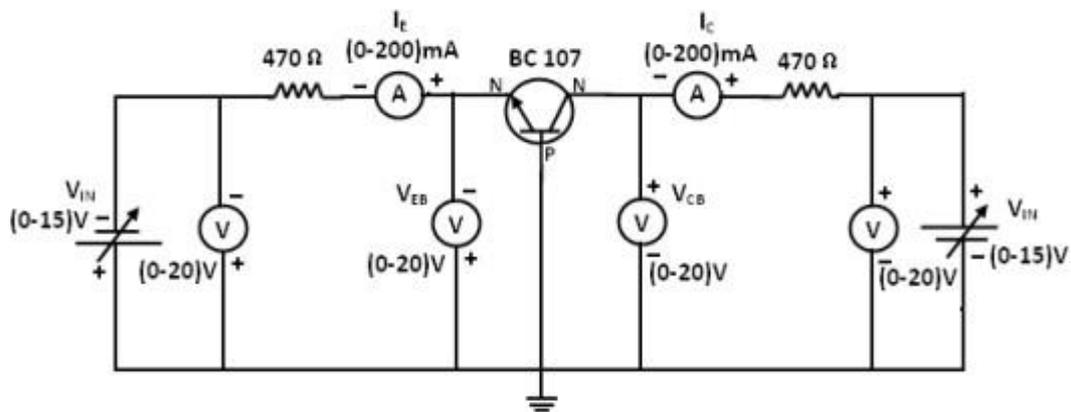
Input Characteristics:

1. Connect the transistor as shown in figure.
2. Keep the V_{CB} constant at 4V and 8V. Vary the V_{EB} in steps and note corresponding I_E values as per tabular form.

Output Characteristics:

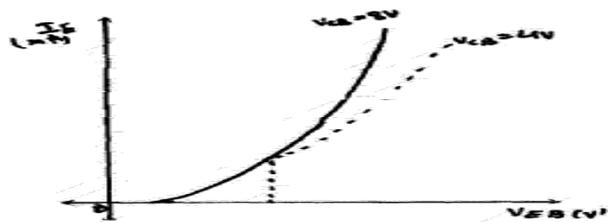
1. Keep the I_E constant at 4mA and 8mA. Vary the V_{CB} in steps and note corresponding I_C values.
2. Readings are tabulated as shown in tabular column.

CIRCUIT DIAGRAM:

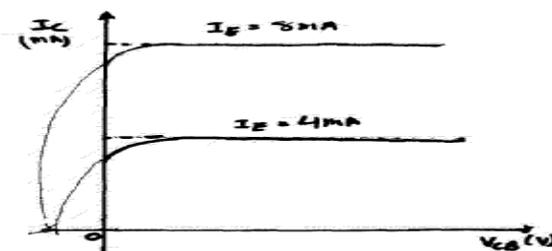


EXPECTED GRAPHS

Input Characteristics



Output characteristics



H-parameter calculations

$$h_{ib} = \Delta V_{cb} / \Delta I_e =$$

$$h_{ob} = \Delta I_c / \Delta V_{cb}$$

$$= h_{fb} = \Delta I_c / \Delta I_e$$

$$= h_{rb} = \Delta V_{cb} / \Delta$$

$$V_{cb} =$$

RESULT

Input and output curves are plotted.

1. R_i Input Resistance:

(i) $V_{EB} = 4V$ and $I_E = 12 \text{ mA}$, $R_i =$

(ii) $V_{EB} = 8V$ and $I_E = 12 \text{ mA}$, $R_i =$

2. R_o Output Resistance:

(i) $V_{CB} = 8V$ and $I_E = 8 \text{ mA}$, $R_o =$

(ii) $V_{CB} = 8V$ and $I_E = 4 \text{ mA}$, $R_o =$

3. Current Amplification factor

„ α “ = (at $V_{CB} = 6V$)

Viva questions:

1. What are the applications of CB configuration?
2. What are the input and output impedances of CB configuration?
3. Define α (alpha)?
4. What is EARLY effect?
5. What is the power gain of CB configuration

Experiment-13

LED characteristics

AIM: To study the V-I and L-I characteristics of LED

APPARATUS:

1. Light emitting diode
2. 0-5V variable Supply for Light emitting diode
3. 20mW Digital Optical power meter to measure optical power of Light emitting diode
4. 20V Digital Voltmeter to measure voltage across Light emitting diode
5. 200mA DC Digital Ammeter to measure Light emitting diode Current

THEORY: - A P- N junction diode, which emits light on forward biasing, is known as light emitting diode. The emitted light may be in the visible range or invisible range and the intensity of light depends on the applied potential. In a P N junction charge carrier recombination takes place when the electrons cross from the N-layer to the P-layer. The electrons are in the conduction band on the N-side while holes are in the valence band on the P-side. The conduction band has a higher energy level compared to the valence band and so when the electrons recombine with a hole the difference in energy is given out in the form of heat or light. In case of silicon or germanium, the energy dissipation is in the form of heat, whereas in case of gallium-arsenide and gallium phosphate, it is in the form of light. But this light is in the invisible region & so this material cannot be used in the manufacture of LED. Hence gallium – arsenide phosphate which emits light in the visible region is used to manufacture an LED.

CONSTRUCTION: -An n-type layer is grown on a substance and a p-type layer is grown over it by diffusion process. The P-layer is kept at the top because carrier recombination takes place in it. The terminals anode and cathode are taken out of the n-layer and P-layer respectively. The anode connections are made at the edge in order to provide more surface area for the emission of light. A metal film is applied to the bottom of substance to reflect light to the surface of the device and also to provide connection for the cathode terminal. Finally the structure is provided with an encapsulated (cover) to protect them from destruction.

ADVANTAGE: -

1. Works on low voltage and current and hence consumes less power.
2. Require no warm up time.
3. Can be switched ON and OFF at a faster rate.
4. Long lifetime.
5. Small size and less weight.

APPLICATIONS: -

1. Infra red LEDs are used in burglar alarms.
2. Used in solid state video displays.
3. Used in the field of optical communication.
4. Used in image sensing circuits.
5. Used in numerical displays like watches, pocket calculators etc.

Experimental Procedure

Procedure for V-I characteristics of a Light emitting diode:

1. Connect the Light emitting diode circuit as shown below:

0-5V Variable Supply

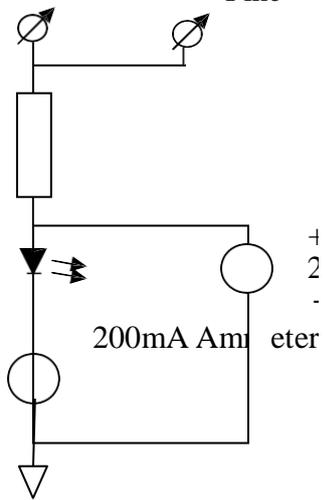
Coarse

Fine

100Ω

LED

+
-



V DVM

0-5V Variable Supply

Coarse

Fine

100Ω

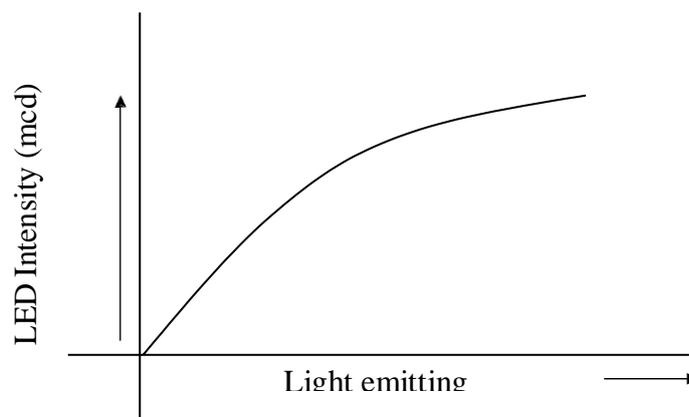
LED

Inbuilt Optical power meter (2000 mcd)

200mA Ammeter

Table 2:

S.NO.	Current(mA)	Power (mcd)



Experiment-14

Solar cell characteristics

AIM: To plot the V-I characteristics of Solar cell.

MICRO BOARD CONSISTS OF:

1. Solar Cell/Photovoltaic cell mounted on the wooden base.
2. Single directional mercury coated variable intensity source.
3. Voltmeter.
4. Ammeter.
5. Load resistance.

THEORY:

Sunlight consists of little particles of solar energy called photons. As the photovoltaic cell is exposed this sunlight, many of the photons are reflected, pass right through or absorbed by the solar cell.

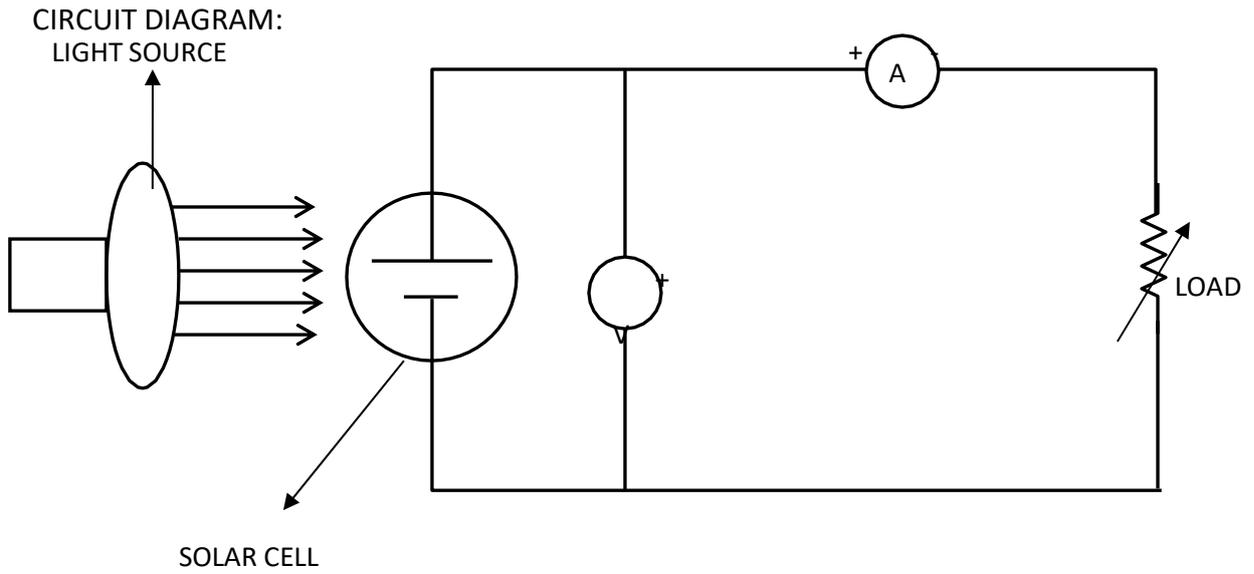
When enough photons are absorbed by the negative layer of the photovoltaic cell, electrons are freed from the negative semiconductor material. Due to the manufacturing process of the positive layer, these freed electrons naturally migrate to the positive layer creating a voltage differential, similar to a household battery.

When the 2 layers are connected to an external load the electrons flow through the circuit create electricity. Each individual solar energy cell produces only 1-2 watts. To increase power output, cells are combined in a weather-tight package called a solar module. These modules (from one to several thousand) are then wired up in serial and/or parallel with one another, into what's called a solar array, to create the desired voltage and amperage output required.

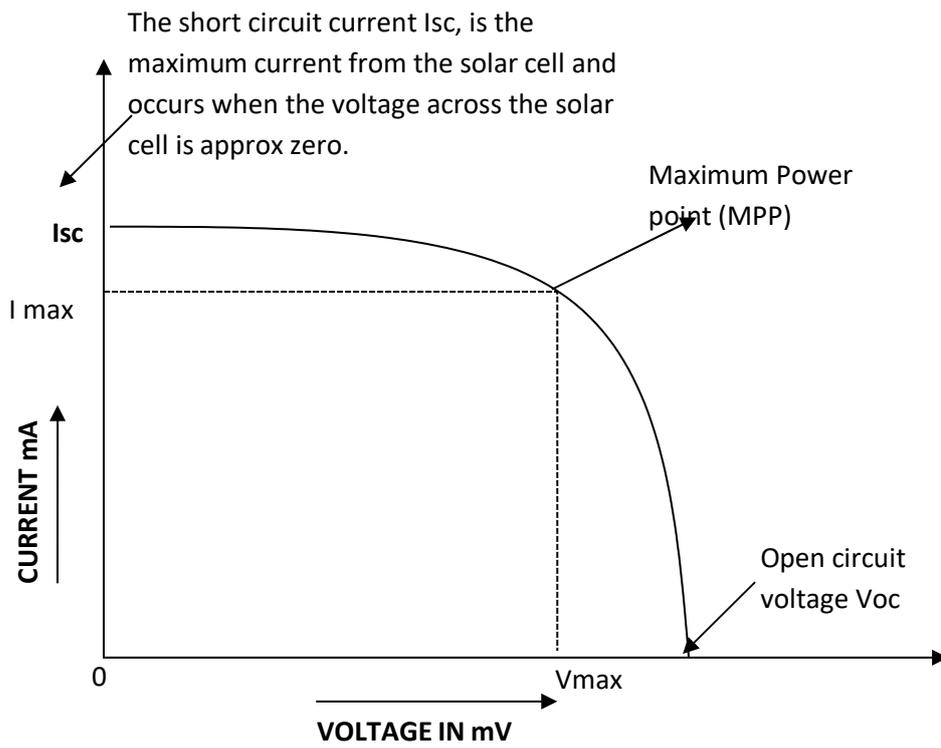
Due to the natural abundance of silicon, the semi-conductor material that PV cells are primarily made of, and the practically unlimited resource in the sun, solar power cells are very environmentally friendly. They burn no fuel and have absolutely no moving parts which makes them virtually maintenance free, clean, and silent.

PROCEDURE:

1. Connect the circuit as per the circuit diagram shown in fig (1).
2. Place the solar cell at a particular distance say 1cm from the variable light source.
3. Vary intensity of the light source, note down the voltage and current in the tabular column.
4. Next note the short circuit current I_{sc} , when the voltage across the solar cell is zero & open circuit voltage V_o by removing the load resistance across the solar cell.
5. Calculate power $P=VI$ for each reading.
6. Plot the graph between the voltage Vs Current , mark the maximum power point,
7. Repeat the experiment by changing the distance between the solar cell & lightsource.



IDEAL GRAPH:



TABULAR COLUMN:

Sl.No	Distance between the light source & solar cell in cms	Voltage (mv)	Current (mA)	P=VI

OBSERVATION:

1. Short Circuit Current $I_{sc} = \dots\dots\dots$
2. Open Circuit Voltage $V_{oc} = \dots\dots\dots$
3. Maximum Peak Point

RESULT:

Studied V-I Characteristics of Solar Cell and determined maximum powerpoint as -----

viva questions:

- 1) What is a solar cell?
- 2) What is the purpose of a solar cell?
- 3) What is the mode of biasing?
- 4) What is the principle of solar cell?
- 5) What is open circuit of a solar cell?

