Sri Indu College of Engineering & Technology

HAND OUT

DEPARTMENT OF ARTIFICIAL INTELLIGENCE AND DATA SCIENCE

ACADEMIC YEAR 2025-26

HANDOUT-INDEX

S.No	Contents
1	Vision,Mission,PEOs,POs,PSOs&COs
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Sri Indu College of Engineering & Technology

ARTIFICIAL INTELLIGENCE AND DATA SCIENCE

Sheriguda (V), R.R.Dist

INSTITUTION VISION

To be a premier Institution in Engineering & Technology and Management with competency, values and social consciousness.

INSTITUTION MISSION

IM_1 Provide high quality academic programs, training activities and research facilities.

IM_2 Promote continuous Industry-Institute interaction for employability, Entrepreneurship, leadership and research aptitude among stakeholders.

IM_3 Contribute to the economical and technological development of the region, state and nation.

PRINCIPAL

Sri Indu College of Engineering & Technology :: Sheriguda (V), R.R.Dist

Department of Artificial Intelligence And Data Science

DEPARTMENT VISION

To be a center of excellence in Electronics and Communication Engineering Education to produce professionals for ever-growing needs of society.

DEPARTMENT MISSION

The Department has following Missions:

DM_1 To promote and facilitate student- centric learning.

DM_2 To involve in activities that enable overall development of stakeholders.

DM_3 To provide holistic environment with state-of-art facilities for students to develop solutions for various social needs.

DM_4 Organize trainings in embedded systems with Industry interaction.

Sri Indu College of Engineering & Technology ::
Sheriguda (V), R.R.Dist

Department of Artificial Intelligence And Data Science

Program Educational Objectives (PEOs)

PEO1: Accomplish technical proficiency for the efficacious ECE Professional.

PEO2: Pursue higher studies with emphasizing design, test and development of the systems to meet the industry and societal needs.

PEO3: Become entrepreneur by practicing ethics, professional integrity and leadership qualities.

Head of the Department (AIDS)

Sri Indu College of Engineering & Technology

Sheriguda (V), R.R.Dist

Department of Artificial Intelligence And Data Science

PROGRAM OUTCOMES (POs) & PROGRAM SPECIFIC OUTCOMES (PSOs)

PO	Description
PO 1	**gineering Knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO 2	**oblem Analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO 3	**Design / development of Solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO 4	**Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO 5	**Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO 6	**The engineer and Society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO 7	**vironment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO 8	**Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice
PO 9	**Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO 10	**Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO 11	**Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO 12	**Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological Change
Program Specific Outcomes	
PSO 1	To nurture and empower the SICET-ECE students strong in practical, technical and research domains in the areas of Signal/Image processing, VLSI and wireless Communication.
PSO 2	To design and develop a prototype system that will incorporate user requirements using modern devices and emerging technology for industry automations.
PSO 3	To make the SICET-ECE students as successful **industry ready engineers** by imparting essential **interpersonal skills and widespread exposure** on multi-disciplinary technologies

Head of the Department (AIDS)

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY
(An Autonomous Institution under UGC, New Delhi)
Recognized under 2(f) and 12(B) of UGC Act 1956
NBA & NAAC Accredited, Approved by AICTE and Permanently affiliated to JNTUH
Sheriguda (V), Ibrahimpatnam, R.R.Dist, Hyderabad - 501 510

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ANNEXURE -III

BR-22

Lr.No.SICET/AUTO/DAE/II B.Tech Academic Calendar/30/2025

B.TECH II-YEAR I-SEM & II-SEM ACADEMIC CALENDAR

(FOR ACADEMIC YEAR : 2025-26)

Academic Calendar for B.Tech – IInd Year Students (2024 - 25 Batch), BR-22 Regulation.

I – Semester

S.No.	EVENT	PERIOD	DURATION
1.	**Commencement of class work.**	**01.08.2025**	
2.	1st Spell of Instructions for covering First Two and a half Units.	01.08.2025 –07.10.2025	9 Weeks
3.	I Mid Term Examinations.	08.10.2025 –10.10.2025	3 Days
4.	Submission of I Mid Term Examination Marks.	16.10.2025	
5.	2nd Spell of Instructions for Remaining Two and a half Units.	13.10.2025 – 13.12.2025	9 Weeks
6.	II Mid Term Examinations.	15.12.2025 – 17.12.2025	3 Days
7.	Preparation Holidays and Practical Examinations	18.12.2025 – 27.12.2025	1 Week
8.	Submission of II Mid Term Examination Marks.	23.12.2025	
9.	I Semester End Examinations.	29.12.2025 – 10.01.2026	2 Weeks
Commencement of Class-Work for II B.Tech - II Semester 19.01.2026			

Note: No of Working/instructional days : 92

II – Semester

S.No.	EVENT	PERIOD	DURATION
1.	**Commencement of class work.**	**19.01.2026 (Monday)**	
2.	1st Spell of Instructions for covering First Two and a half Units.	19.01.2026 – 14.03.2026	8 Weeks
3.	I Mid Term Examinations.	16.03.2026 – 18.03.2026	3 Days
4.	Submission of I Mid Term Examination Marks.	24.03.2026	
5.	2nd Spell of Instructions for Remaining Two and a half Units.	20.03.2026 – 09.05.2026	7 Weeks
6.	Continuation of remaining 2nd Spell of Instructions	25.05.2026 – 10.06.2026	2 Weeks
7.	II Mid Term Examinations.	11.06.2026 –13.06.2026	3 Days
8.	Preparation Holidays and Project Evaluation.	15.06.2026 – 20.06.2026	1 Week
9.	Submission of II Mid Term Examination Marks.	18.06.2026	
10.	II Semester End Examinations	22.06.2026 – 04.07.2026	2 Weeks

Note: No of Working/instructional days : 92

ACE **CE** **DIRECTOR** **PRINCIPAL**

Controller of Examination
Sri Indu College of Engineering & Technology
(An Autonomous Institution Under UGC)
Sheriguda (V), Ibrahimpatnam, R.R. Dist-501510

DIRECTOR
Sri Indu College of Engineering & Technology
(An Autonomous Institution Under UGC)
Sheriguda (V), Ibrahimpatnam, R.R. Dist-501510

PRINCIPAL
Sri Indu College of Engineering & Technology
(An Autonomous Institution Under UGC)
Sheriguda (V), Ibrahimpatnam, R.R. Dist-501510.

Sign:
Dr. M.V.S.S. Giridhar
Prof. of CEA; JNTUH Nominee

Sign:
Dr. T. Venu Gopal
Prof. of CSE; JNTUH Nominee

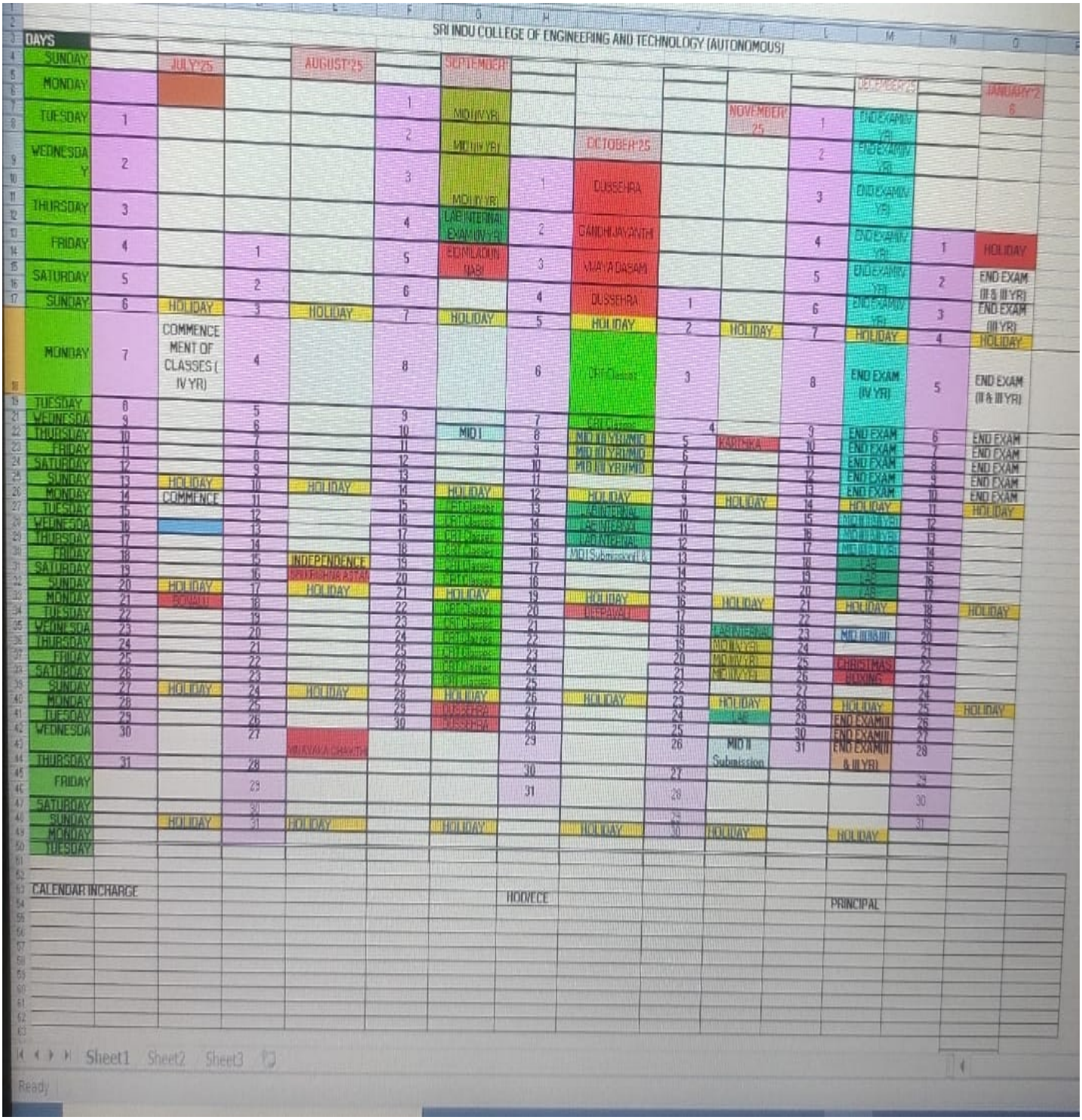
Sign:
Dr. D. Ramesh
Prof. of CSE; JNTUH Nominee

(Copy to DAP&E and Copy to all the Dept. Heads)

SRI INDU COLLEGE OF ENGINEERING AND TECHNOLOGY(AUTONOMOUS)

DEPARTMENT OF ARTIFICIAL INTELLIGENCE AND DATA SCIENCE

DEPARTMENT CALENDAR–2025-2026(SEMESTER-1)



SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

B.Tech. - II Year – I Semester

L	T	P	C
3	0	0	3

(R22ECE2112) DIGITAL ELECTRONICS

Course Objectives: This course aims at through understanding of binary number system, logic gates, combination logic and synchronous and asynchronous logic.

UNIT - I:

BOOLEAN ALGEBRA AND LOGIC GATES: Digital Systems, Binary Numbers, Number base conversions, Octal and Hexadecimal Numbers, complements, Signed binary numbers, Binary codes, Binary Storage and Registers, Binary logic.

Basic Definitions, Axiomatic definition of Boolean Algebra, Basic theorems and properties of Boolean algebra, Boolean functions, canonical and standard forms, other logic operations, Digital logic gates.

UNIT - II:

GATE – LEVEL MINIMIZATION: The map method, Four-variable map, Five-Variable map, product of sums simplification Don't-care conditions, NAND and NOR implementation other Two-level implementations, Exclusive – Or function.

UNIT - III:

COMBINATIONAL LOGIC: Combinational Circuits, Analysis procedure Design procedure, Binary Adder-Subtractor Decimal Adder, Binary multiplier, magnitude comparator, Decoders, Encoders, Multiplexers, HDL for combinational circuits.

UNIT - IV:

SEQUENTIAL LOGIC: Sequential circuits, latches, Flip-Flops Analysis of clocked sequential circuits, state Reduction and Assignment, Design Procedure. Registers, shift Registers, Ripple counters, synchronous counters, other counters.

UNIT - V

MEMORIES AND ASYNCHRONOUS SEQUENTIAL LOGIC: Introduction, Random-Access Memory, Memory Decoding, Error Detection and correction Read-only memory, Programmable logic Array programmable Array logic, Sequential Programmable Devices.

Introduction, Analysis Procedure, Circuits with Latches, Design Procedure, Reduction of state and Flow Tables, Race-Free state Assignment Hazards, Design Example.

TEXT BOOKS:

1. Digital Design – Third Edition, M. Morris Mano, Pearson Education/PHI.
2. Digital Principles and Applications Albert Paul Malvino Donald P. Leach TATA McGraw Hill Edition.
3. Fundamentals of Logic Design, Roth, 5th Edition, Thomson.

REFERENCE BOOKS:

1. Switching and Finite Automata Theory by Zvi. Kohavi, Tata McGraw Hill.
2. Switching and Logic Design, C.V.S. Rao, Pearson Education
3. Digital Principles and Design – Donald D.Givone, Tata McGraw Hill, Edition.
4. Fundamentals of Digital Logic and Microcomputer Design, 5TH Edition, M. Rafiquzzaman JohnWiley

	SRI INDU COLLEGE OF ENGG&TEH **LESSON PLAN** **(Regulation:R22)** **Department of AIDS**	**(Regulation:R22)** **Prepared on** **Rev1:**
	Sub.Code&Title	**R22ECE2112&DIGITAL ELECTRONICS**
	AcademicYear:2025-26	**Year/Sem.** **II/II**
	FacultyName&Designation	**D.JYOTHI**

Unit/ Item No.	Topic (s)	Book Reference	Page (s) From	Page (s) To	Teaching Methodology	Proposed No. of Periods	Actual Date of Handled	CO/RBT
	UNIT – I							
I	**BOOLEAN ALGEBRA AND LOGIC GATES**					**17**		
1.1	Introduction to digital systems	T1	17	20	Black board	01		CO-1
1.2	Binary Number Systems	T1	20	22	Blackboard	01		CO-1
1.3	Number base conversion	T1	22	27	Blackboard	01		CO-1
1.4	Complements of Numbers	T1	27	32	Blackboard	01		CO-1
1.5	Signed binary Numbers	T1	33	37	Blackboard	01		CO-1
1.6	Binary Codes	T1	38	47	Blackboard	01		CO-1
1.7	Binary Storage &Registers	T1	47	49	Blackboard	01		CO-1
1.8	Binary Logic	T1	50	51	Blackboard	01		CO-1
1.9	Axiomatic definition of Boolean Algebra	T1	59	62	Blackboard	01		CO-1
1.10	Basic theorems&Properties	T1	63	66	Black board	01		CO-1
1.11	Boolean Functions	T1	66	72	Black board	01		CO-1
1.12	Canonical & Standard form	T1	72	82	Black board	01		CO-1
1.13	Logic Gates	T1	83	84	Black board	01		CO-1
1.14	AND	T1	84	86	Black board	01		CO-1
1.15	OR,NOT,Ex-OR,EX-NOR,NAND,NOR	T1	86	89	Black board	01		CO-1
1.16	Problems	T1	131	133	Black board	01		CO-1
1.17	Problems	T1	135	137	Black board	01		CO-1
	Review	**Signature of the HOD/Coordinator**						

	SRI INDU COLLEGE OF ENGG&TEH **LESSON PLAN** **(Regulation:R22)** **Department of AIDS**	**(Regulation:R22)** **Prepared on** **Rev1**

Sub.Code&Title	**R22ECE2112&DIGITAL ELECTRONICS**	
AcademicYear:2025-26	**Year/Sem.**	**II/II**
FacultyName&Designation	**D.JYOTHI**	

Unit/ Item No.	Topic (s)	Book Reference	Page (s) From	Page (s) To	Teaching Methodology	Proposed No. of Periods	Actual Date of Handled	CO/RBT
	UNIT – II							
II	**GATE – LEVEL MINIMIZATION:**					**15**		
2.1	Introduction to Gate Level Minimization	T1	98	99	Black board	01		CO-2
2.2	Karnaugh Map Method - Up to 3 Variables	T1	99	106	Black board	02		CO-2
2.3	Karnaugh Map Method - 4,5 Variables	T1	107	111	Black board	02		CO-2
2.4	Product of Sum	T1	111	115	Black board	01		CO-2
2.5	Don't care Condition	T1	115	117	Black board	01		CO-2
2.6	NAND& NOR Implemetation	T1	118	119	Black board	02		CO-2
2.7	Two-Level Implementation	T1	119	124	Black board	02		CO-2
2.8	Problems	T1	124	130	Black board	02		CO-2
2.10	Exclusive -OR Function	T1	131	136	Black board	01		CO-2
2.11	HDLs	T1	137	161	Black board	01		CO-2
	Review	**Signature of the HOD/Coordinator**						

	SRI INDU COLLEGE OF ENGG&TEH **LESSON PLAN** **(Regulation:R22)** **Department of AIDS**	**(Regulation:R22)** **Prepared on** **Rev1**

	Sub.Code&Title	**R22ECE2112&DIGITAL ELECTRONICS**	
	AcademicYear:2025-26	**Year/Sem.**	**II/II**
	FacultyName&Designation	**D.JYOTHI**	

Unit/ Item No.	Topic (s)	Book Reference	Page (s) From	Page (s) To	Teaching Methodology	Proposed No. of Periods	Actual Date of Handled	CO/RBT
	UNIT – III							
III	**COMBINATIONAL LOGIC**					**17**		
3.1	**Introduction to Combinational Logic Circuits**	T1	163	165	Black board	01		CO-3
3.2	Analysis of Combinational circuits	T1	165	168	Black board	02		CO-3
3.3	Design of Combinational circuits	T1	169	172	Black board	02		CO-3
3.4	Binary Adder	T1	172	184	Black board	01		CO-3
3.5	Decimal Adder	T1	184	186	Black board	01		CO-3
3.6	Multiplier	T1	186	188	Black board	02		CO-3
3.7	Magnitude Comparator	T1	188	190	Black board	01		CO-3
3.8	Decoders	T1	191	195	Black board	01		CO-3
3.9	Encoders	T1	195	198	Black board	01		CO-3
3.11	Multiplexers	T1	198	205	Black board	02		CO-3
3.12	HDL Models of Combinational Circuits	T1	205	252	Black board	02		CO-3
	Review	**Signature of the HOD/Coordinator**						

	Sub.Code&Title	**R22ECE2112&DIGITAL ELECTRONICS**	
	AcademicYear:2025-26	**Year/Sem**	**II/II**
	FacultyName&Designation	**D.JYOTHI**	

Unit/ Item No.	Topic (s)	Book Reference	Page (s) From	Page (s) To	Teaching Methodology	Proposed No. of Periods	Actual Date of Handled	CO/RBT
	UNIT – IV							
IV	**SEQUENTIAL LOGIC:**					**13**		
4.1	Introduction	T1	262	264	Black board	01		CO-3
4.2	Storage elements:Latches	TI	264	269	Black board	01		CO-3
4.3	Flip-Flops	T1	269	277	Black board	01		CO-3
4.4	Analysis of clocked squential circuits	T1	277	288	Black board	01		CO-3
4.5	State Reduction &Assignment	T1	316	321	Black board	01		CO-3
4.6	Design Procedure	T1	321	330	Black board	01		CO-3
4.7	Registers	T1	342	346	Black board	01		CO-3
4.8	Shift Registers	T1	347	353	Black board	02		CO-3
4.9	Ripple Counters	T1	354	359	Black board	02		CO-3
4.10	Synchronous Counters	T1	359	367	Black board	01		CO-3
4.11	Other Counters	T1	367	372	Black board	01		CO-3
	Review	**Signature of the HOD/Coordinator**						

	SRI INDU COLLEGE OF ENGG&TEH **LESSON PLAN** **(Regulation:R22)** **Department of AIDS**		**(Regulation:R22)** **Prepared on** **Rev1**
	Sub.Code&Title	**R22ECE2112&DIGITAL ELECTRONICS**	
	AcademicYear:2025-26	**Year/Sem./Section**	**II/II**

	FacultyName&Designation	D.JYOTHI

Unit/ Item No.	Topic (s)	Book Reference	Page (s) From	Page (s) To	Teaching Methodology	Proposed No. of Periods	Actual Date of Handled	CO/RBT
	UNIT –V							
V	**MEMORIES AND ASYNCHRONOUS SEQUENTIAL LOGIC:**					17		
5.1	Introduction	T1	394	395	Black board	01		CO-4
5.2	Random Acess Memory	T1	395	402	Black board	01		CO-4
5.3	Memory Decoding	T1	402	407	Black board	01		CO-4
5.4	Error detection&Correction	T1	407	410	Black board	01		CO-4
5.5	Read only Memory	T1	410	416	Black board	01		CO-4
5.6	Programmable Logic Array	T1	416	420	Black board	01		CO-4
5.7	Programmable Array Logic	T1	420	424	Black board	01		CO-4
5.8	Sequential Programmable Devices	T1	424	440	Black board	01		CO-4
5.9	Asynchronous Sequential Logic	T1	571	573	Black board	01		CO-4
5.11	Analysis Procedure	T1	589	596	Black board	01		CO-4
5.12	Circuits with Latches	T1	581	589	Black board	01		CO-4
5.13	Design Procedure	T1	589	596	Black board	01		CO-4
5.14	Reduction of State Assignment	T1	596	604	Black board	01		CO-4
5.15	Race -free State Assignment	T1	604	609	Black board	01		CO-4
5.16	Hazards	T1	609	614	Black board	01		CO-4
5.17	Design Examples	T1	614	626	Black board	01		CO-4
	Review	**Signature of the HOD/Coordinator**						

LIST OF TEXT BOOKS AND REFERENCES

TEXTBOOKS:

1. Digital Design–Third Edition, M.MorrisMano, PearsonEducation/PHI.
2. DigitalPrinciplesandApplicationsAlbertPaulMalvinoDonaldP.LeachTATAMcGrawHillEdition.
3. FundamentalsofLogicDesign,Roth,5th Edition,Thomson.

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4. Fundamentals of Digital Logic and Microcomputer Design,5TH Edition,M.RafiquzzamanJohnWiley.

QUESTIONBANK

	SRI INDU COLLEGE OF ENGG & TECHOLOGY **QUESTIONBANK** **(Regulation:R22)** **Department of AIDS**	**Prepared onRev1:** **Page:1of5**

Sub.Code&Title	**(R22ECE2112)DIGITAL ELECTRONICS**	
AcademicYear:2025-26	**Year/Sem.**	**IIB.TECHI-II SEM**
FacultyName&Designation	**D.JYOTHI**	

UNIT-I:BOOLEAN ALGEBRA AND LOGIC GATES:

	Multiple Choice Questions	BT Level	Course Outcome
1M-1	In Boolean algebra, the OR operation is performed by which properties ? ( ) a)associative properties b)commutative properties c)distributive properties d)all of the mentioned	I	CO1
1M-2	Change SOP to POS form F(A,B,C,D)=∑m(0,1,2,4,5,6,8,9,11,12,15) ( ) a)π(3,7,10,13,14) b)π(3,7,12,13,14) c)π(3,2,10,13,4) d)π(3,7,10,11,14)	VI	CO1
1M-3	According to boolean law rule : A + 1 = ? ( ) a) 1 b) A c) 0 d) A’	V	CO1
1M-4	Determine A (A + B) = ? ( ) a) AB b) 1 c) 1+AB d) A	V	CO1
1M-5	De Morgan’s theorem states that _____ ( ) a) (AB)’=A’+B’ b) (A+B)’ =A’*B c) A’+B’=A’B’ d) (AB)’ = A’+B	III	CO1

1M-6	Choose the Complement of the expression A+B + ABC' is _ ( ) a) (A' + B)(C' + D) b) (A + B')(C' + D) c) A' B' d) (A + B')(C + D')	III	CO1
1M-7	Simplify Y = AB' + (A' + B)C. ( ) a) AB' + C b) AB + AC c) A'B + AC' d) AB + A	IV	CO1
1M-8	Determine the equivalent hexadecimal number for given octal number $(615.25)_8$ is ( ) a) $(1A9.2A)_{16}$ b) $(1B0.10)_{16}$ c) $(1A8.A3)_{16}$ d) $(18D.54)_{16}$	V	CO1
1M-9	What is the addition of the binary numbers 11011011010 and 010100101? ( ) a) 0111001000 b) 1100110110 c) 11101111111 d) 10011010011	I	CO1
1M-10	Simplify the binary subtraction: 101111 – 010101 = ? a) 100100 b) 010101 c) 011010 d) 011001	IV	CO1
1M-11	Determine 100101 × 0110 = ? ( ) a) 011011110 b) 0100110011 c) 101111110 d) 0110100101	V	CO1
1M-12	The logical sum of two or more logical product terms is called? ( ) a) SOP b) POS c) OR operation d) NAND operation	IV	CO1
1M-13	A code converter is a logic circuit that ( ) a) Inverts the given input b) Converts into decimal number c) Converts data of one type into another type d) Converts to octal	VI	CO1
1M-14	The primary use of Gray code is _____. ( ) a) Coded representation of a shift's mechanical position b) Turning on/off software switches c) To represent the correct ASCII code to indicate the angular position of	I	CO1

	a shaft on rotating machinery d) To convert the angular position of a shaft on rotating machinery into hexadecimal code		
1M-15	Code is a symbolic representation of _____ ( ) a) Discrete information b) Continuous information c)) Decimal information into binary d) Binary information in to decimal	IV	CO1
	#Filling The Blank Questions		
1F-1	The expression Y=AB+BC+AC shows the_____ operation	I	CO1
1F-2	Evaluate the 2's complement of 11001011 is _____	V	CO1
1F-3	Determine the 1's complement of 1011101 is _____	V	CO1
1F-4	Solve the subtracting $(01010)_2$ from$(11110)_2$ using 1's complement, we get _____	III	CO1
1F-5	Determine addition of 28 and 18 then we get _____	V	CO1
1F-6	How many truth table entries are necessary for a four-input circuit_____ .	I	CO1

1F-7	What is the canonical sum of product form of the function Y(A,B)=A+B is _____.	I	CO1
1F-8	Summarize a variable on its own or in its complemented form is known as a _____.	II	CO1
1F-9	Tell canonical form is a unique way of representing _____ .	I	CO1
1F-10	Assume there are _____ minterms for 3 variables (a,b,c)	IV	CO1
1F-11	Find the addition 83 & 34 in BCD _____ .	I	CO1
1F-12	Name the Reflected binary code is also known as _____. .	I	CO1
1F-13	Tell in r's complement if carry is not generated then the result is _____ .	I	CO1
1F-14	What is the BCD number for decimal no 29 is _____.	I	CO1
1F-15	Suppose converting any radix to decimal _____.	VI	CO1

#Match The Following Questions

1M-1	Match the following a) 10101010 (i) 128 b) 11110000 (ii) 240 c) 10001000 (iii) 170 d) 10000000 (iv) 136	V	CO1
1M-2	Match the following a) A+A = (i) 0 b) A+1 = (ii) B c) (A+A)B= (iii) A d) A.0 = (iv) 1	II	CO1
1M-3	Match the following a) 1110010011 (i) $(010101101.011100)_2$ b) 1000 1100 0101 (ii) $(125.62)_8$ c) $(001010101.110010)_2$ (iii) Ex-3 of 592 d) $(255.34)_8$ (iv) 1011100010 to Gray	I	CO1
1M-4	Match the following a) Counting (i) ROM b) Decoding (ii) Multiplexer c) Data selecting (iii) Demultiplexer d) Code conversion (iv) Register	IV	CO1

1M-5	Match the following a) Excess-3 code b) BCD code c) ASCII code d) Gray code	(i) weighted code (ii)only 1-bit change during transistion (iii) self complementing code (iv) 7-bit code	I	CO1

#5MARKSQUESTIONS			
1.	What are the rules for Excess-3 addition? Add two decimal numbers 123 and 658 in Excess-3 code?	I	CO1
2.	Simplify the logic function i).F (A, B, C, D) = AB+AC+C+AD+ABC+ABC ii) .F (A, B, C, D) = AC+ABC+BC	IV	CO1
3.	Minimize the following Boolean expressions. i. B'C'D+(B+C+D)'+B'C'D'E ii. AB+(AC)'+AB'C(AB+C) iii. A'B'C'+A'BC'+AB'C'+ABC' iv. A+B+A'B'C	VI	CO1
4.	Write the minterms and maxterms for the following functions i) $F=\sum m(1,4,6,7,9)$ ii) $F=\pi m(3,5,7,11,14)$ iii) State and prove Demorgan's theorems	I	CO1
5.	A) Justify the BINARY TO GRAY and GRAY TO BINARY WITH (10110011) ? B) Justify with your answer Why are NAND and NOR gates known as universal gates?	V	CO1
6.	Construct the logic gate diagram for the expression [(A+B).C]'D by using NAND gate ?	III	CO1
7.	What are the logic gates with truth tables and Properties of Ex-or gate?	I	CO1
8.	Convert i .$(110101.0101)_2$__( )$_8$ ii .$(125.62)_8$__( )$_2$ iii.$(11001101.110110)_2$__( )$_{16}$ iv .$(8A9.B4)_{16}$__( )$_2$ v .$(615.25)_8$__( )$_{16}$ vi .$(BC66.AF)_{16}$__( )$_8$	V	CO1
9.	Translate or Convert the following i. $(AF.B9)_{16} = (\ )_{10}$ ii. $(126.75)_8 = (\ )_{10}$ iii. $(11011.1101)_2 = (\ )_{10}$ iv. $(153)_{10} = (\ )_2$	II	CO1
10.	Explain different types of number systems with example?	VI	CO1
11.	A) Make use of 1's and 2's complement method subtract 42 from 36 ? B) Construct a truth table for a given expression AB+CD?	III	CO1
12.	Explain Boolean algebra laws and rules? State Duality Theorem?	II	CO1
13.	A) Change the given SOP into POS form $f(A,B,C,D)=\sum m(0,2,4,6,8,10,12,14)$ B) Construct the logic diagram of Y = AC+ABC+A'BC+AB+D	VI	CO1
14.	Draw the logic diagram of NOR- NOR implementation of Y = AC+BC+AB+D?	I	CO1
15.	Implement the function f=ABC+DE+F by using NAND-NAND implementation?	II	CO1

#UNIT-II:GATE-LEVELMINIMIZATION:			
#MultipleChoiceQuestions		**BT Level**	**Course Outcome**
2M-1	Choose the minterm in a karnaugh map are marked with a? a) Y ( ) b) X c) 0 d) 1	I	CO2
2M-2	Identify a karnaugh map (k-map) is a theoretical form of representing ? ( ) a) Circuit diagram b) Block diagram c) Logic diagram d) Venn diagram	III	CO2
2M-3	Map method provides a straight forward procedure for ( ) a) Minimizing Boolean function b) Minimizing sop c) Minimizing pos d) Minimizing boxes	I	CO2
2M-4	Which of the following is not considered for forming groups in K-map? ( ) a) Rolling b) Diagonal c) Vertical d) Horizontal	I	CO2
2M-5	Choose the one input NOR and NAND gate behaves like a ? ( ) a) Converter b) Inverter c) Reflector d) Differentiator	VI	CO2

2M-6	Name the NOR function is the dual of ? ( ) a) AND function b) OR function c) XOR function d) NAND function	I	CO2
2M-7	What value is to be considered for a " don't care condition"? ( ) a) 0 b) 1 c) Either 0 or 1 d) Any number except 0 and 1	I	CO2
2M-8	Utilize the minimum number of 2 input NAND gates required to implement the function F=A+AB'+AB'C is equal to ? ( ) a)Zero b) 1 c) 4 d) 7	III	CO2
2M-9	Select the one option Karnaugh map is used to ( ) a) Minimize the number of flip-flop in digital circuit b) Minimize the number of gates only a digital circuit c) Minimize the number of gates and fan-in of a digital circuit d) Design gates	III	CO2
2M-10	Which of the following is equivalent to AND –OR realization? ( ) a) NAND-NOR realization b) NOR-NOR realization c) NOR-NAND realization d) NAND-NAND realization	I	CO2
2M-11	A three –input NAND gate is to be used as an inverter which one of the following measures will achieve better result? ( ) a) The two input not used are kept open b) The two input not are connected to ground (0 level) c) The two inputs not used are connected to logic (1 level) d) None of the above	V	CO2

2M-12	Which of the following is equivalent to NAND-NAND realization? ( ) a) AND-OR realization b) NOR-NOR realization c) NOR-NAND realization d) NAND-NAND realization	I	CO2
2M-13	Which of the following is equivalent to NAND-NOR realization ( ) a) Inverted –input OR gate, inverted-input AND gate b) AND-OR realization c) NOR-NOR realization d) NAND-NAND realization	I	CO2
2M-14	Identify how many cells have 5 variable K-map? ( ) a) 16 Cells b) 8 Cells c) 32 Cells d) 4 Cells	III	CO2
2M-15	Choose how many cells have 4 variable K-map? ( ) a) 16 Cells b) 8 Cells c) 32 Cells d) 4 Cells	VI	CO2

	#Filling The Blank Questions		
2F-1	Name the Karnaugh map is used to _____.	I	CO2
2F-2	Tell that minterms in a Karnaugh map are marked with a _____.	I	CO2
2F-3	What value is to be considered for a don't care condition _____.	I	CO2
2F-4	Which of the following is equivalent to AND-OR realization _____.	I	CO2
2F-5	Original NOR function is the dual of _____.	VI	CO2
2F-6	Determine how many cells have 5 variable K-map _____.	V	CO2
2F-7	Assume how many cells have 4 variable K-map _____.	IV	CO2
2F-8	Classify how many types of Degenerative form _____.	IV	CO2
2F-9	Which of the following is equivalent to NAND-NOR realization _____.	I	CO2
2F-10	What is the output of Ex-or gate _____ .	I	CO2
2F-11	Apply product of sum form is a method (or form) of simplifying _____.	III	CO2
2F-12	Analyze the function can be written in product of sum form as _____ .	IV	CO2
2F-13	Construct exclusive or equivalent gate is equal _____ .	VI	CO2
2F-14	Tell the map method is also known as the _____ map.	I	CO2
2F-15	What is meant by pair _____ .	I	CO2
	#Match The Following Questions		
2M-1	Match the following a) Exclusive or gate (i)(A+B)' b) NAND gate (ii)A'B'+AB c) NOR gate (iii)AB'+A'B d) Exclusive or gate (iv)(AB)'	I	CO2
2M-2	Match the following a) 2-variable map (i) 32 Cells b) 3-variable map (ii) 16 Cells c) 4-variable map (iii) 8 Cells d) 5-variable map (iv) 4 Cells	II	CO2
2M-3	Match the following a) AND-OR realization (i) AND-OR b) NAND-NOR realization (ii) NAND-NAND c) NOR-NAND realization (iii) OR-AND d) NAND-NAND realization (iv) Inverted I/POR gate, inverted I/PAND	III	CO2

2M-4	Match the following a) Exclusive -OR (i) (AB)' b) NAND (ii) (A+B)' c) NOR (iii) A'B+AB' d) Don't care (iv) X	III	CO2
2M-5	Match the following a) NAND (i) 32 Cells b) 5-variable (ii) 16 Cells c) 4-variable (iii) A'B+AB' d) EX-OR (iv) A'B'	III	CO2

#5MARKSQUESTIONS			
1.	A) What is don't care condition and explain with one example? B) What is Prime Implicates and Essential Prime Implicates?	I	CO2
2.	A)Determine the Boolean expression for given function by using K-map & Realize by using NAND gates f (A, B, C) =∑ (0, 1,2, 4,5) ? B)Reduce the following function using K-map f(A,B,C,D) = ΠM or Ø (0,2,3,8,9,12,13,15) ?	V	CO2
3.	A) What is meant by pair and quads? B) Reduce the expression by using K-map Y = ∑m (1, 5,7,9, 11,13,15) ?	I	CO2
4.	Implement Boolean expression for EX-OR gate using NAND gates?	I	CO2
5.	Construct a logic diagram using only two input NAND gate to implement the following expression (AB + A'B')(CD' + C'D)	VI	CO2
6.	What is Karnaugh map? 4-variable k- map?	I	CO2
7.	Solve the SOP expression by using 5 variable K-map F(A,B,C,D,E) =∑m(0,2,5,7,8,10,13,15,16,18,20,21,23,24,26,28,29,31) ?	III	CO2
8.	Discuss about the product of sum ?Reduce the expression by using K-map method Y=(A'+B'+C+D)(A'+B'+C'+D)(A'+B'+C'+D')(A+B'+C'+D)(A+B+C+D)(A'+B'+C+D')(A+B'+C'+D')(A'+B+C+D)	VI	CO2
9.	Find the reduced sop form for the given expression F(A,B,C,D) = ∑m(0,7,8,9,10,12)+∑d(2,5,13) ?	I	CO2
10.	Discuss about the OR-OR Implementation? (Two-Level Implementation)?	VI	CO2
11.	Summarize about the NAND-NOR Implementation?	II	CO2
12.	A) Implement the function f=ABC+DE+F by using NAND-NAND implementation? B) Draw the logic diagram of NOR- NOR implementation of Y = AC+BC+AB+D?	I	CO2
13.	Simplify the function using tabular method (or) QUINE- MCCLUSKEY method f(A,B,C,D) = ∑(0,2,3,6,7,8,10,12,13)?	IV	CO2
14.	Reduce the following function using K-map f(A,B,C,D) = ΠM or Ø (0,2,3,8,9,12,13,15)?	II	CO2
15.	Simplify the function using K-map method and realize by NAND gates? f(A,B,C,D) = ∑(0,1,2,3,12,13,14,15)?	IV	CO2

#UNIT-III:COMBINATIONALLOGIC:		
#Multiple Choice Questions	**BT Level**	**Course Outcome**

3M-1	Code conversion circuits mostly uses? ( ) a. AND-OR gates b. AND gates c. OR gates d. XOR gates	I	CO3
3M-2	Full Adder combinational circuits has 3 inputs and ? ( ) a. 2 outputs b. 1 output c. 3 outputs d. None	I	CO3
3M-3	Designing combinational circuit involves ? ( ) a. 4 steps b. 5 steps c. 6 steps d. 8 steps	VI	CO3
3M-4	Half adder circuits two binary? ( ) a. Inputs b. Outputs c. Digits d. Both a and b	I	CO3
3M-5	Circuits that employ memory elements in addition to gates is called? ( ) a. Combinational circuit b. Sequential circuit c. Combinational sequence d. Series	II	CO3
3M-6	When both inputs are 1,the output of XOR is ? ( ) a. 1 b. 0 c. X d. 10	II	CO3

3M-7	Half subtractor is used to perform subtraction of ? ( ) a. 2 bits b. 3 bits c. 4 bits d. 5 bits	I	CO3
3M-8	Dual of the NAND function is ( ) a. AND function b. OR function c. NOR function d. NAND function	I	CO3
3M-9	Choose 2 to 4 line decoder will have ( ) a. 2 enables b. 3 enables c. 4 enables d. 8 enables	I	CO3
3M-10	All the comparisons made by comparator is done using ( ) a. 1 circuit b. 2 circuit c. 3 circuit d. 4 circuits	V	CO3
3M-11	Identify if two numbers are not equal then the binary variable will ( ) a. 0 b. 1 c. a d. b	III	CO3
3M-12	Which is not the outcome of magnitude comparator is ( ) a. a>b b. a-b c. a<b d. a=b	I	CO3
3M-13	Which of the following expression is true if the output is equal to zero? ( ) a. A=B b. A>B c. A	I	CO3

	d. A==B		
3M-14	In the design procedure, the first step is to ( ) a. Make map b. Make table c. Make graph d. Make chart	VI	CO3
3M-15	IC decoders are made with ( ) a. AND gate b. XOR gate c. OR gate d. NAND gate	I	CO3
	#Filling The Blank Questions		
3F-1	An eight –line multiplexer must have how many inputs _____.	I	CO3
3F-2	Name the device that generates a coded output from a single active numeric input line is _____.	I	CO3
3F-3	In HDL , the operation of the De-mux is exactly described using a _____.	I	CO3
3F-4	How many outputs are on a BCD decoder _____.	I	CO3
3F-5	What is the function of an enable input on a multiplexer chip _____.	I	CO3
3F-6	Suppose how many inputs will a decimal-to-BCD encoder have _____.	VI	CO3
3F-7	The largest truth table that can be implemented directly with an 8-line-to-1-line MUX has _____.	I	CO3
3F-8	Construct a 2 bit binary multiplier can be implemented using _____.	III	CO3
3F-9	The minimum number of 2 to 1 multiplexer required to generate a 2-input AND gate and a 2-input EX-OR gate _____.	I	CO3
3F-10	What are the minimum number of 2 to 1 multiplexer required to generate a 2-input AND gate and a 2 input EX-OR gate _____.	II	CO3
3F-11	Full adder circuit can be implemented by _____	I	CO3
3F-12	In a 4- bit full adder ,how many half adders and OR gates required _____.	VI	CO3
3F-13	Realization or build a full adder using HA and _____gate.	III	CO3
3F-14	The multiplexer is also known as_____.	I	CO3
3F-15	A _____ is a combinational circuit that compares two numbers.	IV	CO3

	#Match The Following Questions		
3M-1	Match the following a) Multiplexer (i) 2^n:n b) Encoder (ii) n:2^n c) Decoder (iii)2^nx1 d) Demultiplexer (iv) 1x2^n	II	CO3

3M-2	Match the following a) Full adder (i) Combinational b) Shift register (ii) Sequential circuit c) Flip-flop (iii) 0 or 1 d) MUX (iv) 2X1	I	CO3
3M-3	Match the following a) No.of 3 to 8 decoders to perform 5 to 32 decoder (i) 5 b) No.of NAND gates to design Half Adder (ii) 15 c) No.of 2:1 mux required to construct 16:1 mux (iii) 3 d) No.of states does a buffer has (iv) 4	I	CO3
3M-4	Match the following a) Full adder (i) VLSI b) Magnitude Comparator (ii) SSI c) Programmable logic array (iii) LSI d) RAM (iv) MSI	I	CO3
3M-5	Match the following a) BCD to 7 segment decoder (i) Sequential circuit b) Decoder (ii) Combinational circuit c) 4 bit shift register (iii) Displayed decoder d) 4-to-1 MUX (iv) Code convertor	I	CO3

#5MARKSQUESTIONS			
1.	Design 32×1 Multiplexer using 8×1 Multiplexers and 2 to 4 decoder?	VI	CO3
2.	Build the full adder using two half adders ?	III	CO3
3.	what is multiplexer? Design 8 to 1 mux using two 4 to 1 mux ?	VI	CO3
4.	what is comparator? Design &implement a 2-bit comparator using logic gates?	VI	CO3
5.	A) Define combinational circuit? B) Implement of Full Subtractor with 2 half subtractor ?	I	CO3
8.	A) List the applications of multiplexer and demultiplexer ? B) Difference between serial adder & parallel adder?	IV	CO3
9.	Explain 4 bit parallel adder and 4 bit parallel subtractor ?	II	CO3
10.	Draw the circuit& truth table of Half Sub tractor?	I	CO3
11.	Construct the following functions using Multiplexer F1 = m (2, 3, 6, 8, 12) F2 = m (1, 3, 5, 6, 7, 8, 10)	III	CO3

12.	A) Design Octal to Binary or 8:3 Encoder using OR gates? B) Design binary multiplier?	VI	CO3
13.	Explain about the 3:8 Decoders?	II	CO3
14.	Explain about 8:1 Multiplexer and 1:8 Demultiplexer using logic diagram ?	II	CO3
15.	Construct a Full-Subtractor circuit and write a HDL program module for the same?	III	CO3
14	Design BCD or Decimal adder using two 4 bit adder?	VI	CO3
15	Explain about Binary Multiplier?	II	CO3

#UNIT-IV: SEQUENTIALLOGIC:			
#Multiple Choice Questions		**BT Level**	**Course Outcome**
4M-1	In Synchronous circuits , the present state is determined by ( ) *a)* Unclocked flip-flops b) Clocked flip-flops c) Flip-flops d) Latches	V	CO4
4M-2	Unclocked flip-flops are known as ( ) a) Latches b) Registers c) Transition tables d) Clocked flip-flop	I	CO4
4M-3	Transition table consists of ( ) a. Squares b. Rectangles c. Circles	I	CO4

	d. Oval		
4M-4	The change in state occurs during ( ) a. Pulse Transition b. Outputs c. Clock pulses d. Inputs	III	CO4
4M-5	Shift registers are used for ( ) a) Shifting b) Rotating c) adding d) both a and b	I	CO4
4M-6	Enable input of the shift register is known as ( ) a. Load b. Store c. Reset d. Strobe	V	CO4
4M-7	The shift register has an integrated circuit with the number ( ) a. 74195 b. 74123 c. 74124 d. 74154	II	CO4
4M-8	When J and complement of K are 1, flip-flop QA after the shift is equal to ( ) a. 1 b. 0 c. Reset d. Defined	V	CO4
4M-9	State box has a shape of ( ) a. Square b. Rectangle c. Rhombus d. Pentagon	I	CO4
4M-10	Which one of the following is not the element of the ASM chart? ( ) a. State box b. Decision box c. Data box d. Conditional box	I	CO4
4M-11	Sequential operations in digital system are described by ( ) a) Map b) ASM chart c) Flow chart d) Graph	I	CO4
4M-12	Which of these flip-flops cannot be used to construct a serial shift register? ( ) a) D-flip-flop b) SR flip-flop c) T flip-flop d) JK flip-flop	I	CO4
4M-13	What kind of operation occurs in a J-K flip-flop when both inputs J and K are Equal to 1? ( ) a) Preset operation b) Reset operation	I	CO4

	c) Clear operation d) Toggle operation		
4M-14	A Johnson counter, constructed with N flip-flops, has how many unique states? ( ) a) N b) 2^N c) 2^{N+1} d) N^2	III	CO4
4M-15	A type of shift register in which the Q or Q output of one stage is not connected to the input of the next stage is ( ) a) Parallel in/Serial out b) Serial in/Parallel out c) Serial in/Serial out d) Parallel in/Parallel out	I	CO4

#FillingTheBlankQuestions			
4F-1	A Johnson counter ,constructed with N flip-flops,has how many unique states_____.	I	CO4
4F-2	A 4-bit ring counter is loaded with a single 1.The frequency of any given output is _____.	II	CO4
4F-3	Shifting a binary number to the left by one position is equivalent to _____.	III	CO4
4F-4	A gated D latch does not have _____.	IV	CO4
4F-5	The maximum possible number of states in clocked sequential circuit having 5 flip-flops is _____.	VI	CO4
4F-6	An R-S latch is _____.	II	CO4
4F-7	Synchronous counters are _____ than the ripple counter	II	CO4
4F-8	A switch –trail ring counter is made by using a single D flip-flop The resulting circuit is a _____	II	CO4
4F-9	The present output Qn of an edge triggered JK flip-flop is logic 0. If J=1 then Qn+1_____.	V	CO4
4F-10	Which of the following equations satisfies the JK flip-flop truth table _____.	I	CO4
4F-11	State transition table and state transition diagram form part of the design steps Is the case of _____.	I	CO4
4F-12	The characteristic equation of an SR flip-flop is given by _____.	IV	CO4
4F-13	The race around condition exists in JK flip-flop if _____.	III	CO4
4F-14	Which of the following flip-flop cannot be converted to D flip-flop _____.	I	CO4
4F-15	In JK if J=1,K=1 _____ condition.	I	CO4

#Match The Following Questions			
4M-1	Match the following a) Ripple up counter (i) Division b) Synchronous Down counter (ii) Multiplication c) Shift left register (iii) To create Delay d) Shift right register (iv) Transient states	III	CO4
4M-2	Match the following a) SISO (i) Serial in parallel out b) SIPO (ii) Parallel in Parallel out c) PIPO (iii) Parallel in serial out d) PISO (iv) Serial in serial out	II	CO4
4M-3	Match the following a) T-FF (i) Delay b) D-FF (ii)Toggle c) JK FF (iii) Set-Reset d) SR FF (iv) Jack Kilby	VI	CO4
4M-4	Match the following a) Latch (i) Level triggering b) Flip-Flop (ii) Edge triggering c) Register (iii)Memory element d) Counter (iv) Store 1 bit information	IV	CO4
4M-5	Match the following a) Up counter (i) The last Flip-flop fed to the input of the first b) Down counter (ii) Cascaded arrangement c) Ripple counter (iii) 9 to 0 d) Ring counter (iv) 0 to 9	V	CO4

#5MARKSQUESTIONS

1.	A) Distinguish between Combinational circuits and Sequential circuits? B) Draw the D latch?	IV	CO4
2.	Write the Characteristic table and Excitation table for JK flip- flop & T flip-flop?	I	CO4
3.	Sketch& Explain the D flip-flop using NAND gates?	II	CO4
4.	What is the drawback of JK flip-flop, design a flip-flop which overcomes this drawback and explain with neat diagram?	VI	CO4
5.	Distinguish between latch and flip- flop? Draw the SR latch?	IV	CO4
6.	Conversion of SR flip- flop to JK flip- flop?	II	CO4
7.	Differentiate between ring counter & ripple counter?	IV	CO4
8.	What is a shift register? &What are the applications of shift register?	I	CO4
9.	Discuss about state diagram, state table, state reduction& state assignment?	VI	CO4
10.	What is sequential machine? Distinguish between synchronous& Asynchronous sequential circuit?	IV	CO4
11.	Construct the state table & state diagram for sequential circuit with one example	III	CO4
12.	Distinguish between Moore Model And Melay Model?	IV	CO4
13.	Design Synchronous Sequential Circuit by using any flip-flop?	VI	CO4
14.	Classification of shift Registers & applications?	II	CO4
15.	Explain about Synchronous counters and draw the timing diagram for 3 bit up/down counter?	II	CO4

#UNIT-V:MEMORIESANDASYCHRONOUSSEQUENTIALLOGIC:			
#Multiple Choice Questions		**BT Level**	**Course Outcome**
5M-1	Asynchronous circuits are useful in application where the input signals may? ( ) a. Change at any time b. Never change c. both a and b d. Continuously change	I	CO6
5M-2	The table that is not a part of the asynchronous analysis procedure is ? ( ) a. Transition table b. State table c. Flow table d. Excitation table	I	CO6
5M-3	That is the significant capacity of memory elements utilized in the sequential circuits? ( ) a. Storage of binary information b. Specify the state of sequential	II	CO6

	c. both a and b d. State machine		
5M-4	In the asynchronous circuit, the change occur with the change of ( ) a) Input b) Output c) Clock pulse d) Time	IV	CO6
5M-5	The complexity of the asynchronous circuit is involved in timing problems of ( ) a. Inputs b. Outputs c. Clock pulse d. Feedback path	III	CO6
5M-6	A condition occurs when an asynchronous sequential circuit changes two or more binary states variable is known as? ( ) a. Deadlock condition b. Running condition c. Race condition d. Live lock	VI	CO6
5M-7	Time delay device is the memory element of ? ( ) a. Unclocked flip-flops b. Clocked flip-flops c. Synchronous circuits d. Asynchronous circuits	VI	CO5
5M-8	Asynchronous sequential logic circuit not uses? ( ) a) Inputs b) Outputs c) Clock pulses d) Time	II	CO6
5M-9	The analysis of asynchronous sequential circuits are used to obtain? ( ) a) a table b) a diagram c) Graph	III	CO6

	d) Flow chart		
5M-10	In the design procedure of the asynchronous circuit ,the flow of the table ( ) a) Increased to maximum states b) Reduced to maximum states c) Changed d) Remain same	VI	CO6
5M-11	RAM is also known as _____ ( ) a) RWM b) MBR c) MAR d) ROM	I	CO5
5M-12	If a RAM chip has n address input lines then it can access memory locations up to ____ ( ) a) $2^{(n-1)}$ b) $2^{(n+1)}$ c) 2^{n} d) 2^{2n}	III	CO5
5M-13	The n bit address is placed in the _____ ( ) a) MBR b) MAR c) RAM d) ROM	VI	CO5
5M-14	Which of the following is not a type of memory? ( ) a) RAM b) FPROM c) EEPROM d) ROM	I	CO5
5M-15	The chip by which both the operation of read and write is performed? ( ) a) RAM b) ROM c) PROM d) EPROM	II	CO5

#Filling The Blank Questions			
5F-1	How many address bits are needed to select all memory locations in the 2118 16K X 1RAM _____.	I	CO5
5F-2	The storage element for a static RAM is the _____.	II	CO5
5F-3	The condition occurring when two or more devices try to write data to bus Simultaneously is called _____.	III	CO5
5F-4	A 64 bit word consists of _____byte.	IV	CO5
5F-5	How many 2K X 8 ROM chips would be required to build a 16K X 8 memory System _____.	I	CO5
5F-6	ROM is made up of _____. A PLA is similar to a ROM in concept except that_____.	I	CO5
5F-7	Why ROMs are called non-volatile memory _____.	II	CO5
5F-8	PLA contains _____.	II	CO5
5F-9	A _____ is said to exist in an asynchronous sequential circuit when two or more binary variables change value in response to a change in an input variable.	VI	CO6
5F-10	The _____ method of analysis can be useful in detecting the occurrence of instability.	IV	CO6
5F-11	A _____ is one that removes the series of pulses that result from a contact bounce and produce a single smooth transition of the binary signal from 0 to 1 or from 1 to 0.	I	CO6
5F-12	The _____ is a chart that consists of squares, one for every possible pair of states, that provides spaces for listing any possible implied states.	IV	CO6
5F-13	The _____ compatible is a group of compatibles that contains all the possible combinations of compatible states.	I	CO6
5F-14	An n-state compatible is represented in the _____ diagram by an n-sided polygon with all its diagonals connected.	I	CO6
5F-15	_____ are unwanted switching transients that may appear at the output of a circuit because different paths exhibit different propagation delays .	1	CO6
#MatchTheFollowing Questions			
5M-1	Match the following a) RAM (i) Programmable Read-Only Memory b) ROM (ii) Random access memory c) EPROM (iii) Read-Only memory d) PROM (iv) Electrically Erasable Programmable Read only memory	II	CO5

5M-2	Match the following a) DRAM (i) Hard disk b) SRAM (ii) Chip c) RAM (iii) a capacitor d) ROM (iv) a Transistor	I	CO5
5M-3	Match the following a) PROM (i) Programmable b) PAL (ii) Programmable AND gate & Programmable OR c) PLA (iii) Programmable AND gate & fixed OR array d) PLD (iv) Permanent and cannot be changed	III	CO5
5M-4	Match the following a) Static hazard (i) Output changes for two adjacent inputs b) Dynamic hazard (ii) Input changes and the output to change c) Essential hazard (iii) Unequal delays along two or more paths d) RAM (iv) Main memory	I	CO6
5M-5	Match the following a) Error detection and correction check(CRC) (i) Parity check and cyclic redundancy b) Memory decoder (ii) Addresses are used to identify the specific memory lo cation c) Latch (iii) Circuit that store a signal bit of information d) RAM (iv) Non-volatile memory	I	CO5

#5MARKSQUESTIONS			
1.	What is memory decoding?	I	CO5
2.	What is Sequential (or simple) programmable logic device (SPLD)	I	CO5
3.	What is hazard? What are the various types of hazard that may be encountered in a combinational logic? Explain in detail how hazards are eliminated?	II	CO6
4.	Discuss About Binary Cell In Detail?	VI	CO5
5.	What is Race -free state assignment hazard?	I	CO6
6,	Distinguish between a PAL & a PLA.	IV	CO5
7.	Explain about programmable array logic?	II	CO5
8.	Explain about programmable logic array?	II	CO5
9.	Discuss about error detection and correction	VI	CO5
10.	Compare the read only memory(ROM) and random access memory(RAM)?	IV	CO5
11.	Discuses about state reduction table?	VI	CO6
12.	Define static hazard, Dynamic hazard and Essential Hazard & compare?	I	CO6
13.	Explain about circuits with latches and types of latches?	II	CO6
14.	State assignment to modified flow table and Multiple row assignment?	I	CO6
15.	Explain about Error detection and Correction?	II	CO6

WEB REFERENCES FOR DIGITAL ELECTRONICS

W1.https://www.ee.iitb.ac.in/~sequel/ee101/ee101_dgtl_4.pdf
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W13.http://faculty.kfupm.edu.sa/COE/ashraf/RichFilesTeaching/COE022_200/Chapter4_1.htm
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CONTENT BEYOND THE SYLLABUS

S.No	Topics	Proposed Actions	Date	Resource Person/Mode	POs	PSOs
1.	**Finite State Machines**	**PPTS**	**07/11/2026**	**Dr. Nageshwar Rao**	**1**	**1**
2.	**Timing Analysis,Setup/Hold Time**	**PPTS**	**20/11/2026**	**Dr. Manwinder Singh**	**1**	**1**

SELF STUDY TOPICS

S.No	Topics	Books&Journals	Course Outcome
1.	Combination &Sequential circuits	DIGITAL DESIGN Sixth edition,M.Morris Mano	**CO3,CO4**
2.	Memories	Switching and Finite Automata Theory by Zvi.Kohavi,Tata McGraw Hill.	**CO5**

Prepared by	Recommended and Approved by
D.JYOTHI	HOD/AIDS

II B.TECH I SEM MID-I DIGITAL ELECTRONICS ASSIGNMENT QUESTIONS A.Y 2025-2026

(1. Remembering 2. Understanding, 3. Applying 4. Analyzing, 5. Evaluating 6. Creating)

	SET-1	BT Level	Course Outcome
1	Explain are the rules for Excess-3 addition? Add two decimal numbers 123 and 658 in Excess-3 code?	II	COI
2	Apply theorems simplify the logic function i) F (A, B, C, D) = AB+AC+C+AD+ABC+ABC ii) F (A, B, C, D) = AC+ABC+BC	III	CO1
3	C) What is don't care condition? D) Simplify the expression by using QC method &Realize by using NAND gates f(A,B,C,D,E)=∑m(0,1,9,15,24,29,30)+∑d(8,11,31)?	IV	CO2
4	A)Determine the Boolean expression for given function by using K-map f (A, B, C) =∑ (0, 1,2, 4,5) ? B)Reduce the following function using K-map f(A,B,C,D) = ΠM (0,2,3,8,9,12,13,15) ?	V	CO2
5	Explain 4 bit parallel adder and 4 bit parallel subtractor?	VI	CO3
	SET-2		
1	Explain duality &minimize the following Boolean expressions. v. B'C'D+(B+C+D)'+B'C'D'E vi. AB+(AC)'+AB'C(AB+C) vii. A'B'C'+A'BC'+AB'C'+ABC' viii. A+B+A'B'C	II	CO1
2	Choose &write the minterms and maxterms for the following functions i) F=∑m(1,4,6,7,9) ii) F=πm(3,5,7,11,14) iii) State and prove Demorgan's theorems	III	CO1
3	A)Compare between pair and quads? B)Simplify the expression by using K-map Y = ∑m (1,5,7,911,13,15) ?	IV	CO2
4	Choose NAND gates to Implement boolean expression for EX-OR gate?	V	CO2
5	What is multiplexer? Design 8 to 1 mux using two 4 to 1 mux?	VI	CO3
	SET-3		
1	A) Explain &Justify the BINARY TO GRAY and GRAY TO BINARY WITH (10110011)? B) Explain &Justify with your answer Why are NAND and NOR gates known as universal gates?	II	CO1
2	Construct the logic gate diagram for the expression [(A+B).C]'D by using NAND gate?	III	CO1
3	Analyze &construct a logic diagram using only two input NAND gate to implement the following expression (AB + A'B')(CD' + C'D)	IV	CO2
4	Explain about Karnaugh map? 4-variable k- map?	V	CO2
5	Discuss the applications of multiplexer and demultiplexer	VI	CO3
	SET-4		
1	**Explain the different logic gates with truth tables and Properties of Ex-or gate?**	**II**	**CO1**
2	Solve i .(110101.0101)2__()8 ii .(125.62)8__()2 iii.(11001101.110110)2__()16 iv .(8A9.B4)16__()2 v .(615.25)8__()16 vi .(BC66.AF)16__()8	III	CO1
3	Simplify the SOP expression by using 5 variable K-map F(A,B,C,D) =∑m(0,2,5,7,13,15,18,20,21,23,28,29,31) ?	IV	CO2
4	Explain about the product of sum? Reduce the expression by using K-map method Y=(A'+B'+C+D)(A'+B'+C'+D)(A'+B'+C'+D')(A+B'+C'+D)(A+B+C+D)(A'+B'+C+D')(A+B'+C'+D')(A'+B+C+D)	V	CO2
5	Discuss about combinational circuits?	VI	CO3

	SET-5		
1	Translate or Convert the following i. (AF.B9)16 = ( )10 ii. (126.75)8 = ( )10 iii. (1 1 0 1 1 . 1 1 0 1)2 = ( )10 iv. (1 5 3)10 =( )2	II	CO1
2	Construct the logic gate diagram for the expression [(A+B).C]'D by using NAND gate ?	III	CO1
3	Distinguish between the OR-OR & AND-AND Implementation?	IV	CO2
4	Explain about the NAND-NOR Implementation?	V	CO2
5	Discuss about Binary Multiplier?	VI	CO3
	SET-6		
1	Explain Boolean algebra laws and rules? &State Duality Theorem?	II	CO1
2	Solve the following i. (AF.B9)16 = ( )10 ii. (126.75)8 = ( )10 iii. (1 1 0 1 1 . 1 1 0 1)2 = ( )10 iv. (1 5 3)10 =( )2	III	CO1
3	Simplify the function using tabular method (or) QUINE- MCCLUSKEY method f(A,B,C,D) = ∑(0,2,3,6,7,8,10,12,13)?	IV	CO2
4	A)Determine the Boolean expression for given function by using K-map f (A, B, C) =∑ (0, 1,2, 4,5) ? B)Reduce the following function using K-map f(A,B,C,D) = ΠM (0,2,3,8,9,12,13,15) ?	V	CO2
5	Discuss the applications of multiplexer and demultiplexer?	VI	CO3
	SET-7		
1	Explain Boolean algebra laws and rules? &State Duality Theorem?	II	CO1
2	Solve i .(110101.0101)2__()8 ii .(125.62)8__()2 iii.(11001101.110110)2__()16 iv .(8A9.B4)16__()2 v .(615.25)8__()16 vi .(BC66.AF)16__()8	III	CO1
3	Simplify the following function using K-map f(A,B,C,D) = ΠM (0,2,3,8,9,12,13,15) ?	IV	CO2
4	Evaluate the function using tabular method (or) QUINE- MCCLUSKEY method Y =A'BC'D'+A'BC'D+ABC'D'+ ABC'D+ AB'C'D+A'B'CD'?	V	CO2
5	Discuss 4 bit parallel addar and 4 bit parallel subtractor?	VI	CO3
	SET-8		
1	C) Translate the given SOP into POS form f(A,B,C,D)=∑m(0,2,4,6, 8,10,12,14) D) Construct the logic diagram of Y = AC+ABC+A'BC+AB+D	II	CO1
2	Construct the logic diagram of NOR- NOR implementation of Y = AC+BC+AB+D?	III	CO1
3	Simplify the SOP expression by using 5 variable K-map F(A,B,C,D) =∑m(0,2,5,7,13,15,18,20,21,23,28,29,31) ?	IV	CO2
4	Explain about the NAND-NOR Implementation?	V	CO2
5	Discuss & draw the circuit& truth table of Half Sub tractor?	VI	CO3
	SET-9		
1	Outline & Implement the function f=ABC+DE+F by using NAND-NAND implementation?	II	CO1
2	Apply Boolean algebra laws and rules state Duality theorem?	III	CO1
3	E) What is don't care condition? F) Simplify the expression by using QC method &Realize by using NAND gates f(A,B,C,D,E)=∑m(0,1,9,15,24,29,30)+∑d(8,11,31)?	IV	CO2
4	A)Determine the Boolean expression for given function by using K-map f (A, B, C) =∑ (0, 1,2, 4,5) ? B)Reduce the following function using K-map f(A,B,C,D) = ΠM (0,2,3,8,9,12,13,15) ?	V	CO2

II B.TECH I SEM MID-II DIGITAL ELECTRONICS ASSIGNMENT QUESTIONS A.Y 2025-2026

(1. Remembering 2. Understanding, 3. Applying 4. Analyzing, 5. Evaluating 6. Creating)

		BT Level	Course Outcome
	SET-1		
1	What is comparator? Construct a 2-bit comparator using logic gates?	III	CO3
2	Explain Characteristic table and Excitation table for JK flip- flop & T flip-flop?	II	CO4
3	Distinguish between Combinational circuits and Sequential circuits? Draw the D latch?	IV	CO4
4	Explain Sequential (or simple) programmable logic device (SPLD) with example.	V	CO5
5	Construct the logic gate diagram for the expression [(A+B).C]'D by using NAND gate ?	III	CO6
	SET-2		
1	Construct the following functions using Multiplexer F1 = m(2, 3, 6, 8, 12) F2 = m(1, 3, 5, 6, 7, 8, 10)	III	CO3
2	Sketch& Explain the using NAND gates?	II	CO4
3	What is the drawback of JK flip-flop, analyze a flip-flop which overcomes this drawback and explain with neat diagram?	IV	CO4
4	Explain About Binary Cell In Detail?	V	CO5
5	What is hazard? Classifications of hazards that may be encountered in a combinational logic? Explain in detail how hazards are eliminated?	IV	CO6
	SET-3		
1	Construct Octal to Binary or 8:3 Encoders using OR gates?	III	CO3
2	Show SR flip- flop from JK flip- flop?(conversion of JK to SR)	II	CO4
3	Distinguish between latch and flip- flop? Draw the SR latch?	IV	CO4
4	Explain the design procedure of a PAL with example.	V	CO5
5	Explain about Race -free state assignment hazard?	II	CO1
	SET-4		
1	Identify the Full Adder and Full subtractor using the 3:8 Decoders?	III	CO3
2	Discuss about shift register? &What are the applications of shift register?	II	CO4
3	Differentiate between ring counter & ripple counter?	IV	CO4
4	Explain about the product of sum? Reduce the expression by using K-map method Y=(A'+B'+C+D)(A'+B'+C'+D)(A'+B'+C'+D')(A+B'+C'+D)(A+B+C+D)(A'+B'+C'+D')(A+B'+C'+D')	V	CO2
5	Explain the design procedure of a PAL with example. Compare the ROM & RAM circuits?	VI	CO3
	SET-5		
1	Make use of logic gates, explain 8:1 Multiplexer and 1:8 Demultiplexer?	III	CO3
2	Construct the logic diagram of NOR- NOR implementation of Y = AC+BC+AB+D?	III	CO1
3	Simplify the given expression F(A,B,C,D) = ∑m(0,7,8,9,10,12)+∑d(2,5,13) using K-map ?	IV	CO2
4	Explain about the OR-OR Implementation?	IV	CO2
5	Discuss the applications of multiplexer and demultiplexer ?	VI	CO3
	SET-6		
1	Construct a FULL-Subtractor circuit and write a HDL program module for the same?	III	CO3
2	Explain the Design procedure of a sequential circuit with one example	II	CO4
3	Distinguish between Moore Model And Mealy Model?	IV	CO4
4	A)Determine the Boolean expression for given function by using K-map F(A,B,C,D) = ∑(0, 1, 2, 4, 5, 7) ? B)Reduce the following function using K-map F(A,B,C,D) = ΠM (0,2,3,8,9,12,13,15) ?	V	CO2
5	Discuss & draw the circuit& truth table of Half Sub tractor?	VI	CO3
	SET-7		
1	Translate i .(110101.0101)2__()8 ii .(125.62)8__()2 iii.(11001101.110110)2__()16 iv .(8A9.B4)16__()2 v .(615.25)8__()16 vi .(BC66.AF)16__()8	II	CO1
2	Construct the logic gate diagram for the expression [(A+B).C]'D by using NAND gate?	III	CO1
3	Explain what is Karnaugh map? 4-variable k- map?	IV	CO2
4	Explain & construct a logic diagram using only two input NAND gate to implement the following expression (AB + A'B')(CD' + C'D)	V	CO2
5	Design Full adder with 2 half adders?	VI	CO3
	SET-8		
1	Explain the rules for Excess-3 addition? Add two decimal numbers 123 and 658 in Excess-3 code?	II	CO1
2	Make use of theorems and laws simplify the logic function iii) F (A, B, C, D) = AB+AC+C+AD+ABC+ABC iv)F (A, B, C, D) = AC+ABC+BC	II	CO6
3	Simplify the SOP expression by using 5 variable K-map F(A,B,C,D) = ∑m(0,2,5,7,13,15,16,18,20,21,23,28,29,31) ?	III	CO2
4	Explain about Universal Shift registers.	II	CO4
5	What is sequential machine? Distinguish between synchronous& Asynchronous sequential circuits?	V	CO4
	SET-9		
1	Translate i .(110101.0101)2__()8 ii .(125.62)8__()2 iii.(11001101.110110)2__()16 iv .(8A9.B4)16__()2 v .(615.25)8__()16 vi .(BC66.AF)16__()8	II	CO1
2	Sketch& Explain the using NAND gates?	II	CO4
3	What is the drawback of JK flip-flop, analyze a flip-flop which overcomes this drawback and explain with neat diagram?	IV	CO4
4	Explain About Binary Cell In Detail?	V	CO5
5	What is hazard? Classifications of hazards that may be encountered in a combinational logic? Explain in detail how hazards are eliminated?	IV	CO6
	SET-10		
1	Translate i .(110101.0101)2__()8 ii .(125.62)8__()2 iii.(11001101.110110)2__()16 iv .(8A9.B4)16__()2 v .(615.25)8__()16 vi .(BC66.AF)16__()8	II	CO1
2	Construct the logic gate diagram for the expression [(A+B).C]'D by using NAND gate?	III	CO1
3	Explain what is Karnaugh map? 4-variable k- map?	IV	CO2
4	Explain & construct a logic diagram using only two input NAND gate to implement the following expression (AB + A'B')(CD' + C'D)	V	CO2
5	Design Full adder with 2 half adders?	VI	CO3
	SET-11		
1	Construct Octal to Binary or 8:3 Encoders using OR gates?	III	CO3
2	Show SR flip- flop from JK flip- flop?(conversion of JK to SR)	II	CO4
3	Distinguish between latch and flip- flop? Draw the SR latch?	IV	CO4
4	Explain the design procedure of a PAL with example.	V	CO5
5	Explain about Race -free state assignment hazard?	II	CO1
	SET-12		
1	Identify the Full Adder and Full subtractor using the 3:8 Decoders?	III	CO3
2	Discuss about shift register? &What are the applications of shift register?	II	CO4
3	Differentiate between ring counter & ripple counter?	IV	CO4
4	Explain about the product of sum? Reduce the expression by using K-map method Y=(A'+B'+C+D)(A'+B'+C+D')(A'+B'+C'+D)(A+B'+C'+D)(A+B+C+D)(A'+B'+C'+D')(A+B'+C'+D')	V	CO2
5	Explain the design procedure of a PAL with example. Compare the ROM & RAM circuits?	VI	CO3
	SET-13		
1	Translate i .(110101.0101)2__()8 ii .(125.62)8__()2 iii.(11001101.110110)2__()16 iv .(8A9.B4)16__()2 v .(615.25)8__()16 vi .(BC66.AF)16__()8	II	CO1
2	Explain about Universal Shift registers.	II	CO4
3	Simplify the given expression F(A,B,C,D) = ∑m(0,7,8,9,10,12)+∑d(2,5,13) using K-map ?	IV	CO2
4	Explain about the OR-OR Implementation?	IV	CO2
5	Discuss the applications of multiplexer and demultiplexer ?	VI	CO3
	SET-14		
1	Outline & Implement the function f=ABC+DE+F by using NAND-NAND implementation?	II	CO1
2	Define and explain about state diagram, state table, state reduction and state assignment?	II	CO1
3	Simplify the function using tabular method (or) QUINE- MCCLUSKEY method f(A,B,C,D) = ∑(0,2,3,6,7,8,10,12,13)?	IV	CO2
4	Discuss about error detection and correction		CO5
5	Apply Boolean algebra laws and rules state Duality theorem?	II	CO6

4	Discuss about memory decoding?	V	CO5
5	Explain about static hazard, Dynamic hazard and Essential Hazard? Discuses about state reduction table?	II	CO6
	SET-7		
1	Construct BCD or Decimal adder using two 4 bit adders?	III	CO3
2	Explain the design of a Synchronous Sequential Circuit by using any flip-flop?	II	CO4
3	Classification of shift Registers & applications?	IV	CO4
4	Explain about circuits with latches and types of latches?	V	CO5
5	Explain a) Fundamental mode operation b) Debounce circuit	II	CO6
	SET-8		
1	Applying three bit inputs, explain the working of Binary Multiplier?	III	CO3
2	Explain about Synchronous counters and draw the timing diagram for 3 bit up/down counter?	II	CO4
3	Analyze a sequential circuit by considering an example.	IV	CO4
4	Discuss about Complex programmable logic device.	V	CO5
5	Explain static Hazard and dynamic hazard?	II	CO6
	SET-9		
1	Construct a 4x16 decoder using five 2x4 decoders modules with neat schematic diagram.	III	CO3
2	Convert JK flip- flop to SR flip-flop?	II	CO4
3	Distinguish between Synchronous and Asynchronous counters	IV	CO4
4	Discuss the advantages of PROM over PLA and PAL.	V	CO5
5	Explain the procedure for analyzing an asynchronous sequential circuit with SR latches with an example.	II	CO6
	SET-10		
1	Construct the following functions using Multiplexer F1 = m (2, 3, 6, 8, 12) F2 = m (1, 3, 5, 6, 7, 8, 10)	III	CO3
2	Sketch& Explain the D & T flip-flop using NAND gates?	II	CO4
3	Draw the logic diagram and timing diagram of Asynchronous decade counter and distinguish between decade counter and 4 bit counter	IV	CO4
4	Explain about Sequential (or simple) programmable logic device (SPLD)	V	CO5
5	Explain the block diagram of Asynchronous Sequential circuit	II	CO6
	SET-11		
1	Construct a 4x16 decoder using 3x8 decoders with an additional logic.	III	CO3
2	Explain about SR flip-flop and Jk flip-flop with diagrams.	II	CO4

3	Design a synchronous mod-10 Counter.	VI	CO4
4	Discuss about ROM with internal logic diagram and its types.	V	CO5
5	Explain about Race -free state assignment hazard?	II	CO6
	SET-12		
1	Build a 4 bit Binary Adder and explain	III	CO3
2	Construct a shift register? What are the applications of shift register?	II	CO4
3	Differentiate between ring counter & ripple counter?	IV	CO4
4	Discuss about Sequential Programmable Devices.	V	CO5
5	Explain about Transition table and Excitation table with example.	II	CO6
	SET-13		
1	Construct 8:1 Multiplexer and 1:8 Demultiplexer and explain.	III	CO3
2	Explain how to design D flip-flop and T flip-flop from JK flip-flop.	II	CO4
3	What is sequential machine? Distinguish between synchronous& Asynchronous sequential circuit?	IV	CO4
4	Discuss about error detection and correction	V	CO5
5	Explain the read only memory (ROM) and random access memory (RAM)?	II	CO6
	SET-14		
1	Construct a FULL-Subtractor circuit and write a HDL program module for the same?	III	CO3
2	Explain the Design the sequential circuit for given state diagram with one example	II	CO4
3	Distinguish between Moore Model And Mealy Model?	IV	CO4
4	Discuss about a PAL, PLA, ROM, RAM?	V	CO5
5	What is hazard? What are the various types of hazard that may be encountered in a combinational logic? Explain in detail how hazards are eliminated?	II	CO6

BR-22

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QC3156

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi) - Recognized under 2(f) and 12(B) of UGC Act 1956

II B.Tech. II Semester (REG & SUPPL) End Examinations – JUNE 2025

(R22ECE2112) DIGITAL ELECTRONICS

28/06/2025 (For EEE & AIDS) Day-3(FN)

Duration: 3 Hrs Maximum Marks: 60M

Blooms Taxonomy : (I-Remembering, II-Understanding, III-Applying, IV-Analyzing, V-Evaluating and VI-Creating)

Course Outcomes : CO

PART – A

Answer ALL the following questions. (10Qx1M=10M)

1.	a)	Write the equivalent number $(2378)_{10}$ in hexadecimal.	I	CO1
	b)	State De-Morgan's theorem.	I	CO1
	c)	What is prime implicant?	I	CO2
	d)	Represent the 3 variable k-Map in SOP and POS forms.	I	CO2
	e)	Define full subtractor.	I	CO3
	f)	Implement the function F = Σm(0,2,3) using 4*1 MUX.	II	CO3
	g)	Distinguish between combinational and sequential circuits.	II	CO4
	h)	Write the characteristics table for T flip flop.	I	CO4
	i)	Give the comparison of PROM, PAL and PLA.	II	CO5
	j)	Implement the function by using PROM f(A,B,C) = Σm(0,1,2,6,7).	II	CO5

PART – B

Answer FIVE questions choosing at least one from each unit. (5Qx10M=50M)

UNIT-I

2a.		Explain different types of number systems with example.	II	CO1
		(OR)		
2b.		Convert the following to decimal. (i) $(10111)_2$ (ii) $(ABCD)_{16}$ (iii) $(7234)_8$ (iv) $(1110)_2$	III	CO1

UNIT-II

3a.		Minimize using K-map and realize by NAND gates. F(A,B,C,D)=Σ(0,1,2,3,12,13,14,15).	III	CO2
		(OR)		
3b.		i) Minimize and realize, $F = (X' + Y' + Z)' + Z + W$ by basic gates. ii) Realize Ex-OR and Ex-NOR gate operations by NOR gates.	V	CO2

UNIT-III

4a.		Implement the following function using a 16 x 1 MUX. $F(A, B, C, D) = \sum(1,3,4,11,12,13,14,15)$.	IV	CO3
		(OR)		
4b.		i) Implement F=Σ(0,1,2,3) using decoder. ii) Design binary multiplier.	III	CO3

P.T.O

UNIT-IV

5a.	Design a 4 bit universal shift register with neat diagram.	IV	CO4
	(OR)		
5b.	i) Develop 3 bit ripple up counter.	IV	CO4
	ii) Create the circuit of JK flip-flop using NAND gates and explain its operation.		

UNIT-V

6a.	Implement the following functions using PLA with three inputs, four product terms and two outputs. F1 (A, B, C) = ∑m (3, 5, 6, 7), F2 (A, B, C) = ∑m (0, 2, 4, 7).	III	CO5
	(OR)		
6b.	Design the reduction of state and flow tables with an example.	III	CO5

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BR-22

HT.No. 23D45A3301. D4

QC2586

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi) - Recognized under 2(f) and 12(B) of UGC Act 1956

II B.Tech. I Semester (REG & SUPPL) End Examinations, DECEMBER – 2024.

(R22ECE2112) DIGITAL ELECTRONICS

31/12/2024 (For CSE, CS, DS, IoT, CSIT & IT) Day-1(FN)

Duration: 3 Hrs (Assume the data wherever required) **Maximum Marks: 60M**

Blooms Taxonomy : (I-Remembering, II-Understanding, III-Applying, IV-Analyzing, V-Evaluating and VI-Creating)

Course Outcomes : CO

PART – A

Answer ALL the following questions. (10Qx1M=10M)

1.	a)	Determine the missing member in the given series 10000, 121, 100, ?, 24, 22, 20.	II	CO1
	b)	Write axiomatic definition of Boolean Algebra.	I	CO1
	c)	Draw the symbol of Three Input EX-OR gate.	II	CO2
	d)	Form the Truth Table for Two Input EX-NAND gate.	I	CO2
	e)	Realize given function $f(a,b) = \sum(1,3)$ using basic gates.	II	CO3
	f)	Write down the acronym of VHDL.	II	CO3
	g)	Write the operating characteristics of Flip-Flops.	II	CO4
	h)	Mention the number of Flip-Flops required for MOD-6 counter.	I	CO4
	i)	Is RAM volatile or not? Justify.	I	CO5
	j)	Mention the type of gates used in PAL.	I	CO5

PART – B

Answer FIVE questions choosing at least one from each unit. (5Qx10M=50M)

UNIT-I

2a.		i) Explain about AND, OR, NOT logic gates along with symbol and truth tables. ii) Construct a truth table for a given expression $AB + CD$.	II	CO1
		(OR)		
2b.		i) Write and explain about the basic laws of Boolean algebra. ii) Obtain the canonical and standard forms of given function $f_1 = (AB'(C + BD) + A'B')C$?	III	CO1

UNIT-II

3a.		I) Explain about terms i) Minterms ii) Maxterms with help of 4-variable k-map and explain about limitations of K-map. II) Obtain prime implicants for the functions (i) $f_1(x,y,z) = \sum(0,2,4,6)$ (ii) $f_2(w,x,y,z) = \sum(0,1,2,4,8,11) + \Phi(6,9)$.	II	CO2
		(OR)		
3b.		i) What is K-map and illustrate representation of product terms in 3-variable k-map and cell adjacency? ii) Minimize the given function $f_7 = \sum(1,5,6,12,13,14) + \emptyset(2,4)$ hence implement using NOR gates only.	IV	CO2

P.T.O

UNIT-III

4a.	i) Explain about the concept of encoder with the help of diagrams. ii) Realize magnitude comparator along with truth table.	III	CO3
	(OR)		
4b.	i) Explain the concept of Half-Adder along with truth table. ii) Design $f = \prod (0,1,3,7,9,10,11,13,14,15)$ using 8:1 multiplexer.	II	CO3

UNIT-IV

5a.	i) Design the conversion of JK FF to (i) D FF and (ii) T FF hence mention the difference. ii) Obtain the Excitation tables for SR flip-flops and realize it.	III	CO4
	(OR)		
5b.	i) Illustrate Right Shift and Left Shift Registers with examples. ii) Design a counter that can count states from *0,1,2,3,4,5,6* using D-FF.	II	CO4

UNIT-V

6a.	i) Illustrate error detection and error correction capabilities of Hamming code. ii) What is Static hazard and show how it can be removed for the expression $f(x,y,z) = \sum(1,3,4,5)$.	IV	CO5
	(OR)		
6b.	i) Draw the block diagram and explain in detail about the PAL. ii) Realize $f = \sum(0,2,4,6,8,10,12,14)$ using PLA.	V	CO5

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QC2806

HT.No. P. Swetha

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi) - Recognized under 2(f) and 12(B) of UGC Act 1956

II B.Tech. II Semester (SUPPL.) End Examinations, JANUARY – 2025.

(R22ECE2112) DIGITAL ELECTRONICS

(For EEE & AIDS)

07/01/2025 **Day-3(AN)**

Duration: 3 Hrs **Maximum Marks: 60M**

Blooms Taxonomy : (I-Remembering, II-Understanding, III-Applying, IV-Analyzing, V-Evaluating and VI-Creating)

Course Outcomes : CO

Answer ALL the following questions. **PART – A** **(10Qx1M=10M)**

1.	a)	Explain universal logic gates.	II	CO1
	b)	Find the following i) $(125F)_{16} = (\quad)_{10}$ ii) $(10111111)_2 = (\quad)_{10}$	I	CO1
	c)	List and prove the Boolean Commutative Theorem.	1	CO2
	d)	Explain the excitation table and characteristic equations of JK Flip Flops.	II	CO2
	e)	How many 2:1 multiplexers do we need to make a 2 input XOR gate?	1	CO3
	f)	What is an Encoder?	1	CO3
	g)	What are the main advantages of synchronous circuit?	1	CO4
	h)	Define Sampling rate.	1	CO4
	i)	What is Cache memory?	1	CO5
	j)	How many flip-flops will be required for a Mod -100 counter?	1	CO5

Answer FIVE questions choosing at least one from each unit. **PART – B** **(5Qx10M=50M)**

UNIT-I

2a.	I) Solve the dual of the following Boolean expressions. i) AB+A(B+C)+B′(B+D) ii) A+B+A′B′C. II) Solve the following. i) Add $6E_{16}$ and $C5_{16}$ ii) Add $5D_{16}$ from $3A_{16}$	III	CO1
	(OR)		
2b.	Simplify $F(A,B,C,D) = \sum (4,5,6,7,12,13,14) + d(1,9,11,15)$ using K-map and construct the logic diagram.	IV	CO1

UNIT-II

3a.	Reduce the following function using K-Map. $F(A,B,C,D,E) = \Sigma m\,(1,4,8,10,11,20,22,24,25,26) + d(0,12,16,17)$ and develop the logic circuit for the obtained function.	II	CO2
	(OR)		
3b.	Examine and Minimize the following expression using K-map and realize using NAND Gates. $F(A,B,C,D) = \sum m(1,3,7,11,15) + \sum d(0,2,5)$	III	CO2

P.T.

UNIT-III

4a. i) Analyse the logic function $F = A \oplus B \oplus C$ using a multiplexer.
ii) With a neat design procedure, explain the implementation of a 2-bit Magnitude Comparator.

(OR)

4b. Design a 32:1 Multiplexer using two 16:1 and 2:1Multiplexers.

UNIT-IV

5a. i) Construct a 3-bit synchronous counter with T-flip flop and draw the diagram.
ii) list the differences between combinational and sequential circuit.

(OR)

5b. Construct a synchronous modulo-12 counter using JK flip-flop.

UNIT-V

6a. Differentiate between Static and Dynamic memory.

6b. Explain PLA with an example.

(OR)

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BR-22 HT.No. 22041A7208 D4 QC1950

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi) - Recognized under 2(f) and 12(B) of UGC Act 1956

II B.Tech. II Semester (REGULAR) End Examinations, JULY – 2024

(R22ECE2112) DIGITAL ELECTRONICS

12/07/2024 (For EEE & AIDS) Day-3(FN)

Duration: 3 Hrs **Maximum Marks: 60M**

Blooms Taxonomy : (I-Remembering, II-Understanding, III-Applying, IV-Analyzing, V-Evaluating and VI-Creating)

Course Outcomes : CO

PART – A

Answer ALL the following questions. **(10Qx1M=10M)**

1.	a)	What is a Parity bit?	I	CO1
	b)	Convert the binary number into decimal system $(1011010.11)^2$.	I	CO1
	c)	Represent the 3 Variable k-Map in SOP form.	II	CO2
	d)	Draw the logic diagram of NAND gate.	I	CO2
	e)	What is a Half adder?	I	CO3
	f)	Why a multiplexer is called a data selector?	II	CO3
	g)	List the various memory elements used in sequential machines.	I	CO4
	h)	Define Level Edge triggering.	I	CO4
	i)	Define Fan-in and Fan-out.	I	CO5
	j)	Write the difference between CPLD and FPGA.	I	CO5

PART – B

Answer FIVE questions choosing at least one from each unit. **(5Qx10M=50M)**

UNIT-I

2a.	Convert the following binary and then gray code. i) $(6648)_{10}$ ii) $(ABEF)_{16}$ iii) $(4423)_5$ iv) $(1234)_8$		II	CO1
	(OR)			
2b.	Minimize the expression BD+BCD'+AB'CD' and implement by using NAND and NOR gates.		IV	CO1

UNIT-II

3a.	Reduce the Boolean expressions into minimum number of literals by using theorems. i) AB+(AC)'+AB'C(AB+C) ii) (A+B+D') (A'+C+D) (A'+D')		IV	CO2
	(OR)			
3b.	i)Minimize the Boolean function f=Σm(0,1,4,5,6,7,9,11,15)+d(10,14) by using K-Map. ii)Minimize the expression BD+BCD'+AB'CD' and implement by using NAND gates.		IV	CO2

UNIT-III

4a.	Explain how multiplication can be performed using binary multiplier with neat diagrams.		II	CO3
	(OR)			
4b.	i) Implement the function F(A,B,C,D)=Σm(0,1,2,5,6,11,13,14) using 16X1,8X1 and 4X1 MUX.		III	CO3

UNIT-IV

8a.	Explain the D flip flop using NAND gates.	II	CO4
	(OR)		
8b.	What is the drawback of JK flip flop, design a flip flop which overcomes this drawback and explain with neat diagram.	VI	CO4

UNIT-V

9a.	Implement the following Boolean functions using PLA. $A(x,y,z)=\Sigma m(1,2,4,6)$ $B(x,y,z)=\Sigma m(0,1,6,7)$ $C(x,y,z)=\Sigma m(2,6)$.	III	CO5
	(OR)		
9b.	What is Hazard? Explain with suitable examples.	V	CO5

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BR-22 Ht.No. Upendar D4 QC2052

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi) - Recognized under 2(f) and 12(B) of UGC Act 1956

II B.Tech. I Semester (SUPPL) End Examinations, JULY – 2024

(R22ECE2112) DIGITAL ELECTRONICS

09/07/2024 (For CSE, CS, DS, IoT, CSIT & IT) Day-1(AN)

Duration: 3 Hrs **Maximum Marks: 60M**

Blooms Taxonomy : (I-Remembering, II-Understanding, III-Applying, IV-Analyzing, V-Evaluating and VI-Creating)

Course Outcomes : CO

PART – A

Answer ALL the following questions. (10Qx1M=10M)

1.	a)	Find the Hexadecimal number equivalent of $(10001)_2$.	I	CO1
	b)	Find the subtraction of the following binary numbers using 1's complement method. $(11101)_2 - (10100)_2$.	I	CO1
	c)	Why are NAND and NOR gates called Universal gates?	I	CO2
	d)	How many NAND gates are used to form AND gates?	I	CO2
	e)	Demonstrate 4:2 encoder.	II	CO3
	f)	Compare Multiplexer and Demultiplexer.	II	CO3
	g)	Compare the Synchronous and Asynchronous counters.	II	CO4
	h)	How many types of registers are there in digital electronics?	I	CO4
	i)	Compare RAM and ROM.	II	CO5
	j)	What is Error detection and Correction of memory?	I	CO5

PART – B

Answer FIVE questions choosing at least one from each unit. (5Qx10M=50M)

UNIT-I

2a.	i)	Find the canonical SOP form for the following Boolean function. $F(A, B, C) = A + AB + BC + AC$	III	CO1
	ii)	Find the signed 8-bit binary equivalent number for the given decimal value. a) -98 b) -67		
		(OR)		
2b.	i)	Find the canonical POS form for the following Boolean function. $f(A, B, C) = (A+B).(B+C).(C+A)$	III	CO1
	ii)	List out the laws of Boolean algebra. Prove any five laws.		

UNIT-II

3a.	i)	Make use of the k-map method to simplify the given Boolean expression. $F(A, B, C, D) = \sum m(2,4,6,8,10,12,14) + d(1,3,5,7)$	III	CO2
	ii)	Develop the following Boolean function using NAND gates. $f(X,Y,Z) = \bar{X}Y + \bar{Y} + Z$		
		(OR)		
3b.	i)	Make use of the k-map method to simplify the given Boolean expression. $F(W, X, Y, Z) = \sum m(0,1,3,5,6,9,10,14)$	II	CO2
	ii)	Develop the following Boolean function using NOR gates. $f(X,Y,Z) = XY + \bar{Y} + XZ$		

P.T.O

UNIT-III

4a.	i) Construct 8:1 Multiplexer using 4:1 Multiplexer. ii) Construct Full adder circuit.	II	CO3
	(OR)		
4b.	i) Construct 4:16 decoder using 8:3 decoders. ii) Construct Half subtractor circuit.	II	CO3

UNIT-IV

5a.	i) Demonstrate the D flip-flop and derive the excitation table. ii) Demonstrate a 2-bit synchronous up counter.	V	CO4
	(OR)		
5b.	i) Demonstrate the T flip-flop and derive the excitation table. ii)Demonstrate a 3-bit ripple up/down counter.	V	CO4

UNIT-V

6a.	i) Explain in detail about state reduction and state assignment. ii) Explain in detail about Race-free state assignment.	V	CO5
	(OR)		
6b.	i) Explain in detail about PLA and PAL. ii) Explain the role of hazards in combinational and sequential circuits.	V	CO5

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BR-22

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

D4

II B.Tech - I Semester - I Mid Term Examination, SEP/OCT-2024

(R22ECE2112) DIGITAL ELECTRONICS

(For CSE, CS, DS, IoT, CSIT and IT)

Duration: 2 Hrs **Dt: 30-09-2024, Day-1 (FN)** **Max Marks: 30M**

Part – A

Answer *All* multiple choice questions. **Marks: 10Qx1/2M = 5M**

* (L1-Remembering, L2-Understanding, L3-Applying, L4-Analyzing, L5-Evaluating, and L6-Creating.)

			*Bloom's Taxonomy Levels	Course Outcomes
1.	Choose the Complement of the expression A+B + ABC' is _____ A) (A' + B)(C' + D) B) (A + B')(C' + D) C) A' B' D) (A + B')(C + D')	[ ]	III	CO1
2.	What is the addition of the binary numbers 11011011010 and 010100101? A) 0111001000 B) 1100110110 C) 11101111111 D) 10011010011	[ ]	I	CO1
3.	Simplify the binary subtraction: 101111 – 010101 = ? A) 100100 B) 010101 C) 011010 D) 011001	[ ]	IV	CO1
4.	The logical sum of two or more logical product terms is called? A) SOP B) POS C) OR operation D) NAND operation	[ ]	IV	CO1
5.	Choose the minterms in a karnaugh map are marked with a? A) Y B) X C) 0 D) 1	[ ]	I	CO2
6.	Which of the following is not considered for forming groups in K-map? A) Rolling B) Diagonal C) Vertical D) Horizontal	[ ]	I	CO2
7.	Which of the following is equivalent to NAND-NAND realization? A) AND-OR realization B) NOR-NOR realization C) NOR-NAND realization D) NAND-NAND realization	[ ]	I	CO2
8.	Identify how many cells have 5 variable K-map? A) 16 Cells B) 8 Cells C) 32 Cells D) 4 Cells	[ ]	III	CO2
9.	Half adder circuits two binary? A) Inputs B) Outputs C) Digits D) Both A and B	[ ]	I	CO3
10.	Half subtractor is used to perform subtraction of ? A) 2 bits B) 3 bits C) 4 bits D) 5 bits	[ ]	I	CO3

Answer *All* fill in the blank questions. **Marks: 6Qx1/2M = 3M**

11.	What is the canonical sum of product form of the function Y(A,B)=A+B is _____.		I	CO1
12.	Find the addition 83 & 34 in BCD _____.		I	CO1
13.	Suppose converting any radix to decimal _____.		VI	CO1
14.	Classify how many types of Degenerative form _____.		IV	CO2
15.	What is the output of Ex-OR gate _____.		I	CO2
16.	Name the device that generates a coded output from a single active numeric input line is _____.		I	CO3

P.T.O.

Answer *All* Match the following questions. **Marks: 2Qx1M = 2M**

17.

	1.	Excess-3 code	A.	Weighted code	V CO1
	2.	BCD code	B.	Only 1-bit change	
	3.	ASCII code	C.	Self complementing during transistion	
	4.	Gray code	D.	7-bit code	

18.

	1.	Exclusive -OR	A.	(AB)'	III CO2
	2.	NAND	B.	(A+B)'	
	3.	NOR	C.	(A+B)'	
	4.	Don't care	D.	X	

Part – B

Answer any *FOUR* questions. **Marks: 4Qx5M = 20M**

19. Minimize the following Boolean expressions. VI CO1
    i. B'C'D+(B+C+D)'+B'C'D'E
    ii. AB+(AC)'+AB'C(AB+C)

20. Translate or Convert the following II CO1
    i. $(AF.B9)_{16} = (\ )_{10}$
    ii. $(126.75)_8 = (\ )_{10}$
    iii. $(11011.1101)_2 = (\ )_{10}$
    iv. $(153)_{10} = (\ )_2$

21. Solve the SOP expression by using 5 variable K-map III CO2
    $F(A,B,C,D,E) = \sum m(0,2,5,7,8,10,13,15,16,18,20,21,23,24,26,28,29,31)$.

22. Discuss about the converting AND/OR/NOT to NAND/NOR Implementation? VI CO2

23. i) Change the given SOP into POS form $f(A,B,C,D)=\sum m(0,2,4,6,8,10,12,14)$ VI CO1
    ii) Construct the logic diagram of Y = AC+ABC+A'BC+AB+D

24. i) Define combinational circuit. I CO3
    ii) Implement of Full subtractor with 2 half subtractor.

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BR-22 SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY D4

II B.Tech - I Semester - II Mid Term Examinations, December-2024

(R22ECE2112) DIGITAL ELECTRONICS

(For CSE, CS, DS, IoT, CSIT and IT)

Duration: 2 Hrs **Dt: 17-12-2024, Day-1 (FN)** **Max Marks: 30M**

Part – A

Answer *All* multiple choice questions. **Marks: 10Qx1/2M = 5M**

* (L1-Remembering, L2-Understanding, L3-Applying, L4-Analyzing, L5-Evaluating, and L6-Creating.)

			*Blooms Taxonomy Levels	Course Outcomes
1.	Identify if two numbers are not equal then the binary variable will be _____ A) 0 B) 1 C) a D) b	[ ]	III	CO3
2.	IC decoders are made with _____ A) AND gate B) XOR gate C) OR gate D) NAND gate	[ ]	I	CO3
3.	In Synchronous circuits , the present state is determined by _____ A) Unclocked flip-flops B) Clocked flip-flops C) Flip-flops D) Latches	[ ]	V	CO4
4.	Shift registers are used for _____ A) Shifting B) Rotating C) adding D) both A and B	[ ]	I	CO4
5.	What kind of operation occurs in a J-K flip-flop when both inputs J and K are Equal to 1? A) Preset operation B) Reset operation C) Clear operation D) Toggle operation	[ ]	I	CO4
6.	A Johnson counter, constructed with N flip-flops, has how many unique states? A) N B) 2^N C) 2^{N+1} D) N^2	[ ]	III	CO4
7.	The change in state occurs during _____ A) Pulse Transition B) Outputs C) Clock pulses D) Inputs	[ ]	III	CO4
8.	The complexity of the asynchronous circuit is involved in timing problems of ___ A) Inputs B) Outputs C) Clock pulse D) Feedback path	[ ]	III	CO6
9.	The n bit address is placed in the _____ A) MBR B) MAR C) RAM D) ROM	[ ]	VI	CO5
10.	The chip by which both the operation of read and write is performed? A) RAM B) ROM C) PROM D) EPROM	[ ]	II	CO5

Answer *All* fill in the blank questions. **Marks: 6Qx1/2M = 3M**

11.	A _____ is a combinational circuit that compares two numbers.	IV	CO3
12.	A Johnson counter ,constructed with N flip-flops,has how many unique states_____.	I	CO4
13.	The characteristic equation of an SR flip-flop is given by _____.	VI	CO4
14.	Which of the flip-flop cannot be converted to D flip-flop _____	I	CO4
15.	The _____ method of analysis can be useful in detecting the occurrence of instability	IV	CO6
16.	A _____ is one that removes the series of pulses that result from a contact bounce and produce a single smooth transition of the binary signal from 0 to 1 or from 1 to 0.	I	CO6

P.T.O.

Answer *All* Match the following questions. **Marks: 2Qx1M = 2M**

17.

1.	Latch	A.	Level triggering	VI	CO4
2.	Flip-Flop	B.	Edge triggering		
3.	Register	C.	Memory element		
4.	Counter	D.	Store 1 bit information		

18.

1.	Static hazard	A.	Output changes for two adjacent inputs	I	CO6
2.	Dynamic hazard	B.	Input changes and the output to change		
3.	Essential hazard	C.	Unequal delays along two or more paths		
4.	RAM	D.	Main memory		

Part – B

Answer any *FOUR* questions. **Marks: 4Qx5M = 20M**

19.	Explain about 8:1 Multiplexer and 1:8 De-multiplexer using logic diagram.	II	CO3
20.	Write the Characteristic table and Excitation table for JK flip- flop & T flip-flop.	I	CO4
21.	Construct the state table & state diagram for sequential circuit with one example.	III	CO4
22.	What is Sequential (or simple) programmable logic device (SPLD)?	I	CO5
23.	Distinguish between PAL and PLA.	IV	CO5
24.	Compare static Hazard and dynamic hazard.	II	CO6

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BR-22 **SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY** **D4**

II B.Tech - II Semester - I Mid Term Examinations, MARCH – 2025

(R22ECE2112) DIGITAL ELECTRONICS

(For EEE & AIDS)

Duration: 2 Hrs **Dt: 25-03-2025, Day-2 (FN)** **Max Marks: 30M**

Blooms Taxonomy Levels : I-Remembering, II-Understanding, III-Applying, IV-Analyzing, V-Evaluating, and VI-Creating.

Course Outcomes: CO

Part – A (10 Marks)

SECTION A1: Answer *All* multiple choice questions. **Marks: 10Qx1/2M = 5M**

1.	In Boolean algebra, the OR operation is performed by which properties ? A) associative properties B) commutative properties C) distributive properties D) all of the mentioned	[ ]	I	CO1
2.	What is the addition of the binary numbers 11011011010 and 010100101? A) 0111001000 B) 1100110110 C) 11101111111 D) 10011010011	[ ]	I	CO1
3.	DeMorgan's theorem states that _____ A) (AB)'=A'+B' B) (A+B)' =A'*B C) A'+B'=A'B' D) (AB)' = A'+B	[ ]	III	CO1
4.	The primary use of Gray code is _____. A) Coded representation of a shift's mechanical position B) Turning on/off software switches C) To represent the correct ASCII code to indicate the angular position of a shaft on rotating machinery D) To convert the angular position of a shaft on rotating machinery into hexadecimal code	[ ]	I	CO1
5.	Choose the minterms in a karnaugh map are marked with a_____. A) Y B) X C) 0 D) 1	[ ]	I	CO2
6.	Map method provides a straight forward procedure for _____ A) Minimizing Boolean function B) Minimizing sop C) Minimizing pos D) Minimizing boxes	[ ]	I	CO2
7.	Which of the following is not considered for forming groups in K-map? A) Rolling B) Diagonal C) Vertical D) Horizontal	[ ]	I	CO2
8.	What value is to be considered for a " don't care condition"? A) 0 B) 1 C) Either 0 or 1 D) Any number except 0 and 1	[ ]	I	CO2
9.	Code conversion circuits mostly uses_____ A) AND-OR gates B) AND gates C) OR gates D) XOR gates	[ ]	I	CO3
10.	Full Adder combinational circuits has 3 inputs and _____ A) 2 outputs B) 1 output C) 3 outputs D) None	[ ]	I	CO3

SECTION A2: Answer *All* fill in the blank questions. **Marks: 6Qx1/2M = 3M**

11.	The expression Y=AB+BC+AC shows the_____ operation	I	CO1
12.	What is the canonical sum of product form of the function Y(A,B)=A+B is _____.	I	CO1
13.	Summarize a variable on its own or in its complemented form is known as a _____.	II	CO1
14.	Assume how many cells have 4 variable K-map _____.	IV	CO2
15.	Apply product of sum form is a method (or form) of simplifying _____.	III	CO2
16.	Construct a 2 bit binary multiplier can be implemented using _____.	III	CO3

P.T.O

SECTION A3: Answer *All* Match the following questions **Marks: 2Qx1M = 2M**

17.

1.	Counting		A.	ROM	IV CO1
2.	Decoding		B.	Multiplexer	
3.	Data selecting		C.	Demultiplexer	
4.	Code conversion		D.	Register	

18.

1.	2-variable map		A.	32 Cells	II CO2
2.	3-variable map		B.	16 Cells	
3.	4-variable map		C.	8 Cells	
4.	5-variable map		D.	4 Cells	

Part – B (20 Marks)

Answer any *FOUR* questions. **Marks: 4Qx5M = 20M**

19. What are the rules for Excess-3 addition? Add two decimal numbers 123 and 658 in Excess-3 code? — I CO1

20. Simplify the logic function — IV CO1
    i) F (A, B, C, D) = AB+AC+C+AD+ABC+ABC
    ii) F (A, B, C, D) = AC+ABC+BC

21. Convert the following number systems : — V CO1
    i . $(110101.0101)_2$____( )$_8$
    ii . $(125.62)_8$____( )$_2$
    iii.$(11001101.110110)_2$____( )$_{16}$
    iv . $(8A9.B4)_{16}$___( )$_2$
    v . $(615.25)_8$___( )$_{16}$
    vi .$(BC66.AF)_{16}$____( )$_8$

22. i) What is don't care condition? — I CO2
    ii) Simplify the expression by using QC method and Realize by using NAND gates
    f(A,B,C,D,E)=∑m(0,1,9,15,24,29,30)+∑d(8,11,31).

23. Solve the SOP expression by using 5 variable K-map — III CO2
    F(A,B,C,D,E) =∑m(0,2,5,7,8,10,13,15,16,18,20,21,23,24,26,28,29,31) .

24. What is multiplexer? Design 8 to 1 mux using two 4 to 1 mux? — VI CO3

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24 DuSA c102

BR-22 **SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY** D4

II B.Tech - II Semester - II Mid Term Examinations, JUNE – 2025

(R22ECE2112) DIGITAL ELECTRONICS

(For EEE & AIDS)

Duration: 2 Hrs **Dt: 13-06-2025, Day-2 (FN)** **Max Marks: 30M**

Blooms Taxonomy Levels : I-Remembering, II-Understanding, III-Applying, IV-Analyzing, V-Evaluating, and VI-Creating.

Course Outcomes: CO

Part – A (10 Marks)

SECTION A1: Answer *All* multiple choice questions. **Marks: 10Qx1/2M = 5M**

1.	Choose 2 to 4 line decoder will have _____ A) 2 Enables B) 3 enables C) 4 enables D) 8 enables	[ ]	I	CO3
2.	IC decoders are made with_____ A) AND gate B) XOR gate C) OR gate D) NAND gate	[ ]	I	CO3
3.	The shift register has an integrated circuit with the number_____ A) 74195 B) 74123 C) 74124 D) 74154	[ ]	II	CO4
4.	State box has a shape of _____ A) Square B) Rectangle C) Rhombus D) Pentagon	[ ]	I	CO4
5.	Which one of the following is not the element of the ASM chart? A) State box B) Decision box C) Data box D) Conditional box	[ ]	I	CO4
6.	A type of shift register in which the Q or Q output of one stage is not connected to the input of the next stage is _____ A) Parallel in/Serial out B) Serial in/Parallel out C) Serial in/Serial out D) Parallel in/Parallel out	[ ]	I	CO4
7.	The table that is not a part of the asynchronous analysis procedure is _____ A) Transition table B) State table C) Flow table D) Excitation table	[ ]	I	CO6
8.	Asynchronous sequential logic circuit not uses? A) Inputs B) Outputs C) Clock pulses D) Time	[ ]	II	CO6
9.	Which of the following is not a type of memory? A) RAM B) FPROM C) EEPROM D) ROM	[ ]	I	CO5
10.	The chip by which both the operation of read and write is performed? A) RAM B) ROM C) PROM D) EPROM	[ ]	II	CO5

SECTION A2: Answer *All* fill in the blank questions. **Marks: 6Qx1/2M = 3M**

11.	Construct a 2 bit binary multiplier can be implemented using _____.	III	CO3
12.	Realization or build a full adder using HA and _____gate	III	CO3
13.	A gated D latch does not have _____	IV	CO4
14.	A Johnson counter ,constructed with N flip-flops,has how many unique states_____.	I	CO4
15.	ROM is made up of _____. A PLA is similar to a ROM in concept except that_____.	I	CO5
16.	A 64 bit word consists of _____byte.	IV	CO5

P.T.O

SECTION A3: Answer *All* Match the following questions **Marks: 2Qx1M = 2M**

17. IV CO4

1.	Latch	A.	Level triggering
2.	Flip-Flop	B.	Edge triggering
3.	Register	C.	Memory element
4.	Counter	D.	Store 1 bit information

18. I CO5

1.	DRAM	A.	Hard disk
2.	SRAM	B.	Chip
3.	RAM	C.	a capacitor
4.	ROM	D.	a Transistor

Part – B (20 Marks)

Answer any *FOUR* questions. **Marks: 4Qx5M = 20M**

19.	Construct the following functions using Multiplexer. F1 = m (2, 3, 6, 8, 12) and F2 = m (1, 3, 5, 6, 7, 8, 10)	III	CO3
20.	Differentiate between ring counter and ripple counter.	IV	CO4
21.	What is a shift register? And what are the applications of shift register?	I	CO4
22.	Explain about Synchronous counters and draw the timing diagram for 3 bit up/down counter?	II	CO4
23.	Distinguish between a Programmable Array Logic and a Programmable Logic Array.	IV	CO5
24.	Discuses about state reduction table.	VI	CO6

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