Sri Indu
College of Engineering & Technology
UGC Autonomous Institution
Recognized under 2(f) & 12(B) of UGC Act 1956,
NAAC, Approved by AICTE &
Permanently Affiliated to JNTUH
Estd.2001

NAAC
NATIONAL ASSESSMENT AND ACCREDITATION COUNCIL

HANDOUT

II Year I Semester
(R22CSE2114)
Computer Organization & Architecture

DEPARTMENT OF ARTIFICIAL INTELLIGENCE AND DATA SCIENCE

ACADEMIC YEAR 2025-2026

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

(Permanently Affiliated to JNTUH, Approved by AICTE, New Delhi and Accredited by NBA, NAAC)
Sheriguda Village, Ibrahimpatnam Mandal, Ranga Reddy Dist. – 501 510

DEPARTMENT OF ARTIFICIAL INTELLIGENCE AND DATA SCIENCE

HANDOUT- INDEX

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1	Vision, Mission, PEOs, PSOs,POs& Cos
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iii)	Question Bank
iv)	End Examination Questions (Previous 3 Academic Year)
v)	Mid-1 & Mid-2 Questions (Previous 3 Academic Year)

VISION OF THE INSTITUTE

To be a premier institution in engineering & technology and management for competency, values and social consciousness.

MISSION OF THE INSTITUTE

IM1: Provide high quality academic programs, training activities and research facilities.
IM2: Promote continuous industry-institute interaction aimed at promoting employability, entrepreneurship, leadership and research aptitude among stakeholders.
IM3: Contribute to the economic and technological development of the region, state and nation.

VISION OF THE DEPARTMENT

To be a technologically adaptive centre for computing by grooming the students as top notch professionals.

MISSION OF THE DEPARTMENT

The Department has following Missions:

DM1: To offer quality education in computing.
DM2: To provide an environment that enables overall development of all the stakeholders.
DM3: To impart training on emerging technologies.
DM4: To encourage participation of stakeholders in research and development.

Program Educational Objectives(PEO's)

PEO1	**Higher Studies:** Graduate with an ability to pursue higher studies and get employment in reputed institutions and organizations.
PEO2	**Domain Knowledge:** Graduate with an ability to design and develop a product.
PEO3	**Professional Career:** Graduate with excellence by multidisciplinary approach to achieve successful professional career.
PEO4	**Life Long Learning:** Graduate with an ability to learn advanced skills to face professional competence through lifelong learning

Program Specific Outcomes(PSO's)

PSO1	To Develop software projects using standard practices and suitable programming environment.
PSO2	To identify, formulate and solve the real life problems faced in the society, industry and other areas by applying the skills of the programming languages, networks and databases learned.
PSO3	To apply computer science knowledge in exploring and adopting latest technologies in various inter- disciplinary research activities.

Program Outcomes(PO's)

PO1	**Engineering Knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO2	**Problem Analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO3	**Design / Development of Solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO4	**Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO5	**Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO6	**The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO7	**Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8	**Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9	**Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10	**Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO11	**Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	**Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

COURSE OUTCOMES (CO's)

Academic Year: 2025-26

Class: II YEAR-I SEM.

Course Name: COMPUTER ORGANIZATION AND ARCHITECTURE (R22CSE2114)

At the end of the course, the student will be able to

Course Outcomes (COs)	
C212.1	Understand the basics of instructions sets and their impact on processor design
C212.2	Demonstrate an understanding of the design of the functional units of a digital computer system
C212.3	Evaluate cost performance and design trade-offs in designing and constructing a computer processor Including memory
C212.4	Design a pipeline for consistent execution of instructions with minimum hazards
C212.5	Recognize and manipulate representations of numbers stored in digital computers.
C212.6	Demonstrate the Characteristics of Multiprocessors.

COURSE ARTICULATION MATRIX

COs	POs												PSOs		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C2102.1	3	2	-	-	3	-	2	-	-	-	-	2	2	3	2
C2102.2	3	3	-	2	2	-	-	-	-	-	-	-	3	3	2
C2102.3	3	3	-	2	2	-	2	-	-	-	-	-	3	3	2
C2102.4	3	2	3	2	-	-	2	-	-	-	-	-	3	2	1
C2102.5	3	3	3	3	2	-	-	-	3	-	-	-	3	3	1
C2102.6	3	3	3	3	-	-	2	-	3	-	-	-	3	3	1
C2102	**3**	**2.6**	**3**	**2.6**	**2.2**	**-**	**2**	**-**	**3**	**-**	**-**	**2**	**2.8**	**2.8**	**1.5**

3: High 2. Medium 1. Low

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY
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Sheriguda (V), Ibrahimpatnam, R.R.Dist, Hyderabad - 501 510

D4

ANNEXURE -III

BR-22

Lr.No.SICET/AUTO/DAE/II B.Tech Academic Calendar/30/2025

B.TECH II-YEAR I-SEM & II-SEM ACADEMIC CALENDAR
(FOR ACADEMIC YEAR : 2025-26)

Academic Calendar for B.Tech – IInd Year Students (2024 - 25 Batch), BR-22 Regulation.

I – Semester

S.No.	EVENT	PERIOD	DURATION
1.	**Commencement of class work.**	**01.08.2025 (Monday)**	
2.	1st Spell of Instructions for covering First Two and a half Units.	01.08.2025 –07.10.2025	9 Weeks
3.	I Mid Term Examinations.	08.10.2025 –10.10.2025	3 Days
4.	Submission of I Mid Term Examination Marks.	16.10.2025	
5.	2nd Spell of Instructions for Remaining Two and a half Units.	13.10.2025 – 13.12.2025	9 Weeks
6.	II Mid Term Examinations.	15.12.2025 – 17.12.2025	3 Days
7.	Preparation Holidays and Practical Examinations	18.12.2025 – 27.12.2025	1 Week
8.	Submission of II Mid Term Examination Marks.	23.12.2025	
9.	I Semester End Examinations.	29.12.2025 – 10.01.2026	2 Weeks
Commencement of Class-Work for II B.Tech - II Semester 19.01.2026			

Note: No of Working/instructional days : 92

II – Semester

S.No.	EVENT	PERIOD	DURATION
1.	**Commencement of class work.**	**19.01.2026 (Monday)**	
2.	1st Spell of Instructions for covering First Two and a half Units.	19.01.2026 – 14.03.2026	8 Weeks
3.	I Mid Term Examinations.	16.03.2026 – 18.03.2026	3 Days
4.	Submission of I Mid Term Examination Marks.	24.03.2026	
5.	2nd Spell of Instructions for Remaining Two and a half Units.	20.03.2026 – 09.05.2026	7 Weeks
6.	Continuation of remaining 2nd Spell of Instructions	25.05.2026 – 10.06.2026	2 Weeks
7.	II Mid Term Examinations.	11.06.2026 –13.06.2026	3 Days
8.	Preparation Holidays and Project Evaluation.	15.06.2026 – 20.06.2026	1 Week
9.	Submission of II Mid Term Examination Marks.	18.06.2026	
10.	II Semester End Examinations	22.06.2026 – 04.07.2026	2 Weeks

Note: No of Working/instructional days : 92

ACE CE DIRECTOR PRINCIPAL

Controller of Examination
Sri Indu College of Engineering & Technology
(An Autonomous Institution Under UGC)
Sheriguda (V), Ibrahimpatnam, R.R. Dist-501510

DIRECTOR
Sri Indu College of Engineering & Technology
(An Autonomous Institution Under UGC)
Sheriguda (V), Ibrahimpatnam, R.R. Dist-501510

PRINCIPAL
Sri Indu College of Engineering & Technology
(An Autonomous Institution Under UGC)
Sheriguda (V), Ibrahimpatnam, R.R. Dist-501510.

Sign: _____
Dr. M.V.S.S. Giridhar
Prof. of CEA; JNTUH Nominee

Sign: _____
Dr. T. Venu Gopal
Prof. of CSE; JNTUH Nominee

Sign: _____
Dr. D. Ramesh
Prof. of CSE; JNTUH Nominee

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

B.Tech - II Year – I Semester

L	T	P	C
3	0	0	3

(R22CSE2114)COMPUTER ORGANIZATION AND ARCHITECTURE

Course Objectives:

- The purpose of the course is to introduce principles of computer organization and the basic architectural concepts.
- It begins with basic organization, design, and programming of a simple digital computer and introduces simple register transfer language to specify various computer operations.
- Topics include computer arithmetic, instruction set design, microprogrammed control unit, pipelining and vector processing, memory organization and I/O systems, and multiprocessors.

Course Outcomes:

- Understand the basics of instructions sets and their impact on processor design.
- Demonstrate an understanding of the design of the functional units of a digital computer system.
- Evaluate cost performance and design trade-offs in designing and constructing a computer processor Including memory.
- Design a pipeline for consistent execution of instructions with minimum hazards.
- Recognize and manipulate representations of numbers stored in digital computers

UNIT - I

Digital Computers: Introduction, Block diagram of Digital Computer, Definition of Computer Organization, Computer Design and Computer Architecture.

Register Transfer Language and Micro operations: Register Transfer language, Register Transfer, Bus and memory transfers, Arithmetic Micro operations, logic micro operations, shift micro operations, Arithmetic logic shift unit.

Basic Computer Organization and Design: Instruction codes, Computer Registers Computer instructions, Timing and Control, Instruction cycle, Memory Reference Instructions, Input – Output and Interrupt.

UNIT – II

Micro programmed Control: Control memory, Address sequencing, micro program example, design of control unit.

Central Processing Unit: General Register Organization, Instruction Formats, Addressing modes, Data Transfer and Manipulation, Program Control.

UNIT - III

Data Representation: Data types, Complements, Fixed Point Representation, Floating Point Representation.

Computer Arithmetic: Addition and subtraction, multiplication Algorithms, Division Algorithms, Floating – point Arithmetic operations. Decimal Arithmetic unit, Decimal Arithmetic operations.

UNIT – IV

Input-Output Organization: Input-Output Interface, Asynchronous data transfer, Modes of Transfer, Priority Interrupt Direct memory Access.

Memory Organization: Memory Hierarchy, Main Memory, Auxiliary memory, Associate Memory, Cache Memory

UNIT – V

Reduced Instruction Set Computer: CISC Characteristics, RISC Characteristics.

Pipeline and Vector Processing: Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline, Vector Processing, Array Processor.

Multi Processors: Characteristics of Multiprocessors, Interconnection Structures, Interprocessor arbitration, Interprocessor Communication and Synchronization, Cache Coherence.

TEXT BOOK:

1. Computer System Architecture – M. Moris Mano, Third Edition, Pearson/PHI

REFERENCE BOOKS:

1. Computer Organization – Car Hamacher, Zvonks Vranesic, Safea Zaky, Vth Edition, McGraw Hill.
2. Computer Organization and Architecture – William Stallings Sixth Edition, Pearson/PHI.
3. Structured Computer Organization – Andrew S. Tanenbaum, 4th Edition, PHI/Pearson.

WEB-LINKS:

https://onlinecourses.nptel.ac.in/noc21_cs61/preview

Department of Artificial Intelligence and Data Science

FACULTY INDIVIDUAL TIME TABLE

Name of the Faculty: D.JYOTHI **AY: 2025-2026**
Designation: Assistant Professor **Semester: I**

Time	9:40 – 10:30	10:30 – 11:20	11:20 – 1:00		1:00 To 1:30	1:30 – 2:20	2:20 – 3:10	3:10 – 4:00
Days	**1**	**2**	**3**	**4**		**5**	**6**	**7**
Monday			COA					
Tuesday	COA					COA		
Wednesday								
Thursday								
Friday							COA	
Saturday			COA					

S.NO.	SUBJECT CODE	SUBJECT	CLASS	No. of Hours
1	R22CSE2114	Computer Organization and Architecture	II YEAR AIDS	5

Faculty Signature **Head of the Department**

	SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY LESSON PLAN (Regulation :R22) Department of AIDS	Prepared on Rev1: Page: 10 of 7
	Sub. Code & Title	**R22CSE2114 Computer Organization and Architecture**
	Academic Year: 2025-26	**Year/Sem./Section** **II-I**
	Faculty Name & Designation	**D.JYOTHI, Assistant Professor**

Unit/ Item No.	Topic (s)	Book Reference	Page (s)		Teaching Methodology	Proposed No. of Periods	Actual Date of Handled	CO/RBT
			From	To				
	UNIT-I							
1	**INTRODUCTION –DIGITAL COMPUTERS**					**15**		
1.1	**Digital Computers:** Introduction	T1	1	11	Black board	01		CO1,L2
1.2	Block diagram of Digital Computer	T1	15	16	Black board	01		CO1,L6
1.3	Definition of Computer Organization, Computer Design and Computer Architecture.	T1	3	4	Black board	01		CO1,L1
1.4	**Register Transfer Language and Micro operations**: Register Transfer language.	T1	111	112	Black board	01		CO1,L2
1.5	Register Transfer	T1	112	115	Black board	01		CO1,L2
1.6	Bus and memory transfers	T1	115	119	Black board	01		CO1,L1
1.7	logic micro operations	T1	125	130	Black board	01		CO1,L3
1.8	shift micro operations	T1	130	133	Black board	01		CO1,L3
1.9	Arithmetic logic shift unit.	T1	133	135	Black board	01		CO1,L3
1.10	Basic Computer Organization and Design:	T1	141	144	Black board	01		CO1,L2
1.11	Computer Registers	T1	144	149	Black board	01		CO1,L1
1.12	Computer instructions	T1	149	153	Black board	01		CO1,L2
1.13	Timing and Control	T1	153	156	Black board	01		CO1,L1
1.14	Instruction cycle	T1	156	161	Black board	01		CO1,L4
1.15	Memory Reference Instructions, Input – Output and Interrupt.	T1	162	172	Black board	01		CO1,L4
	Review	**Signature of the HOD/Coordinator**						

	SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY LESSON PLAN (Regulation :R22) Department of AIDS	Prepared on Rev1: Page: 11 of 7
	Sub. Code & Title	**R22CSE2102 Computer Organization and Architecture**
	Academic Year: 2025-26	**Year/Sem./Section** **II-I**
	Faculty Name & Designation	**D.JYOTHI, Assistant Professor**

Unit/ Item No.	Topic (s)	Book Reference	Page (s) From	Page (s) To	Teaching Methodology	Proposed No. of Periods	Actual Date of Handled	CO/RBT
	UNIT-II							
2	**Microprogrammed Control, Central Processing unit**					**10**		
2.1	Microprogrammed Control: Control memory	T1	235	238	Black board	01		CO2,L1
2.2	Address sequencing	T1	238	16	Black board	01		CO2,L2
2.3	Micro program example	T1	242	4	Black board	01		CO2,L1
2.4	Design of control unit.	T1	253	112	Black board	01		CO2,L2
2.5	Central Processing Unit: General Register Organization,	T1	265	115	Black board	01		CO2,L1
2.6	** Stack Organization	T1	270	119	Black board	01		CO2,L2
2.7	Instruction Formats: Three Address Instructions, Two Address Instructions	T1	278	130	Black board	01		CO2,L3
2.8	Addressing modes	T1	283	133	Black board	01		CO2,L4
2.9	Data Transfer and Manipulation	T1	289	135	Black board	01		CO2,L1
2.10	Program Control.	T1	295	144	Black board	01		CO2,L1
	Review	**Signature of the HOD/Coordinator**						

	SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY LESSON PLAN (Regulation :R22) Department of AIDS	Prepared on Rev1: Page: 12 of 7
	Sub. Code & Title	**R22CSE2114 Computer Organization and Architecture**
	Academic Year: 2025-26	**Year/Sem./Section** **II-I**
	Faculty Name & Designation	**D.JYOTHI, Assistant Professor**

Unit/ Item No.	Topic (s)	Book Reference	Page (s) From	Page (s) To	Teaching Methodology	Proposed No. of Periods	Actual Date of Handled	CO/RBT
	UNIT-III							
3	**Data Representation, Computer Arithmetic**					**09**		
3.1	**Data Representation:** Data types	T1	81	87	Black board	02		CO3,L2
3.2	Complements (r-1)'s Complement and (r's Complement)	T1	89	90	Black board	01		CO3,L3
3.3	Fixed Point Representation,	T1	91	95	Black board	01		CO3,L1
3.4	Floating Point Representation.	T1	97	97	Black board	01		CO3,L1
3.5	Computer Arithmetic: Addition and subtraction	T1	365	370	Black board	02		CO3,L3
3.6	Division Algorithms	T1	372	377	Black board	01		CO3,L3
3.7	Multiplication Algorithms	T1	372	377	Black board	01		CO3,L3
3.8	Floating – point Arithmetic operations.	T1	385	393	Black board	01		CO3,L3
3.9	Decimal Arithmetic unit	T1	395	398	Black board	01		CO3,L3
	Review	**Signature of the HOD/Coordinator**						

	SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY LESSON PLAN (Regulation :R22) Department of AIDS	Prepared on Rev1: Page: 13 of 7
	Sub. Code & Title	**R22CSE2114 Computer Organization and Architecture**
	Academic Year: 2025-26	**Year/Sem./Section** **II-I**
	Faculty Name & Designation	**D.JYOTHI, Assistant Professor**

Unit/ Item No.	Topic (s)	Book Reference	Page (s) From	Page (s) To	Teaching Methodology	Proposed No. of Periods	Actual Date of Handled	CO/RBT
	UNIT-IV							
4	**Input Output Organization, Memory Organization**					**09**		
4.1	Input-Output Organization: Input-Output Interface	T1	413	421	Black board	01		CO4,L2
4.2	Asynchronous data transfer	T1	422	431	Black board	01		CO4,L1
4.3	Modes of Transfer	T1	433	437	Black board	01		CO4,L2
4.4	Priority Interrupt	T1	437	445	Black board	01		CO4,L1
4.5	Direct memory Access.	T1	446	448	Black board	01		CO4,L6
4.6	Discuss Memory Hierarchy, Main Memory	T1	479	490	Black board	01		CO4,L2
4.7	Auxiliary memory	T1	493	495	Black board	01		CO4,L1
4.8	Associate Memory	T1	495	500	Black board	01		CO4,L1
4.9	Cache Memory	T1	500	508	Black board	01		CO4,L1
	Review	**Signature of the HOD/Coordinator**						

	SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY LESSON PLAN (Regulation :R22) Department of AIDS	Prepared on Rev1: Page: 14 of 7
	Sub. Code & Title	**R22CSE2114 Computer Organization and Architecture**
	Academic Year: 2025-26	**Year/Sem./Section** **II-I**
	Faculty Name & Designation	**D.JYOTHI , Associate Professor**

Unit/ Item No.	Topic (s)	Book Reference	Page (s) From	Page (s) To	Teaching Methodology	Proposed No. of Periods	Actual Date of Handled	CO/RBT
	UNIT-V							
5	Reduced Instruction Set Computer, Pipeline and Vector Processing ,Multiprocessors					**14**		
5.1	**Reduced Instruction Set Computer:** CISC Characteristics,	T1,	304	305	Black board	01		CO5,L2
5.2	RISC Characteristics.	T1,	306	312	Black Board	01		CO5,L2
5.3	Pipeline & Vector Processing	T1,	323	328	Black board	01		CO5,L1
5.4	Parallel Processing,	T1,	323	328	Black board	01		CO5,L1
5.5	Pipelining, Arithmetic Pipeline,	T1,	329	336	Black board	01		CO5,L1
5.6	Instruction Pipeline,	T1,	337	343	Black board	01		CO5,L1
5.7	RISC Pipeline,	T1,	343	348	Black board	01		CO5,L1
5.8	Vector Processing,	T1,	348	354	Black board	01		CO5,L1
5.9	Array Processor	T1,	354	356	Black board	01		CO5,L2
5.10	Multi Processors: Characteristics of Multiprocessors,	T1,	529	531	Black board	01		CO6,L2
5.11	Interconnection Structures,	T1,	531	539	Black board	01		CO6,L5
5.12	Inter - Processor arbitration,	T1,	539	544	Black board	01		CO6,L1
5.13	Inter - Processor communication and synchronization,	T1,	545	548	Black board	01		CO6,L1
5.14	Cache Coherence.	T1,	550	553	Black board	01		CO6,L2
	Review	**Signature of the HOD/Coordinator**						

TEXT BOOKS:

T1. Computer System Architecture – M. Moris Mano, Third Edition, Pearson/PHI.

REFERENCE BOOKS:

R1. Computer Organization – Car Hamacher, Zvonks Vranesic, Safea Zaky, Vth Edition,McGraw Hill

R2. Computer Organization and Architecture – William Stallings Sixth Edition, Pearson/PHI.

R3. Structured Computer Organization – Andrew S. Tanenbaum, 4th Edition, PHI/Pearson.

WEB LINKS: **https://onlinecourses.nptel.ac.in/noc21_cs61/previewASSIGNMENT**

S.No.	Assignment Questions	Course Outcome	Books To be Referred
1	How to do address sequencing with diagram. (Understand)	CO1	T1
2.	What is instruction format? Explain the different instruction formats in detail.(Understand)	CO1	T1
3.	Explain the different phases of Instruction Cycle?(Understand)	CO1	T1
4.	Explain the Micro Program Control with Diagram &Examples?(Understand)	CO1	T1
5.	List out any 5 Registers with explains in detail. (Remember)	CO1	T1
6.	Explain general register organization in detail with neat diagrams(Understand)	CO2	T1
7.	Explain Stack organization in detailwith neat diagrams(Understand)	CO2	T1
8.	Evaluate the following program using three address Instruction format X = (A+B) * (C+D)	CO2	T1
9.	Evaluate the following program using two address Instruction format X = (A+B) *(C+D)	CO2	T1
10.	Evaluate the following program using one address Instruction format X = (A+B) * (C+D)	CO2	T1

	SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY Question Bank (Regulation :R22) Department of AIDS	Prepared on Rev1: Page: 16 of 7
	Sub. Code & Title	**R22CSE2114 Computer Organization and Architecture**
	Academic Year: 2025-26	**Year/Sem./Section** **II-I**
	Faculty Name & Designation	**D.JYOTHI, Assistant Professor**

UNIT -1
Digital Computers

	1 MARK Questions L1-Remember L2-Understand L3-Apply L4-Analyze L5-Evaluate L6-Create	BT LEVEL	COURSE OUTCOME
1.	Define Computer Architecture. (Remember)	L1	CO1
2.	Define a Digital Computer. Draw block diagram of Computer. (Remember)	L1	CO1
3.	What is the need of Register? Write the different types of Registers?(Remember)	L1, L2	CO1
4.	Define Computer Design. (Remember)	L1	CO1
5.	Define Computer Organization. (Remember)	L1	CO1
6.	List the various representation of Register. (Remember)	L1	CO1
7.	What are the types of Memory Transfer? (Remember)	L1	CO1
8	Define Micro operation. (Remember)	L1	CO1
9	List the types of micro operation. (Remember)	L1	CO1
10.	Draw the circuit of Four Bit Binary Adder. (Remember)	L1	CO1
11.	Define Instruction code, Operation code and Accumulator. (Remember)	L1	CO1
12.	Define Instruction Cycle. (Remember)	L1	CO1
13.	List Computer Registers. (Remember)	L1	CO1
14.	Discuss Timing and Control Unit.(Understand)	L2	CO1
15.	What is instruction format and its types? (Remember)	L1	CO1
	10 MARKS Questions		
1.	With the help of a block schematic explain the basic organizational units of a Digital computer. (Understand)	L2	CO1
2.	How to construct an ALU, which perform basic arithmetic and logic operations? (Create)	L6	CO1
3.	Explain the stored program organization with neat diagram. (Understand)	L2	CO1
`	Detail the process involved in Register Transfer Language. (Understand)	L2	CO1
5.	Demonstrate the following. (Apply) 1. Bus and Memory Transfer 2. Three – State Bus Buffer with neat diagram	L3	CO1
6.	Illustrate the Direct and Indirect addressing of basic computer. (Analyze)	L4	CO1
7.	List out any 5 Registers with explains in detail. (Remember, Understand)	L1, L2	CO1

8.	Explain in Detail about Common Bus System for basic computer register. (Understand)	L2	CO1
9.	Explain the different instruction formats in detail. (Understand)	L2	CO1
10.	Draw and Explain the Control unit and Timing Diagram of Basic Computer? (Understand)	L2	CO1
11.	Explain the different phases of Instruction Cycle? (Understand)	L2	CO1
12.	Draw the flowchart for interrupt cycle and experiment with it with explanation (Remember)	L1	CO1
13.	Determine the input-output configuration. (Apply)	L3	CO1

	Unit -II **Micro programmed Control,** **Central Processing Unit**		
	1 MARK QUESTIONS		
1.	What is meant by Hardwired Control Unit? (Remember)	L1	CO2
2.	What is meant by Micro programmed control unit? (Remember)	L1	CO2
3.	Discuss the use of Dynamic microprogramming. (Understand)	L2	CO2
4.	Define Micro operations. (Remember)	L1	CO2
5.	Discuss the principle operation of micro programmed control unit. (Understand)	L2	CO2
6.	What is control memory? (Remember)	L1	CO2
7.	State the function of Micro instruction. (Remember)	L1	CO2
8.	What is Micro program, Microcode? (Remember)	L1	CO2
9.	Write example micro programs. (Understand)	L2	CO2
10.	Define control unit. (Remember)	L1	CO2
11.	Define Program Control. (Remember)	L1	CO2
12.	State the process involved in Mapping from instruction code to microinstruction address with example. (Remember)	L1	CO2
13.	Draw the microinstruction format for the control memory. (Understand)	L2	CO2
14.	What is processor unit & control unit of CPU? (Remember)	L1	CO2
15.	Identify the sub cycles in Basic instruction cycle. (Remember)	L1	CO2
16.	Draw the Instruction format with mode field. (Understand)	L2	CO2
17.	List the various types of CPU organizations. (Remember)	L1	CO2
18.	List the types of address instructions of several different lengths. (Remember)	L1	CO2
19.	Write the most commonly used addressing modes. (Remember)	L1	CO2
20.	What is Data Transfer Manipulation? Write the typical instructions used for data transfer? (Remember)	L1	CO2
	10 MARK QUESTIONS		
1	Draw and explain about Micro program Control Organization**.** (Understand**)**	L2	CO2
2.	Explain in detail about the Address Sequencing process in Micro program control unit. (Understand)	L2	CO2
3.	Write short notes on (Remember) (i) Micro instruction format **(ii)** Symbolic micro instruction.	L1	CO2
4.	Explain general register organization in detail with neat diagrams. (Understand)	L2	CO2
5.	To illustrate the influence of the number of address on computer programs, we will evaluate the arithmetic statement X=(A+B)*(C+D) using three address Instruction format. (Apply)	L3	CO2
6.	To illustrate the influence of the number of address on computer programs, we will	L3	CO2

	evaluate the arithmetic statement X=(A+B)*(C+D) using two address Instruction format. (Apply)		
7.	To illustrate the influence of the number of address on computer programs, we will evaluate the arithmetic statement X=(A+B)*(C+D) using one address Instruction format. (Apply)	L3	CO2
8	Explain in detail about various addressing modes. (Understand)	L2	CO2
9.	Explain the operations done through Data Transfer and Manipulation. (Understand)	L2	CO2
10.	Describe detail about Program control unit. (Understand)	L2	CO2

Unit -III : Data Representation, Computer Arithmetic			
1 MARK QUESTIONS			
1.	What is mean by data representation? (Remember)	L1	CO3
2	Draw the typical internal data representation types? (Understand)	L2	CO3
3	Convert the following decimal number to the base indicated 7562 to octal 1938 to hexadecimal? (Apply)	L3	CO3
4.	Find the 1's and 2's complement of the following eight-digit binary number a. 10101110 b. 10000001? (Remember)	L1	CO3
5.	Write 3 ways of representing negative fixed point binary numbers in addition and subtraction. (Remember)	L1	CO3
6.	Draw flow chart for add and subtract operations. (Understand)	L2	CO3
7.	List the steps of Booth's Multiplication algorithm? (Remember)	L1	CO3
8.	Convert the following decimal number to the base indicated 17562 to octal 11938 to hexadecimal. (Apply)	L3	CO4
9.	Define decimal arithmetic unit. (Remember)	L1	CO4
10.	List out computer arithmetic operations. (Remember)	L1	CO4
11.	Design division algorithm.(Create)	L6	CO4
12.	Write about floating point arithmetic. (Remember)	L1	CO4
13.	Define BCD adder and Sub-tractor. (Remember)	L1	CO4
10 MARKS QUESTIONS			
1.	Draw and explain the hardware for signed – magnitude addition and subtraction. (Understand)	L2	CO3
2.	Explain in detail about addition and subtraction with signed 2's complement data. (Understand)	L2	CO3
3.	Explain the booth's multiplication algorithm with neat sketch of hardware design. (Understand)	L2	CO3

4.	Perform division process of fixed point binary number in signed-magnitude representation 10001 and 01110 using restoring division algorithm. (Apply)	L3	CO4
5.	Explain in detail about floating point arithmetic operations.	L2	CO4
6.	Draw a flowchart for adding and subtracting two fixed point binary numbers where negative numbers are signed 1's complement presentation. (Understand)	L2	CO4
7.	Draw the flowchart for divide operation and explain. (Understand)	L2	CO4
8.	Draw and explain the one stage decimal arithmetic unit. (Understand)	L2	CO4
9.	Explain in detail about the derivation of BCD adder. (Understand)	L2	CO4

Unit-IV : Input Output Organization, Memory Organization			
1 MARK QUESTIONS			
1	What is the need of IO Interface.? (Remember)	L1	CO5
2	What is DMA? (Remember)	L1	CO5
3.	Define Priority Interrupt. (Remember)	L1	CO5
4.	List out any 5 IO Devices. (Remember)	L1	CO5
5.	What are peripheral devices? Give a note on video monitors. (Remember)	L1	CO5
6.	Discuss Asynchronous Data. (Understand)	L2	CO5
7	What are the three possible modes of data transfer? (Remember)	L1	CO5
8	List out the memory hierarchy. (Remember)	L1	CO5
9	What is IoP? (Remember)	L1	CO5
10	What is mean by memory management system? (Remember)	L1	CO5
11	Define main memory. (Remember)	L1	CO5
12	Define auxiliary memory. (Remember)	L1	CO5
13	Define associate memory. (Remember)	L1	CO5
14	Draw block diagram of associate memory. (Understand)	L2	CO5
15	What are the three types of mapping procedures in cache memory? (Remember)	L1	CO5
10 MARKS QUESTIONS			
1	Explain in detail about Input and output interface with example. (Understand)	L2	CO5
2	What is asynchronous data transfer? Explain the different types of Asynchronous data transfer techniques. (Remember) (Understand)	L1, L2	CO5
3	Explain the following data transfer modes/techniques. (Understand) a) Program Controlled IO b) Interrupt Initiated IO c) Direct memory access (DMA)	L2	CO5
4	Explain the communication between IOP and CPU. (Understand)	L2	CO5
5	Explain in detail about DMA operation with neat diagram. (Understand)	L2	CO5
6	Write a note on memory hierarchy with the neat diagram. (Remember)	L1	CO5
7	Explain with neat sketch auxiliary memory. (Understand)	L2	CO5
8	Explain in detail about associative memory mechanisms. (Understand)	L2	CO5
9	Explain in detail about Cache memory mechanisms. (Understand)	L2	CO5
10	Describe in brief the different modes by which data transfer can take place between a computer unit and its I/O devices. What is the difference between synchronous and asynchronous data transfer? (Understand) (Evaluate)	L2, L5	CO5

Unit-V: Reduced Instruction Set Computer Pipeline &Vector Processing ,Multiprocessors			
1 MARK QUESTIONS			
1.	Define RISC & CISC. (Remember)	L1	CO6
2	Discuss the difference between RISC & CISC. (Evaluate)	L5	CO6
3	Define a Pipeline. Give an example. (Remember)	L1	CO6
4	Define arithmetic pipeline. (Remember)	L1	CO6
5	What is mean by instruction pipeline? (Remember)	L1	CO6
6	Mention the instruction cycle of instruction pipeline. (Remember)	L1	CO6
7	Define RISC pipeline. (Remember)	L1	CO6
8	List out pipelining types. (Remember)	L1	CO6
9	Define Vector Processing. (Remember)	L1	CO6
10	Define multiprocessor. (Remember)	L1	CO6
10 MARKS QUESTIONS			
1	Explain in detail about the RISC Characteristics. (Understand)	L2	CO6
2	Explain in detail about the CISC Characteristics (Understand)	L2	CO6
3	Explain the different types of Pipeline techniques. (Understand)	L2	CO6
4	Explain in detail about the Instruction Pipeline. (Understand)	L2	CO6
5	Explain in detail about basic multiprocessor architecture. (Understand)	L2	CO6
6	List the Characteristics of Multiprocessors. Explain in detail about the Interconnection structures of Multiprocessor. (Remember) (Understand)	L1, L2	CO6
7	Explain in detail about the Inter processor arbitration. (Understand)	L2	CO6
8	Describe in detail about inter process communication and synchronization.	L2	CO6

MID QUESTION PAPERS

&

END SEMESTER QUESTION PAPERS

BR-20 **SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY** **D4**

IIB.Tech - I Semester - II Mid Term Examination, February – 2022

(R20CSE2102) COMPUTER ORGANIZATION and ARCHITECTURE

(For CSE, CS, AIML, DS, CSIT and IT)

Duration: 90 Mins **Dt: 15-02-2022, Day-2 (AN)** **Max Marks: 25M**

Section – A

Answer *All* the questions **Marks: 5Qx1M = 5M**

* (L1-Remembering, L2-Understanding, L3-Applying, L4-Analyzing, L5-Evaluating, and L6-Creating.)	*Blooms Taxonomy Levels	Course Outcomes
1. Explain floating point arithmetic.	(L2)	CO3
2. Discuss Asynchronous Data.	(L2)	CO4
3. Explain Main Memory.	(L2)	CO3
4. Define a Pipeline. Give an example.	(L2)	CO4
5. Define RISC & CISC.	(L1)	CO6

Section – B

Answer any *FOUR* questions **Marks: 4Qx5M = 20M**

6. Draw the flowchart for divide operation and explain.	(L2)	CO3
7. Explain the following data transfer modes/techniques. a)Program Controlled IO. b)Interrupt Initiated IO.	(L2)	CO4
8. Write a note on memory hierarchy with the neat diagram.	(L2)	CO3
9. Explain in detail about Associative memory mechanisms.	(L2)	CO3
10. Explain in detail about the RISC Characteristics.	(L2)	CO6
11. What is Multiprocessors? Explain in detail.	(L1)	CO6

BR-20 **SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY** **D4**

(An Autonomous Institution Under 2(f) and 12(B) of UGC Act 1956, New Delhi)

II B.Tech - I Semester - I Mid Term Examinations (Model paper)

(R18CSE2102) COMPUTER ORGANIZATION & ARCHITECTURE - (Common to CSE & IT)

Duration: 90Mins **Max Marks: 25M**

Section – A

Answer *All* the questions **5Qx1M = 5M**

1) Define Computer Architecture.
2) Explain data representation?
3) What is control memory**?**
4) Define control unit.
5) Find the 1's and 2's complement of the following eight digit binary number.
   a. 10101110
   b. 10000001

Section – B

Answer any *FOUR* questions **4Qx5M = 20M**

1) Explain about Von Neumann architecture**?**
2) Draw the flowchart for interrupt cycle and experiment with it with explanation**?**
3) Evaluate the following program using three address Instruction format
   X = (A+B) * (C+D)?
4) Explain multiple bus organization in detail?
5) Explain the booth's algorithm with neat sketch of hardware design**?**

BR-20 **SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY** **D4**

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II B.Tech - I Semester - II Mid Term Examinations (Model paper)

(R18CSE2102) COMPUTER ORGANIZATION & ARCHITECTURE - (Common to CSE & IT)

Duration: 90Mins **Max Marks: 25M**

Section – A

Answer *All* the questions **5Qx1M = 5M**

1. List out the steps of Booth's algorithm**.**
2. Define Priority Interrupt**.**
3. Define Cache Memory, Auxilary Memory, Associate Memory**.**
4. Differentiate between the RISC & CISC**?**
5. Explain Vector Processing?

Section – B

Answer any *FOUR* questions **4Qx5M = 20M**

1. Explain about Von Neumann architecture**?**
2. Evaluate the following program using one address Instruction format
   X = (A+B) * (C+D)?
3. Describe in brief the different modes by which data transfer can take place between a computer unit and its I/O devices. What is the difference between synchronous and asynchronous data transfer**?**
4. Explain the different types of Pipeline techniques**?**
5. Write the Characteristics of Multiprocessors. Explain in detail about the Interconnection structures of Multiprocessor**?**

Subject Code: R20CSE2102

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)Recognized under 2(f) and 12(B) of UGC Act 1956

II B.Tech - I Semester –End Examinations (Model paper)

COMPUTER ORGANIZATION & ARCHITECTURE- (Common to CSE &IT)

Duration: 3 Hrs **Max Marks: 70M**

Section – A

Answer *All* the following questions **Marks: 5Qx4M = 20M**

1. Define Computer Architecture.
2. What is Floating Point Representation?
3. Find the 1's and 2's complement of the following eight digit binary number?
   a. 10101110
   b. 10000001
4. Explain Modes of transfer**?**
5. Differentiate between the RISC & CISC**?**

Section – B

Answer any *FIVE* questions choosing at least one from each Unit

Marks: 5Qx10M = 50M

UNIT - I

6. Explain the stored program organization with neat diagram?

(OR)

7. Draw the flowchart for interrupt cycle and experiment with it with explanation**?**

UNIT - II

8. Evaluate the following program using one address Instruction format
   X = (A+B) * (C+D)?

(OR)

9. Draw and explain typical hardware control unit?

UNIT - III

10. Perform division of 1000 and 0011 using restoring division algorithm**?**

(OR)

11. Explain floating point arithmetic**?**

UNIT - IV

12. Describe in brief the different modes by which data transfer can take place between a computer unit and its I/O devices. What is the difference between synchronous and asynchronous data transfer**?**

(OR)

13. Write a note on memory hierarchy with the neat diagram?

UNIT - V

14. Write the Characteristics of Multiprocessors. Explain in detail about the Interconnection structures of Multiprocessor**?**

(OR)

15. Explain the different types of Pipeline techniques**?**