



Sri Indu

College of Engineering & Technology

UGC Autonomous Institution

Recognized under 2(f) & 12(B) of UGC Act 1956,
NAAC, Approved by AICTE &
Permanently Affiliated to JNTUH



NAAC
NATIONAL ASSESSMENT AND
ACCREDITATION COUNCIL



HANDOUT

II Year I Semester
(R22CSE2114)

Computer Organization & Architecture

DEPARTMENT OF COMPUTER SCIENCE AND
ENGINEERING(AIML)

ACADEMIC YEAR 2025-2026



SRIINDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

(Permanently Affiliated to JNTUH, Approved by AICTE, New Delhi and Accredited by NBA, NAAC)
Sheriguda Village, Ibrahimpatnam Mandal, Ranga Reddy Dist. – 501 510

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING (AIML)

HANDOUT- INDEX

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SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

VISION OF THE INSTITUTE

To be a premier institution in engineering & technology and management for competency, values and social consciousness.

MISSION OF THE INSTITUTE

- IM₁:** Provide high quality academic programs, training activities and research facilities.
- IM₂:** Promote continuous industry-institute interaction aimed at promoting employability, entrepreneurship, leadership and research aptitude among stakeholders.
- IM₃:** Contribute to the economic and technological development of the region, state and nation.

VISION OF THE DEPARTMENT

To be a technologically adaptive centre for computing by grooming the students as top notch professionals.

MISSION OF THE DEPARTMENT

The Department has following Missions:

- DM1:** To offer quality education in computing.
- DM2:** To provide an environment that enables overall development of all the stakeholders.
- DM3:** To impart training on emerging technologies.
- DM4:** To encourage participation of stakeholders in research and development

Program Educational Objectives(PEO's)

PEO1	Higher Studies: Graduate with an ability to pursue higher studies and get employment in reputed institutions and organizations.
PEO2	Domain Knowledge: Graduate with an ability to design and develop a product.
PEO3	Professional Career: Graduate with excellence by multidisciplinary approach to achieve successful professional career.
PEO4	Life Long Learning: Graduate with an ability to learn advanced skills to face professional competence through lifelong learning

Program Specific Outcomes(PSO's)

PSO1	To Develop software projects using standard practices and suitable programming environment.
PSO2	To identify, formulate and solve the real life problems faced in the society, industry and other areas by applying the skills of the programming languages, networks and databases learned.
PSO3	To apply computer science knowledge in exploring and adopting latest technologies in various inter- disciplinary research activities.

Program Outcomes(PO's)

PO1	Engineering Knowledge: Apply knowledge of mathematics, natural science, computing, engineering fundamentals and an engineering specialization as specified in WK1 to WK4 respectively to develop to the solution of complex engineering problems.
PO2	Problem Analysis: Identify, formulate, review research literature and analyze complex engineering problems reaching substantiated conclusions with consideration for sustainable development. (WK1 to WK4)
PO3	Design/Development of Solutions: Design creative solutions for complex engineering problems and design/develop systems/components/processes to meet identified needs with consideration for the public health and safety, whole-life cost, net zero carbon, culture, society and environment as required. (WK5)
PO4	Conduct Investigations of Complex Problems: Conduct investigations of complex engineering problems using research-based knowledge including design of experiments, modelling, analysis & interpretation of data to provide valid conclusions. (WK8)..
PO5	Engineering Tool Usage: Create, select and apply appropriate techniques, resources and modern engineering & IT tools, including prediction and modelling recognizing their limitations to solve complex engineering problems. (WK2 and WK6)
PO6	The Engineer and The World: Analyze and evaluate societal and environmental aspects while solving complex engineering problems for its impact on sustainability with reference to economy, health, safety, legal framework, culture and environment. (WK1, WK5, and WK7).
PO7	Ethics: Apply ethical principles and commit to professional ethics, human values, diversity and inclusion; adhere to national & international laws. (WK9)
PO8	Individual and Collaborative Team work: Function effectively as an individual, and as a member or leader in diverse/multi-disciplinary teams.
PO9	Communication: Communicate effectively and inclusively within the engineering community and society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations considering cultural, language, and learning differences
PO10	Project Management and Finance: Apply knowledge and understanding of engineering management principles and economic decision-making and apply these to one's own work, as a member and leader in a team, and to manage projects and in multidisciplinary environments.
PO11	Life-Long Learning: Recognize the need for, and have the preparation and ability for i) independent and life-long learning ii) adaptability to new and emerging technologies and iii) critical thinking in the broadest context of technological change. (WK8)

COURSE OUTCOMES (CO's)

Academic Year: 2025-26

Class: II YEAR-I SEM.

Course Name: COMPUTER ORGANIZATION AND ARCHITECTURE (R22CSE2114)

At the end of the course, the student will be able to

Course Outcomes (COs)	
C212.1	Understand the basics of instructions sets and their impact on processor design
C212.2	Demonstrate an understanding of the design of the functional units of a digital computer system
C212.3	Evaluate cost performance and design trade-offs in designing and constructing a computer processor Including memory
C212.4	Design a pipeline for consistent execution of instructions with minimum hazards
C212.5	Recognize and manipulate representations of numbers stored in digital computers.
C212.6	Demonstrate the Characteristics of Multiprocessors.

COURSE ARTICULATION MATRIX

COs	POs												PSOs		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C2102.1	3	2	-	-	3	-	2	-	-	-	-	2	2	3	2
C2102.2	3	3	-	2	2	-	-	-	-	-	-	-	3	3	2
C2102.3	3	3	-	2	2	-	2	-	-	-	-	-	3	3	2
C2102.4	3	2	3	2	-	-	2	-	-	-	-	-	3	2	1
C2102.5	3	3	3	3	2	-	-	-	3	-	-	-	3	3	1
C2102.6	3	3	3	3	-	-	2	-	3	-	-	-	3	3	1
C2102	3	2.6	3	2.6	2.2	-	2	-	3	-	-	2	2.8	2.8	1.5

3: High 2: Medium 1: Low



Lr.No.SICET/AUTO/DAE/II- B.Tech Academic Calendar/30/2025

B.TECH II-YEAR I-SEM & II-SEM ACADEMIC CALENDAR
(FOR ACADEMIC YEAR : 2025-26)

Academic Calendar for B.Tech – IInd Year Students (2024 - 25 Batch), BR-22 Regulation.

I – Semester

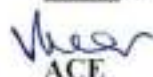
S.No.	EVENT	PERIOD	DURATION
1.	Commencement of class work.	01.08.2025 (Monday)	
2.	1 st Spell of Instructions for covering First Two and a half Units.	01.08.2025 – 07.10.2025	9 Weeks
3.	I Mid Term Examinations.	08.10.2025 – 10.10.2025	3 Days
4.	Submission of I Mid Term Examination Marks.	16.10.2025	
5.	2 nd Spell of Instructions for Remaining Two and a half Units.	13.10.2025 – 13.12.2025	9 Weeks
6.	II Mid Term Examinations.	15.12.2025 – 17.12.2025	3 Days
7.	Preparation Holidays and Practical Examinations	18.12.2025 – 27.12.2025	1 Week
8.	Submission of II Mid Term Examination Marks.	23.12.2025	
9.	I Semester End Examinations.	29.12.2025 – 10.01.2026	2 Weeks
Commencement of Class-Work for II B.Tech - II Semester 19.01.2026			

Note: No of Working/instructional days : 92

II – Semester

S.No.	EVENT	PERIOD	DURATION
1.	Commencement of class work.	19.01.2026 (Monday)	
2.	1 st Spell of Instructions for covering First Two and a half Units.	19.01.2026 – 14.03.2026	8 Weeks
3.	I Mid Term Examinations.	16.03.2026 – 18.03.2026	3 Days
4.	Submission of I Mid Term Examination Marks.	24.03.2026	
5.	2 nd Spell of Instructions for Remaining Two and a half Units.	20.03.2026 – 09.05.2026	7 Weeks
6.	Continuation of remaining 2 nd Spell of Instructions	25.05.2026 – 10.06.2026	4 Weeks
7.	II Mid Term Examinations.	11.06.2026 – 13.06.2026	3 Days
8.	Preparation Holidays and Project Evaluation.	15.06.2026 – 20.06.2026	1 Week
9.	Submission of II Mid Term Examination Marks.	18.06.2026	
10.	II Semester End Examinations	22.06.2026 – 04.07.2026	2 Weeks

Note: No of Working/instructional days : 92


ACE


CE


DIRECTOR


PRINCIPAL

Controller of Examination
Sri Indu College of Engineering & Technology
(An Autonomous Institution Under UGC)
Sheriguda (V), Ibrahimpatnam, R.R. Dist-501510

DIRECTOR
Sri Indu College of Engineering & Technology
(An Autonomous Institution Under UGC)
Sheriguda (V), Ibrahimpatnam, R.R. Dist-501510

PRINCIPAL
Sri Indu College of Engineering & Technology
(An Autonomous Institution Under UGC)
Sheriguda (V), Ibrahimpatnam, R.R. Dist-501510.

Sign: 

Dr. M.V.S.S. Giridhar

Prof. of CEA; JNTUH Nominee

Sign: 

Dr. T. Venu Gopal

Prof. of CSE; JNTUH Nominee

Sign: 

Dr. D. Ramesh

Prof. of CSE; JNTUH Nominee

(Copy to DAP&E and Copy to all the Dept. Heads)

TUESDAY	1	DEPARTMENT MEETING FOR IV-I & III-I 2025-2026		2	IV-I MID I EXAMS		OCTOBER		2	IV-I END EXAMS			
WEDNESDAY	2			3	IV-I MID I EXAMS	1	III-I CRT CLASSES		3	IV-I END EXAMS		JANUARY	
THURSDAY	3		AUGUST	4	IV-I SPELL 2 CLASSES	2	GANDHI JAYANTI & DASHA RA		4	IV-I END EXAMS	1	II-I & III-I END EXAMS	
FRIDAY	4		II-I SPELL I CLASSES COMMENCEMENT	5		3	III-I CRT CLASSES		5	IV-I END EXAMS	2	II-I & III-I END EXAMS	
SATURDAY	5		DEPARTMENT MEETING	6		4	III-I CRT CLASSES	1	WOKSHOP UNDER AI CLUB	6	IV-I END EXAMS	3	II-I & III-I END EXAMS
SUNDAY	6			7		5		2		7		4	
MONDAY	7	IV-I SPELL I CLASSES COMMENCEMENT		8		6	III-I CRT CLASSES	3		8	IV-I END EXAMS	5	II-I & III-I END EXAMS
TUESDAY	8			9		7	III-I CRT CLASSES	4		9	IV-I END EXAMS	6	II-I & III-I END EXAMS
WEDNESDAY	9			10	IV-I MID I EXAMS SUBMISSION	8	III-I MID I EXAMS & II-I MID I EXAMS	5		10	IV-I END EXAMS	7	II-I & III-I END EXAMS
THURSDAY	10			11		9	III-I MID I EXAMS & II-I MID I EXAMS	6		11	IV-I END EXAMS	8	II-I & III-I END EXAMS
FRIDAY	11			12	DEPARTMENT MEETING REVIEW ON IV-I SLOW LEARNERS	10	III-I MID I EXAMS & II-I MID I EXAMS	7		12	IV-I END EXAMS	9	II-I & III-I END EXAMS
SATURDAY	12	AI CLUB MEETING	WOKSHOP UNDER AI CLUB	13	AI CLUB MEETING	11		8		13	IV-I END EXAMS	10	II-I & III-I END EXAMS
SUNDAY	13			14		12		9		14		11	
MONDAY	14	III-I SPELL I CLASSES COMMENCEMENT		15	III-I CRT CLASSES	13	II-I & III-I SPELL 2 CLASSES	10		15	II-I & III-I MID II EXAMS	12	
TUESDAY	15			16	III-I CRT CLASSES	14		11		16	II-I & III-I MID II EXAMS	13	
WEDNESDAY	16			17	III-I CRT CLASSES	15		12		17	II-I & III-I MID II EXAMS	14	
THURSDAY	17			18	III-I CRT CLASSES	16	II-I & III-I MID I EMARKS SUBMISSION	13		18	II-I & III-I PREPARATION & PRACTICAL EXAMS	15	
FRIDAY	18		INDEPENDENCE DAY	19	III-I CRT CLASSES	17	DEPARTMENT MEETING REVIEW ON III-I & II-I SLOW LEARNERS	14		19	II-I & III-I PREPARATION & PRACTICAL EXAMS	16	
SATURDAY	19			20	III-I CRT CLASSES	18	AI CLUB MEETING	15		20	II-I & III-I PREPARATION & PRACTICAL EXAMS	17	
SUNDAY	20			21	BATHUKAMMA	19		16		21		18	
MONDAY	21	BONALU HOLIDAY		22	III-I CRT CLASSES	20	DIWALI	17		22	II-I & III-I PREPARATION & PRACTICAL EXAMS	19	
TUESDAY	22			23	III-I CRT CLASSES	21		18		23	II-I & III-I MID II MARKS SUBMISSION III-I PREPARATION & PRACTICAL EXAMS	20	

WEDNESDAY	23			24	III-I CRT CLASSESS	22		19	IV-I MID II EXAMS	24	II-I & III-I PREPARATION & PRACTICAL EXAMS	21	
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THURSDAY	24		21		25	III-I CRT CLASSESS	23		20	IV-I MID II EXAMS	25	CHRISTMAS DAY	22	
FRIDAY	25		22		26	III-I CRT CLASSESS	24		21	IV-I MID II EXAMS	26	II-I & III-I PREPARATIO N & PRACTICAL EXAMS	23	
SATURDAY	26		23		27	GANESH CHATURTHI	25	DEPARTMEN T MEETING	22	AI CLUB MEETIN G	27	II-I & III-I PREPARATIO N & PRACTICAL EXAMS	24	
SUNDAY	27		24		28		26		23		28		25	
MONDAY	28	DEPARTMENT MEETING FOR II YR 2025-2026	25		29	III-I CRT CLASSESS	27		24	IV-I PREPARATION & PRACTICAL EXAMS	29	II-I & III-I END EXAMS	26	
TUESDAY	29		26		30	III-I CRT CLASSESS	28		25	IV-I PREPARATION & PRACTICAL EXAMS	30	II-I & III-I END EXAMS	27	
WEDNESDAY	30		27				29		26	IV-I PREPARATION & PRACTICAL EXAMS	31	II-I & III-I END EXAMS	28	
THURSDAY	31		28				30		27	IV-I PREPARATION & PRACTICAL EXAMS			29	
FRIDAY			29				31		28	IV-I PREPARATION & PRACTICAL EXAMS			30	
SATURDAY			30	AI CLUB MEETING		WOKSHOP UNDER AI CLUB			29	IV-I PREPARATION & PRACTICAL EXAMS			31	
SUNDAY			31						30					

**COMPUTER ORGANIZATION
&
ARCHITECTURE
SYLLABUS**

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)

B.Tech. - II Year – I Semester

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3	0	0	3

(R22CSE2114) COMPUTER ORGANIZATION AND ARCHITECTURE

Course Objectives

- The purpose of the course is to introduce principles of computer organization and the basic architectural concepts.
- It begins with basic organization, design, and programming of a simple digital computer and introduces simple register transfer language to specify various computer operations.
- Topics include computer arithmetic, instruction set design, microprogrammed control unit, pipelining and vector processing, memory organization and I/O systems, and multiprocessors

Course Outcomes

- Understand the basics of instruction sets and their impact on processor design.
- Demonstrate an understanding of the design of the functional units of a digital computer system.
- Evaluate cost performance and design trade-offs in designing and constructing a computer processor including memory.
- Design a pipeline for consistent execution of instructions with minimum hazards.
- Recognize and manipulate representations of numbers stored in digital computers

UNIT - I

Digital Computers: Introduction, Block diagram of Digital Computer, Definition of Computer Organization, Computer Design and Computer Architecture.

Register Transfer Language and Micro operations: Register Transfer language, Register Transfer, Bus and memory transfers, Arithmetic Micro operations, logic micro operations, shift micro operations, Arithmetic logic shift unit.

Basic Computer Organization and Design: Instruction codes, Computer Registers Computer instructions, Timing and Control, Instruction cycle, Memory Reference Instructions, Input – Output and Interrupt.

UNIT - II

Microprogrammed Control: Control memory, Address sequencing, micro program example, design of control unit.

Central Processing Unit: General Register Organization, Instruction Formats, Addressing modes, Data Transfer and Manipulation, Program Control.

UNIT - III

Data Representation: Data types, Complements, Fixed Point Representation, Floating Point Representation, Computer Arithmetic: Addition and subtraction, multiplication Algorithms, Division Algorithms, Floating-point Arithmetic operations, Decimal Arithmetic unit, Decimal Arithmetic operations.

UNIT - IV

Input-Output Organization: Input-Output Interface, Asynchronous data transfer, Modes of Transfer, Priority Interrupt Direct memory Access.

Memory Organization: Memory Hierarchy, Main Memory, Auxiliary memory, Associate Memory, Cache Memory.

UNIT - V

Reduced Instruction Set Computer: CISC Characteristics, RISC Characteristics.

Pipeline and Vector Processing: Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline, Vector Processing, Array Processor.

Multi Processors: Characteristics of Multiprocessors, Interconnection Structures, Interprocessor arbitration, Interprocessor communication and synchronization, Cache Coherence.

TEXT BOOK:

1. Computer System Architecture – M. Morris Mano, Third Edition, Pearson/PHI.

REFERENCE BOOKS:

1. Computer Organization – Carl Hamacher, Zvonks Vranesic, SafeaZaky, V th Edition, McGrawHill.
2. Computer Organization and Architecture – William Stallings Sixth Edition, Pearson/PHI.
3. Structured Computer Organization – Andrew S. Tanenbaum, 4 th Edition, PHI/Pearson.

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on Rev1:
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Sub. Code & Title	R22CSE2114 Computer Organization and Architecture
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Academic Year: 2025-26	Year/Sem./Section	II-I/AIML
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Faculty Name & Designation	K.PADMA , Assistant Professor
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Unit/ Item No.	Topic (s)	Book Reference	Page (s)		Teaching Methodology	Proposed No. of Periods	Actual Date of Handled	CO/RBT
			From	To				
	UNIT-I							
1	INTRODUCTION –DIGITAL COMPUTERS					15		
1.1	Digital Computers: Introduction	T1	1	11	Black board	01		CO1,L2
1.2	Block diagram of Digital Computer	T1	15	16	Black board	01		CO1,L6
1.3	Definition of Computer Organization, Computer Design and Computer Architecture.	T1	3	4	Black board	01		CO1,L1
1.4	Register Transfer Language and Micro operations: Register Transfer language.	T1	111	112	Black board	01		CO1,L2
1.5	Register Transfer	T1	112	115	Black board	01		CO1,L2
1.6	Bus and memory transfers	T1	115	119	Black board	01		CO1,L1
1.7	logic micro operations	T1	125	130	Black board	01		CO1,L3
1.8	shift micro operations	T1	130	133	Black board	01		CO1,L3
1.9	Arithmetic logic shift unit.	T1	133	135	Black board	01		CO1,L3
1.10	Basic Computer Organization and Design:	T1	141	144	Black board	01		CO1,L2
1.11	Computer Registers	T1	144	149	Black board	01		CO1,L1
1.12	Computer instructions	T1	149	153	Black board	01		CO1,L2
1.13	Timing and Control	T1	153	156	Black board	01		CO1,L1
1.14	Instruction cycle	T1	156	161	Black board	01		CO1,L4
1.15	Memory Reference Instructions, Input – Output and Interrupt.	T1	162	172	Black board	01		CO1,L4
	Review	Signature of the HOD/Coordinator						

[Type text]

	SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY LESSON PLAN (Regulation :R22) Department of Computer Science and Engineering					Prepared on Rev1: Page: 12 of 7			
	Sub. Code & Title		R22CSE2114 Computer Organization and Architecture						
	Academic Year: 2025-26			Year/Sem./Section		II-I/AIML			
	Faculty Name & Designation			K.PADMA &Assistant Professor					
Unit/ Item No.	Topic (s)	Book Reference	Page (s)		Teaching Methodology	Proposed No. of Periods	Actual Date of Handled	CO/RBT	
			From	To					
	UNIT-II								
2	Microprogrammed Control, Central Processing unit					10			
2.1	Microprogrammed Control: Control memory	T1	235	238	Black board	01		CO2,L1	
2.2	Address sequencing	T1	238	16	Black board	01		CO2,L2	
2.3	Micro program example	T1	242	4	Black board	01		CO2,L1	
2.4	Design of control unit.	T1	253	112	Black board	01		CO2,L2	
2.5	Central Processing Unit: General Register Organization,	T1	265	115	Black board	01		CO2,L1	
2.6	** Stack Organization	T1	270	119	Black board	01		CO2,L2	
2.7	Instruction Formats: Three Address Instructions, Two Address Instructions	T1	278	130	Black board	01		CO2,L3	
2.8	Addressing modes	T1	283	133	Black board	01		CO2,L4	
2.9	Data Transfer and Manipulation	T1	289	135	Black board	01		CO2,L1	
2.10	Program Control.	T1	295	144	Black board	01		CO2,L1	
	Review	Signature of the HOD/Coordinator							

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on Rev1:
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Sub. Code & Title	R22CSE2114 Computer Organization and Architecture
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Year/Sem./Section	II-I-AIML
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Faculty Name & Designation	K.PADMA& Assistant Professor
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Unit/ Item No.	Topic (s)	Book Reference	Page (s)		Teaching Methodology	Proposed No. of Periods	Actual Date of Handled	CO/RBT
			From	To				
	UNIT-III							
3	Data Representation, Computer Arithmetic					09		
3.1	Data Representation: Data types	T1	81	87	Black board	02		CO3,L2
3.2	Complements (r-1)'s Complement and (r's Complement)	T1	89	90	Black board	01		CO3,L3
3.3	Fixed Point Representation,	T1	91	95	Black board	01		CO3,L1
3.4	Floating Point Representation.	T1	97	97	Black board	01		CO3,L1
3.5	Computer Arithmetic: Addition and subtraction	T1	365	370	Black board	02		CO3,L3
3.6	Division Algorithms	T1	372	377	Black board	01		CO3,L3
3.7	Multiplication Algorithms	T1	372	377	Black board	01		CO3,L3
3.8	Floating – point Arithmetic operations.	T1	385	393	Black board	01		CO3,L3
3.9	Decimal Arithmetic unit	T1	395	398	Black board	01		CO3,L3
	Review	Signature of the HOD/Coordinator						

Department of Computer Science and Engineering

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R22CSE2114 Computer Organization and Architecture

II-I/AIML

K.PADMA &Assistant Professor

Unit/ Item No.	Topic (s)	Book Reference	Page (s)		Teaching Methodology	Proposed No. of Periods	Actual Date of Handled	CO/RBT
			From	To				
	UNIT-IV							
4	Input Output Organization, Memory Organization					09		
4.1	Input-Output Organization: Input-Output Interface	T1	413	421	Black board	01		CO4,L2
4.2	Asynchronous data transfer	T1	422	431	Black board	01		CO4,L1
4.3	Modes of Transfer	T1	433	437	Black board	01		CO4,L2
4.4	Priority Interrupt	T1	437	445	Black board	01		CO4,L1
4.5	Direct memory Access.	T1	446	448	Black board	01		CO4,L6
4.6	Discuss Memory Hierarchy, Main Memory	T1	479	490	Black board	01		CO4,L2
4.7	Auxiliary memory	T1	493	495	Black board	01		CO4,L1
4.8	Associate Memory	T1	495	500	Black board	01		CO4,L1
4.9	Cache Memory	T1	500	508	Black board	01		CO4,L1
	Review	Signature of the HOD/Coordinator						

	SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY			Prepared on Rev1: Page: 15 of 7	
	LESSON PLAN				
	(Regulation :R22)				
	Department of Computer Science and Engineering				
	Sub. Code & Title		R22CSE2114 Computer Organization and Architecture		
Academic Year: 2025-26			Year/Sem./Section	II-I	
Faculty Name & Designation			K.PADMA , Assistant Professor		

Unit/ Item No.	Topic (s)	Book Reference	Page (s)		Teaching Methodology	Proposed No. of Periods	Actual Date of Handled	CO/RBT
			From	To				
	UNIT-V							
5	Reduced Instruction Set Computer, Pipeline and Vector Processing ,Multiprocessors					14		
5.1	Reduced Instruction Set Computer: CISC Characteristics,	T1,	304	305	Black board	01		CO5,L2
5.2	RISC Characteristics.	T1,	306	312	Black Board	01		CO5,L2
5.3	Pipeline & Vector Processing	T1,	323	328	Black board	01		CO5,L1
5.4	Parallel Processing,	T1,	323	328	Black board	01		CO5,L1
5.5	Pipelining, Arithmetic Pipeline,	T1,	329	336	Black board	01		CO5,L1
5.6	Instruction Pipeline,	T1,	337	343	Black board	01		CO5,L1
5.7	RISC Pipeline,	T1,	343	348	Black board	01		CO5,L1
5.8	Vector Processing,	T1,	348	354	Black board	01		CO5,L1
5.9	Array Processor	T1,	354	356	Black board	01		CO5,L2
5.10	Multi Processors: Characteristics of Multiprocessors,	T1,	529	531	Black board	01		CO6,L2
5.11	Interconnection Structures,	T1,	531	539	Black board	01		CO6,L5
5.12	Inter - Processor arbitration,	T1,	539	544	Black board	01		CO6,L1
5.13	Inter - Processor communication and synchronization,	T1,	545	548	Black board	01		CO6,L1
5.14	Cache Coherence.	T1,	550	553	Black board	01		CO6,L2
	Review	Signature of the HOD/Coordinator						

TEXT BOOKS:

[Type text]

T1. Computer System Architecture – M. Moris Mano, Third Edition, Pearson/PHI.

REFERENCE BOOKS:

R1. Computer Organization – Car Hamacher, Zvonks Vranesic, Safea Zaky, Vth Edition, McGraw Hill

R2. Computer Organization and Architecture – William Stallings Sixth Edition, Pearson/PHI.

R3. Structured Computer Organization – Andrew S. Tanenbaum, 4th Edition, PHI/Pearson.

WEB LINKS: **https://onlinecourses.nptel.ac.in/noc21_cs61/previewASSIGNMENT**

ASSIGNMENT -1

Batch. No	Assignment Questions	Registered Roll Numbers	Course outcome	Level
1.	- What is the primary purpose of a block diagram in digital computers, and how does it represent the computer's components and their connections? - Define Computer Organization and explain its significance in the context of digital computer systems. - Differentiate between Computer Design and Computer Architecture. How do they relate to each other in the development of computer systems? - What is Register Transfer Language (RTL), and how is it used in computer design and organization? - Describe the concept of Register Transfer in computer architecture. How does it facilitate data movement and processing within the CPU?	24D41A6601 to 24D41A6606	CO1 CO1 CO1 CO1	1 2 1 2 1
2.	- Explain the role of the Bus in digital computer systems and how it enables data transfer between different components. - Discuss the various types of memory transfers in computer organization and their importance in data storage and retrieval. - Define Arithmetic Micro Operations and provide examples of common arithmetic operations carried out in digital computers. - What are Logic Micro Operations, and how do they contribute to data manipulation and decision-making in computer systems? - Describe Shift Micro Operations and their relevance in data shifting and manipulation within a computer's registers	24D41A6607 to 24D41A6611	CO1 CO1 CO1 CO1 CO1	2 3 4 4 6
3.	1 What is an Arithmetic Logic Shift Unit (ALU), and how does it perform arithmetic, logic, and shift operations in digital computers? - Explain the concept of Instruction Codes in the context of	24D41A6612 to 24D41A6617	CO1 CO1 CO1	1 2 1

	computer architecture. How are they used to control the execution of computer instructions? 3. How do Computer Registers play a crucial role in the functioning of a CPU, and what are their various types and purposes? 4. Discuss the components and stages involved in the Timing and Control of computer operations within a CPU. 5. Define the term "Instruction Cycle" in computer architecture and outline the steps involved		CO1	1
			CO1	1
4.	1. Explain the significance of Memory Reference Instructions and their role in accessing and manipulating data in computer memory. 2. Describe the role of Input-Output (I/O) operations in a computer system and how they enable communication with external devices. 3. What is an Interrupt in the context of computer architecture, and how does it impact the normal flow of program execution? 4. How does address sequencing play a crucial role in the operation of a control unit? 5. What is the primary function of control memory in a computer's control unit?	24D41A6618 to 24D41A6622	CO1 CO1 CO1 CO1	1 4 3 4 5

5.	1. Can you provide an example of a microprogram for a simple operation like addition in a hypothetical computer architecture? 2. Explain the concept of microinstructions and how they relate to the control unit's operation. 3. What are the key components and signals involved in the design of a control unit for a modern CPU? 4. Describe the difference between horizontal and vertical microprogramming for control unit design. 5. How does the control unit manage branching and conditional execution within a microprogram?	24D41A6623 to 24D41A6627	CO2 CO2 CO2 CO2	1 2 1 1
6.	1. In the context of control unit design, what is meant by a control word and how is it used? 2. Discuss the concept of microprogram sequencing and its importance in executing machine instructions. 3. Can you provide an overview of the control memory organization in a typical microprogrammed control unit? 4. What is the purpose of the general register organization in a CPU, and how does it impact the performance of a computer system? 5. Can you explain the difference between general-purpose registers and special-purpose registers in a CPU's register organization?	24D41A6628 to 24D41A6633	CO2 CO2 CO2 CO2	1 4 3 5 6
7.	1. How does the choice of register organization affect the design and performance of a processor in a computer system? 2. Describe the role of the instruction pointer register in the context of general register organization. How is it used in program execution? 3. What are the advantages and disadvantages of using a stack-based register organization in a CPU? 4. In instruction formats, what is the significance of the opcode field, and how does it determine the operation to be performed by the CPU? 5. Explain the concept of immediate addressing in instruction formats. How is data represented and accessed using this addressing mode?	24D41A6635 to 24D41A6640	CO2 CO2 CO2 CO2	1 2 1 2 1

8.	1. Compare and contrast the various addressing modes commonly used in instruction formats, such as register addressing, direct addressing, and indirect addressing. 2. How do variable-length instruction formats differ from fixed-length instruction formats, and what are the trade-offs associated with each approach? 3. Discuss the role of the condition code flags in the execution of instructions and how they influence the control flow in a processor. 4. What is the purpose of addressing modes in computer architecture, and how do they affect the execution of instructions? 5. Explain the difference between immediate addressing and direct addressing. Provide examples for each.	24D41A6641 to 24D41A6645	CO2 CO2 CO2 CO2	1 3 4 4 6
9.	1. Describe the concept of indexed addressing mode and provide a scenario where it would be useful in a computer program. 2. How does relative addressing mode work, and when is it commonly used in assembly language programming? 3. Discuss the significance of the stack pointer in addressing modes and its role in subroutine calls. 4. Define data transfer instructions in the context of assembly language. Provide examples of commonly used data transfer instructions. 5. Explain the purpose of the "load" and "store" instructions and how they are used to move data between memory and registers	24D41A6646 to 24D41A6651	CO3 CO3 CO3 CO3	1 1 1 2 2
10.	1. How are shift and rotate instructions used to manipulate data, and what are some practical applications of these instructions? 2. Describe the concept of data conversion instructions, such as converting binary to decimal or hexadecimal. Why are these conversions important in assembly language programming? 3. What is the significance of conditional data transfer instructions, and how do they impact program control flow based on specific conditions? 4. What is the difference between unconditional and conditional branching instructions in program control, and when would you	24D41A6652 to 24D41A6656	CO3 CO3 CO3 CO3	1 1 2 3 2

	use each type? 5. Explain the concept of subroutine calls and returns in program control. How do these instructions impact the organization of a program?			
11.	1. How do interrupt instructions affect the normal flow of a program, and what is their role in handling external events? 2. Discuss the significance of the program counter (PC) in program control and how it is updated during instruction execution. 3. What are the benefits and drawbacks of using jump instructions for program control, and in what situations would you choose to use them? 4. What are the key components of a typical instruction format, and how do they work together to decode and execute instructions? 5. Explain the significance of the addressing mode in instruction formats and how it affects the access to memory or registers during instruction execution.	24D41A6657 to 24D41A6661	CO1 CO1 CO1 CO1 CO1	1 2 1 1 1
12.	1. What are the primary data types in most programming languages, and what are their characteristics? 2. Explain the difference between signed and unsigned data types. 3. How are characters represented in computer memory, and what is the ASCII code? 4. What is the two's complement, and how is it used in binary arithmetic? 5. Describe the process of finding the one's complement of a binary number.	24D41A6662 to 24D41A6664	CO1 CO1 CO1 CO1 CO1	1 2 3 4 4
13.	1. How does the method for finding the two's complement differ from the one's complement? 2. What is the purpose of addressing modes in computer architecture, and how do they affect the execution of instructions? 3. Explain the difference between immediate addressing and direct addressing. Provide examples for each. 4. Define the term "Instruction Cycle" in computer architecture and outline the steps involved in the execution of an instruction.		CO1 CO1 CO1 CO1 CO1	1 2 1 2 1

	5. Explain the significance of Memory Reference Instructions and their role in accessing and manipulating data in computer memory.			
14	1. Differentiate between Computer Design and Computer Architecture. How do they relate to each other in the development of computer systems? 2. What is Register Transfer Language (RTL), and how is it used in computer design and organization? 3. Describe the concept of Register Transfer in computer architecture. How does it facilitate data movement and processing within the CPU? 4. Explain the role of the Bus in digital computer systems and how it enables data transfer between different components. 5. Discuss the various types of memory transfers in computer organization and their importance in data storage and retrieval.	-----	-----	-----

ASSIGNMENT -2

Batch. No	Assignment Questions	Registered Roll Numbers	Course outcome	Level
6.	1.The status bit is also called as - a) Unsigned bit b) Signed bit c) Flag bit d) None of the above 7. Cache memory is used in a computer system to _____ 8. To illustrate the influence of the number of address on computer programs, we will evaluate the arithmetic statement $X=(A+B)*(C+D)$ using two address Instruction format. (Apply) 4. In floating-point representation, the part represents a signed & fixed-point number is called as? a) Exponent b) Mantissa c) Normalized d) Float 5. Explain in detail about the RISC Characteristics. (Understand)	24D41A6601 to 24D41A6606	L1 L1 L3 L1 L2	CO2 CO2 CO2 CO3 CO6
2	1.In floating-point representation, the part represents a signed & fixed-point number is called as? 6. Exponent 7. Mantissa 8. Normalized 9. Float. 2. Draw and explain the hardware for signed – magnitude addition and subtraction. (Understand) 3. To reduce the memory access time, we generally make use of _____ a) SDRAM's b) Heaps c) Cache's d) Higher capacity RAM's	24D41A6607 to 24D41A6611	CO3 CO3 CO5 CO5 CO6	1 2 1 1 2

	4. Explain in detail about Input and output interface with example. (Understand) 5. Explain in detail about the CISC Characteristics. (Understand)			
3.	1. Explain the different types of Pipeline techniques. (Understand) 2. RISC stands for _____ 3. Explain in detail about DMA operation with neat diagram. (Understand). 4. Which of the following is correct example for Auxiliary Memory? a) Magnetic disks b) Tapes c) Flash memory. d) Both A and B 5. Explain in detail about addition and subtraction with signed 2's complement data. (Understand)	24D41A6612 to 24D41A6617	CO6 CO5 CO5 CO5 CO3	2 2 2 2 2
4.	1. If the radix point (binary point) is fixed and assumed to be to on the right of the right most digit, the representation of such number is called a) Fixed point b) Floating point c) Radix point D) None of these 2. The interrupt-request line is a part of the _____ 3. Perform division process of fixed point binary number in signed-magnitude representation 10001 and 01110 using restoring division algorithm. (Apply) 4. In memory-mapped I/O _____ a) The I/O devices have a separate address space b) The I/O devices and the memory share the same address space c) A part of the memory is specifically set aside for the I/O operation d) The memory and I/O devices have an associated address space 5. Write a note on memory hierarchy with the neat diagram. (Remember)	24D41A6618 to 24D41A6622	CO3 CO4 CO3 CO5 CO5	1 1 3 1 1

5.	1.Explain in detail about Cache memory mechanisms. (Understand) 2.Which of the following is the full form of CISC? a) Complex Instruction Sequential Compilation b) Complete Instruction Sequential Compilation c) Computer Integrated Sequential Compiler d) Complex Instruction Set Computer 3.Describe in detail about inter process communication and synchronization. 4. Explain the following data transfer modes/techniques. (Understand) a) Program Controlled IO b) Interrupt Initiated IO c) Direct memory access (DMA) 5.What is true about memory unit? a) A memory unit is the collection of storage units or devices together. b) The memory unit stores the binary information in the form of bits. c) Both A and B d) None of the above	24D41A66223 to 24D41A6627	CO5 CO6 CO5 CO5 CO5	2 2 2 2 1
6.	1.Sign bit 1 represents a) Positive number b) FALSE c) TRUE Negative Number 2. Explain the booth's multiplication algorithm with neat sketch of hardware design. (Understand) 3. The devices with variable speeds are usually connected using asynchronous BUS. a) True b) False 4. Write a note on memory hierarchy with the neat diagram. (Remember) 5.The interrupt-request line is a part of the _____	24D41A6628 to 24D41A6633	CO4 CO3 CO5 CO2 CO4	1 2 1 5 1
7.	1.Explain in detail about floating point arithmetic operations. 2. Most computers use the _____ representation when performing arithmetic operations with integers. a) signed-magnitude b) signed-1's complement c) signed-2's complement any of the above 3.Describe detail about Program control unit. (Understand) 4. Draw and explain the one stage decimal arithmetic unit. (Understand)	24D41A6635 to 23D41A6640	CO4 CO4 CO4 CO4	2 1 2 2

	5. Which of the following is the full form of CISC? a) Complex Instruction Sequential Compilation b) Complete Instruction Sequential Compilation c) Computer Integrated Sequential Compiler d) Complex Instruction Set Computer		CO2	6
8.	1. RISC stands for - a) Reduce Instruction Set Computer b) Risk Instruction Sequential Compilation c) Risk Instruction Source Compiler d) None of the above 2. Explain the different types of Pipeline techniques. (Understand) 3. Which one is not benefit of multiprocessors? A single job can be partitioned into multiple parallel tasks b) Multiple jobs can be made to operate in serial c) Multiple independent jobs can be made to operate in parallel d) All are benefits 4. Explain in detail about Cache memory mechanisms. (Understand) 5. RISC stands for _____	24D41A6641 to 24D41A6645	CO6 CO6 CO6 CO5 CO6	1 2 2 2 1
9.	1. Explain in detail about basic multiprocessor architecture. (Understand) 2. Explain with neat sketch auxiliary memory. (Understand) 3. What is true about memory unit? a) A memory unit is the collection of storage units or devices together. b) The memory unit stores the binary information in the form of bits. c) Both A and B d) None of the above 4. Explain in detail about addition and subtraction with signed 2's complement data. (Understand) 5. RISC stands for _____	24D41A6646 to 24D41A6651	CO6 CO5 CO5 CO3 CO6	2 2 1 2 1
10.	1. Which one of the following is a multiplication algorithm? a) Comparison method b) Restoring method c) Quick sort algorithm d) Booth's algorithm 2. The interrupt-request line is a part of the _____ 3. Explain the booth's multiplication algorithm with neat sketch of hardware design. (Understand) 4. How many types of modes of I/O Data Transfer?	24D41A6652 to 24D41A6656	CO4 CO4 CO3 CO3 CO5	2 1 2 2 1

	a) 2 b) 3 c) 4 d) 5 5. MIMD stands for _____			
11.	1. Which of the following is the full form of CISC? a) Complex Instruction Sequential Compilation b) Complete Instruction Sequential Compilation c) Computer Integrated Sequential Compiler d) Complex Instruction Set Computer 2. Explain in detail about the RISC Characteristics. (Understand) 3. Zero address instructions are necessarily used in _____ architecture. a) Stack b) CISC c) RISC d) Parallel 3. write a note on memory hierarchy 4. Explain the different types of Pipeline techniques. (Understand) 5. CISC stands for _____	24D41A6657 to 24D41A6661	CO6 CO6 CO6 CO6 CO6	2 2 1 2 1
12.	1. Explain in detail about floating point arithmetic operations. 2. How many types of modes of I/O Data Transfer? a) 2 b) 3 c) 4 d) 5 3. The computer architecture aimed at reducing the time of execution of instructions is _____ 4. Describe in brief the different modes by which data transfer can take place between a computer unit and its I/O devices. What is the difference between synchronous and asynchronous data transfer? (Understand) (Evaluate) 5. RISC stands for _____	24D41A6662 to 24D41A6664	CO4 CO5 CO5 CO5 CO6	2 1 1 2,5 1
13.	1. Explain in detail about the Instruction Pipeline. (Understand) 2. CISC stands for _____ 3. In memory-mapped I/O _____ a) The I/O devices and the memory share the same address space b) The I/O devices have a separate address space c) The memory and I/O devices have an associated address space d) A part of the memory is specifically set aside for the I/O operation 4. Draw a flowchart for adding and subtracting two fixed point binary numbers where negative numbers are signed 1's complement presentation. (Understand) 5. Explain in detail about Input and output interface with example. (Understand)		CO6 CO5 CO4 CO4 CO5	2 1 1 2 2

QUESTION BANK

	SRI INDU COLLEGE OF ENGG & TECHNOLOGY			Prepared on : 12-09-2024 Pages: 14
	QUESTION BANK			
	(Regulation :R22)			
	Department of COMPUTER SCIENCE AND ENGINEERING (AIML)			
Sub. Code & Title		(R22CSE2114) Computer Organization and Architecture		
Academic Year: 2025-26		Year/Sem./Section	II B.TECH I-SEM/AIML	
Faculty Name & Designation		K.PADMA, Assistant Professor		
UNIT-I: Digital Computers, Register Transfer Language and Micro operations, Basic Computer Organization and Design				
Multiple Choice Questions			BT Level	Course Outcome
#1C-1	What is computer architecture? a) set of categories and methods that specify the functioning, organisation, and implementation of computer systems b) set of principles and methods that specify the functioning, organisation, and implementation of computer systems c) set of functions and methods that specify the functioning, organisation, and implementation of computer systems d) None of the mentioned		L1	CO1
#1C-2	What is computer organization? a) structure and behaviour of a computer system as observed by the user b) structure of a computer system as observed by the developer c) structure and behaviour of a computer system as observed by the developer d) All of the mentioned		L1	CO1
#1C-3	Which of the following is a type of computer architecture? a) Microarchitecture b) Harvard Architecture c) Von-Neumann Architecture d) All of the mentioned		L2	CO1
#1C-4	What is the purpose of the Program Counter Register ? a) Contains the Address of a variable b) Contains the Address of the next instruction to be executed c) Contains the Address of the Memory d) Contains the Address of the Branch Instruction		L2	CO1
#1C-5	What is the purpose of the Full Adder Circuit ? a) Addition of 2 input bits and producing 2 output bits b) Addition of 4 input bits and producing 3 output bits c) Addition of 3 input bits and producing 2 output bits d) None of the above		L2	CO1

#1C-6	How many outputs can be produced by a Decoder with 3 input bits ? a) 3 outputs b) 9 outputs c) 12 outputs d) 8 outputs	L1	CO1
#1C-7	Which of the following allows simultaneous write and read operations? a) ROM b) EROM c) RAM d) None of the above	L2	CO1
#1C-8	Which of the following computer memory is fastest? a) Register b) Hard disk c) RAM d) None of the above	L2	CO1
#1C-9	Which of the following operations is/are performed by the ALU? a) Data manipulation b) Exponential c) Square root d) All of the above	L2	CO1
#1C-10	Which of the following memory of the computer is used to speed up the computer processing? a) Cache memory b) RAM c) ROM d) None of the above	L2	CO1
#1C-11	Identify the type of instruction for the bits 0111 at 15 to 12 locations of Instruction register. a) Indirect Memory Reference Instruction b) Register Reference Instruction c) Input-Output Instruction d) Direct Memory Reference Instruction	L1	CO1

#1C-12	In the Instruction format what are bits allocated for Operation Code ? a) 0 - 15 b) 0 - 11 c) 12 – 14 d) None of the above	L2	CO1
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	Filling The Blank Questions				
#1F-1	The communication line between the CPU, memory and other devices is called _____		L4	CO1	
#1F-2	The full form of EPROM _____		L2	CO1	
#1F-3	The equal-lent decimal value for the binary number 1011101 is _____		L3	CO1	
#1F-4	Computer can understand only _____ language.		L1	CO1	
#1F -5	ASCII stands for _____		L2	CO1	
Match The Following Questions					
#1M-1		a) Address of the next instruction for execution	MAR	L4	CO1
		b) Address of memory unit	PC		
		c) Register to maintain an instruction ready for execution	MBR		
		d) Register to hold the value of memory	IR		
5 MARKS QUESTIONS					
#1D-1	With the help of a block schematic explain the basic organizational units of a Digital computer. (Understand)			L2	CO1
#1D-2	Give the design of basic arithmetic and logic operations of ALU ? (Create)			L6	CO1
#1D-3	Explain the stored program organization with neat diagram construction. (Create)			L6	CO1
#1D-4	Analyze the process involved in Register Transfer Language. (Analyze)			L4	CO1
#1D-5	Perform the Bus and Memory Transfer using MUX (Analyze)			L5	CO1
#1D-6	Explain in Detail about Common Bus System for basic computer register. (Understand)			L2	CO1
#1D-7	Explain the different instruction formats in detail. (Analyze)			L4	CO1
#1D-8	Design and Explain the Control unit and Timing Diagram of Basic Computer? (Create)			L6	CO1
#1D-9	Review the different phases of Instruction Cycle? (Evaluate)			L5	CO1
#1D-10	Determine the input-output configuration. (Evaluate)			L5	CO1

UNIT-II: Micro programmed Control, Central Processing Unit			
Multiple Choice Questions		BT Level	Course Outcome
#2C-1	The control signal in micro programming can be designed by_____ a) Hardwired b) High level language c) Micro-programmed d) Both Micro-programmed and Hardwired	L1	CO2
#2C-2.	The address in the main memory is known as – a) Logical address b) Physical address c) Effective address d) None of the above	L2	CO2
#2C-3.	Which of the following register can interact with the secondary storage memory address ? a) PC b) MAR c) MDR d) IR	L2	CO2
#2C-4.	The decoded instruction placed at the _____ register a) Registers b) MDR c) PC d) IR	L1	CO2
#2C-5.	A Micro program contains sequence of _____ a. Operations b. Micro words c. Micro instructions d. None of the above	L1	CO2
#2C-6.	Which of the following register keeps track of the instructions stored in the program ? a) Accumulator b) Address Register c) Program Counter d) Index Register	L2	CO2
#2C-7.	The address of the instruction for execution at control memory is maintained by _____ a) Control Buffer Register	L3	CO2

	b) Control Address Register c) Program Counter d) Both b & c												
#2C-8.	Multiplexer circuit designed to work with the signals of _____ a) Many inputs and one output b) One input and Many outputs c) One input and One output d) Many inputs and Many outputs	L3	CO2										
#2C-9.	The Micro instruction format requires _____ number of bits a) 11 (0 to 10) b) 20 (0 to 19) c) 16 (0 to 15) d) 12 (0 to 11)	L4	CO2										
#2C-10.	The decoder is a circuit to convert _____ a) Decimal to Binary b) Decimal to Octal c) Binary to Octal d) Binary to Decimal	L2	CO2										
	Filling The Blank Questions												
#2F-1	The MAR stands for _____	L3	CO2										
#2F-2	Cache memory placed between _____ and _____ to improve the computer performance.	L4	CO2										
#2F-3	_____ is a general purpose processing register.	L1	CO2										
#2F-4	In Micro Programmed Control unit, the selection of next instruction address done by _____	L1	CO2										
#2F-5	_____ is a set of micro-instructions that are stored in microprogram memory and are related to a specific instruction.	L2	CO2										
	Match The Following Questions												
#2M-1	<table><tr><th>List I</th><th>List II</th></tr><tr><td>a) Zero Address Instruction</td><td>i) Volatile memory</td></tr><tr><td>b) One Address Instruction</td><td>ii) Compiler</td></tr><tr><td>c) Random Access Memory</td><td>iii) Accumulator</td></tr><tr><td>d) Programming Language Translator</td><td>iv) Stack Organized Computer</td></tr></table>	List I	List II	a) Zero Address Instruction	i) Volatile memory	b) One Address Instruction	ii) Compiler	c) Random Access Memory	iii) Accumulator	d) Programming Language Translator	iv) Stack Organized Computer	L4	CO2
List I	List II												
a) Zero Address Instruction	i) Volatile memory												
b) One Address Instruction	ii) Compiler												
c) Random Access Memory	iii) Accumulator												
d) Programming Language Translator	iv) Stack Organized Computer												
5 MARKS QUESTIONS													
#2D-1	Draw and explain about Micro Program Control Organization. (Understand)	L2	CO2										

#2D-2	Design Micro Program Sequencer for Control Memory and explain. (Understand)	L2	CO2
#2D-3	Design the Selection of Address for Control memory and explain. (Remember)	L1	CO2
#2D-4	Explain general register organization in detail with neat diagrams. (Understand)	L4	CO2
#2D-5	To illustrate the influence of the number of address on computer programs, we will evaluate the arithmetic statement $X=(A+B)*(C+D)$ using THREE address Instruction format. (Evaluate)	L5	CO2
#2D-6	To illustrate the influence of the number of address on computer programs, we will evaluate the arithmetic statement $X=(A+B)*(C+D)$ using TWO address Instruction format. (Evaluate)	L5	CO2
#2D-7	To illustrate the influence of the number of address on computer programs, we will evaluate the arithmetic statement $X=(A+B)*(C+D)$ using ONE address Instruction format. (Evaluate)	L5	CO2
#2D-8	To illustrate the influence of the number of address on computer programs, we will evaluate the arithmetic statement $X=(A+B)*(C+D)$ using ZERO address Instruction format. (Evaluate)	L5	CO2
#2D-9	Explain in detail about various addressing modes. (Understand)	L2	CO2
#2D-10	Explain the operations done through Data Transfer and Manipulation. (Understand)	L2	CO2

UNIT-III: Data Representation, Computer Arithmetic			
Multiple Choice Questions		BT Level	Course Outcome
#3C-1	In floating-point representation, the part represents a signed & fixed-point number is called as? d) Exponent e) Mantissa f) Normalized	L1	CO3

	g) Float		
#3C-2	The method generally used in computer for subtraction is? a) 10's complement b) 9's complement c) 2's complement d) None of above	L1	CO3
#3C-3	2's complement is also called as? a) Mantissa b) 1's Complement + 1 c) Negate d) None of above	L1	CO3
#3C-4	The signed-1's complement representation of (-14) is? a) 10001110 b) 11110010 c) 10100101 d) 11110001	L2	CO3
#3C-5	When the result of an arithmetic operation on signed numbers doesn't fit the number of bits used can be identified by _____ d) Zero flag e) Sign flag f) Overflow flag g) Carry flag	L2	CO3
#3C-6	A 4 digit decimal number equal-lent BCD number can be represented with the help of ____ bits a) 10 bits b) 08 bits c) 12 bits d) 16 bits	L1	CO4
#3C-7	Which one of the following is a multiplication algorithm? e) Comparison method f) Restoring method g) Quick sort algorithm h) Booth's algorithm	L2	CO4
#3C-8	The full form of BCD is _____ a) Binary Calculation for Decimal b) Binary Count for Decimal c) Binary Coded Decimal d) None of the above	L1	CO4
#3C-9	In sign magnitude form the Sign bit 1 represents	L1	CO4

	d) Positive number e) FALSE f) TRUE g) Negative Number			
#3C-10	Most computers use the _____ representation when performing arithmetic operations with integers. d) signed-magnitude e) signed-1's complement f) signed-2's complement g) any of the above	L2	CO4	
Filling The Blank Questions				
#3F-1	A sequence of control words corresponding to a control sequence is called _____	L3	CO3	
#3F-2	Individual control words of the micro routine are called as _____	L3	CO3	
#3F-3	The method which offers higher speeds of I/O transfers is _____	L1	CO3	
#3F-4	The 9's Complement is a process of subtracting each digit from _____	L2	CO4	
#3F-5	The controller is connected to the _____	L1	CO4	
Match The Following Questions				
#3M-1	(i) Base addressing	(a)Pointers	L4	CO3
	(ii) Indexed addressing	(b)Loops		
	(iii) Indirect addressing	(c) Position independent		
	(iv) Auto increment addressing	(d)Array		
#3M -2	1. Booths Algorithm	a. 9's complement +1	L4	CO4
	2. 10's complement	b. To Complement the bits		
	3. Full Adder	c. Multiplication		
	4. Controlled Invertor	d. For addition of 3 bits		
5 MARKS QUESTIONS				
#3D-1	Draw and explain the hardware for signed – magnitude addition and subtraction. (Create)	L6	CO3	
#3D-2	Justify the addition and subtraction operations with signed 2's complement data. (Apply)	L5	CO3	
#3D-3	Explain the booth's multiplication algorithm with neat sketch of hardware design. (Create)	L6	CO3	
#3D-4	Perform division process of fixed-point binary number in signed-magnitude representation 10001 and 01110 using division algorithm. (Create)	L6	CO3	
#3D-5	Explain in detail about floating point arithmetic operations. (Understand)	L2	CO4	
#3D-6	Draw a flowchart for adding and subtracting two fixed point binary numbers where negative numbers are signed 1's complement presentation. (Create)	L6	CO4	
#3D-7	Draw the flowchart for divide operation and explain. (Create)	L6	CO4	
#3D-8	Draw and explain the one stage decimal arithmetic unit. (Create)	L6	CO4	
#3D-9	Explain in detail about the derivation of BCD adder. (Understand)	L2	CO4	

UNIT-IV: Input Output Organization, Memory Organization			
Multiple Choice Questions		BT Level	Course Outcome
#4C-1	To reduce the memory access time we generally make use of _____ a) SDRAM's b) Heaps c) Cache's d) Higher capacity RAM's	L1	CO5
#4C-2	In memory-mapped I/O _____ a) The I/O devices and the memory share the same address space b) The I/O devices have a separate address space c) The memory and I/O devices have an associated address space d) A part of the memory is specifically set aside for the I/O operation	L2	CO5
#4C-3	The performance of the cache memory can be measured in terms of ____ a. Check ratio b. Hit ratio c. Miss ratio d. Data transfer ratio	L1	CO5
#4C-4	The devices with variable speeds are usually connected using asynchronous BUS. a) True b) False	L1	CO5
#3C-5	How many types of modes of I/O Data Transfer? a) 2 b) 3 c) 4 d) 5	L1	CO5
#4C-6	The method which offers higher speeds of I/O transfers is _____ a) Interrupts b) Memory mapping c) Program-controlled I/O d) DMA	L2	CO5
#4C-7	In memory-mapped I/O _____ a) The I/O devices have a separate address space b) The I/O devices and the memory share the same address space c) A part of the memory is specifically set aside for the I/O operation d) The memory and I/O devices have an associated address space	L1	CO5
#4C-8	Which of the following is true about DMA? a) DMA is an approach of performing data transfers in bulk between memory and the external device without the intervention of the processor. b) The DMA controller acts as a processor for DMA transfers and overlooks the entire process. c) The DMA controller has 3 registers. d) All of the above	L2	CO5

#4C-9	Which of the following is correct example for Auxiliary Memory? a) Magnetic disks b) Tapes c) Flash memory. d) Both A and B	L2	CO5										
#4C-10	What is true about memory unit? a) A memory unit is the collection of storage units or devices together. b) The memory unit stores the binary information in the form of bits. c) Both A and B d) None of the above	L1	CO5										
Filling The Blank Questions													
#4F-1	The computer architecture aimed at reducing the time of execution of instructions is _____	L1	CO5										
#4F-2	The Sun micro systems processors usually follow _____ architecture.	L3	CO5										
#4F-3	MIMD stands for _____	L1	CO5										
#4F-4	A processor does not require _____ bus to communicate with memory.	L3	CO5										
#4F-5	A crossbar switch is an interconnection between CPUs and _____.	L4	CO5										
Match The Following Questions													
#4M-1	<table><tr><th>List I</th><th>List II</th></tr><tr><td>a) Handshaking</td><td>i) I/O interface informs the CPU that device is ready for transfer</td></tr><tr><td>b) Programmed I/O</td><td>ii) Requires two control signals working in opposite directions</td></tr><tr><td>c) Interrupt-initiated I/O</td><td>iii) Has local memory & control large set of I/O devices</td></tr><tr><td>d) I/O processor</td><td>iv) require CPU to check the I/O flag & perform transfer</td></tr></table>	List I	List II	a) Handshaking	i) I/O interface informs the CPU that device is ready for transfer	b) Programmed I/O	ii) Requires two control signals working in opposite directions	c) Interrupt-initiated I/O	iii) Has local memory & control large set of I/O devices	d) I/O processor	iv) require CPU to check the I/O flag & perform transfer	L4	CO5
List I	List II												
a) Handshaking	i) I/O interface informs the CPU that device is ready for transfer												
b) Programmed I/O	ii) Requires two control signals working in opposite directions												
c) Interrupt-initiated I/O	iii) Has local memory & control large set of I/O devices												
d) I/O processor	iv) require CPU to check the I/O flag & perform transfer												
5 MARKS QUESTIONS													
#4D-1	Explain in detail about Input and output interface with example. (Analyze)	L4	CO5										
#4D-2	What is asynchronous data transfer? Explain the different types of Asynchronous data transfer techniques. (Understand)	L2	CO5										
#4D-3	Compare the following data transfer modes/techniques. (Evaluate) a) Program Controlled IO b) Interrupt Initiated IO	L5	CO5										
#4D-4	Assess about memory hierarchy based on Access time ratio and cost per bit. (Evaluate)	L5	CO5										
#4D-5	Design and explain in detail about DMA operation. (Create)	L6	CO5										
#4D-6	Construct the diagram about memory hierarchy and explain (Create)	L6	CO5										
#4D-7	Distinguish the Synchronous and Asynchronous data transmission. (Analyze)	L4	CO5										

[Type text]

#4D-8	Explain in detail about associative memory mechanisms. (Understand)	L2	CO5
#4D-9	Demonstrate in detail about Cache memory mechanisms. (Apply)	L3	CO5
#4D-10	Explain about hand-shaking method of Asynchronous data transfer. (Analyze)	L4	CO5

UNIT-V: Reduced Instruction Set Computer, Pipeline & Vector Processing, Multiprocessors			
Multiple Choice Questions		BT Level	Course Outcome
#5C-1	Which of the architecture is power efficient? a) RISC b) ISA c) IANA d) CISC	L2	CO6
#5C-2	In CISC architecture most of the complex instructions are stored in ____ a) CMOS b) Register c) Transistors d) Diodes	L1	CO6
#5C-3	Both the CISC and RISC architectures have been developed to reduce the ____ a) Time delay b) Semantic gap c) Cost d) All of the mentioned	L1	CO6
#5C-4	Which of the following is the full form of CISC? a) Complex Instruction Sequential Compilation b) Complete Instruction Sequential Compilation c) Computer Integrated Sequential Compiler d) Complex Instruction Set Computer	L2	CO6
#5C-5	RISC stands for - e) Reduce Instruction Set Computer f) Risk Instruction Sequential Compilation g) Risk Instruction Source Compiler h) None of the above	L1	CO6
#5C-6	Zero address instructions are necessarily used in _____ architecture. e) Stack f) CISC g) RISC h) Parallel	L4	CO6
#5C-7	In CISC architecture most of the complex instructions are stored in ____ a) Register b) Diodes c) CMOS	L1	CO6

	d) Transistors												
#5C-8	Which one is not benefit of multiprocessors? a) single job can be partitioned into multiple parallel tasks b) Multiple jobs can be made to operate in serial c) Multiple independent jobs can be made to operate in parallel d) All are benefits	L2	CO6										
#5C-9	Which of the following is not one of the interconnection structures? a) Crossbar switch b) Hypercube system c) Single port memory d) Time-shared common bus	L3	CO6										
#5C-10	Which of the following is not characteristics of tightly coupled multiprocessors? a) Each processor has its own cache memory b) One global common memory that all CPUs can access c) Each processor has its own local memory d) Shared memory processors	L4	CO6										
Filling The Blank Questions													
#5F-1	_____ is the process of ensuring that shared data is consistent across multiple caches in a multiprocessor system	L3	CO6										
#5F-2	RISC stands for _____	L1	CO6										
#5F-3	CISC stands for _____	L1	CO6										
#5F-4	In CISC architecture most of the complex instructions are stored in _____	L3	CO6										
#5F-5	Multiprocessors are classified as _____	L2	CO6										
Match The Following Questions													
#5M-1	<table><tr><th>List I</th><th>List II</th></tr><tr><td>a) Isolated I/O</td><td>i) Same set of control signal for I/O and memory communication</td></tr><tr><td>b) Memory mapped I/O</td><td>ii) Separate instruction for I/O and memory communication</td></tr><tr><td>c) I/O interface</td><td>iii) Requires control signals to be transmitted between the communicating units</td></tr><tr><td>d) A synchronous data transfer</td><td>iv) Resolve the differences in central computer and peripherals</td></tr></table>	List I	List II	a) Isolated I/O	i) Same set of control signal for I/O and memory communication	b) Memory mapped I/O	ii) Separate instruction for I/O and memory communication	c) I/O interface	iii) Requires control signals to be transmitted between the communicating units	d) A synchronous data transfer	iv) Resolve the differences in central computer and peripherals	L4	CO6
	List I	List II											
	a) Isolated I/O	i) Same set of control signal for I/O and memory communication											
	b) Memory mapped I/O	ii) Separate instruction for I/O and memory communication											
	c) I/O interface	iii) Requires control signals to be transmitted between the communicating units											
d) A synchronous data transfer	iv) Resolve the differences in central computer and peripherals												

#5M -2	List I	List II	L4	CO6
	(a) Micro Operation	(i) Specify micro operation		
	(b) Micro Programed control unit	(ii) Improve CPU utilization		
	(c) Interrupts	(iii) Control Memory		
	(d) Micro Instruction	(iv) Elementary operation performed on data stored in registers		
#5M -3	List I	List II	L4	CO6
	a) Pipelined ALU	i) RISC		
	b) Simpler compiler	ii) CISC		
	c) Separate data and instruction	iii) Mixed RISC-CISC		
	d) Lesser cycles per instruction	iv) None		

5 MARKS QUESTIONS

#5D-1	Give a review on the RISC Characteristics. (Evaluate)	L5	CO6
#5D-2	Give a review on the CISC Characteristics. (Evaluate)	L5	CO6
#5D-3	Classify the different types of Pipeline techniques. (Analyze)	L4	CO6
#5D-4	Explain in detail about the Instruction Pipeline. (Understand)	L2	CO6
#5D-5	Explain in detail about basic multiprocessor architecture. (Analyze)	L4	CO6
#5D-6	List the Characteristics of Multiprocessors. Explain in detail about the Interconnection structures of Multiprocessor. (Understand)	L2	CO6
#5D-7	Illustrate about the Inter processor arbitration. (Apply)	L3	CO6
#5D-8	Analyze in detail about inter process communication and synchronization. (Create)	L6	CO6

	SRI INDU COLLEGE OF ENGG & TECHNOLOGY			Prepared on 08-07-2025
	Department of CSE- AIML			
	Sub.Code &Title	R22CSE2114-COA		
	AcademicYear:2025-26	Year/Sem./Section	II/I/AIML	
	Faculty Name & Designation	K.PADMA, Assistant Professor		

SELFSTUDYTOPICS			
S.No.	Topics	Books&Journals	CourseOutcomes
1	CPU DESIGN	Computer Organization – Car Hamacher, Zvonks Vranesic, Safea Zaky, Vth Edition, McGraw Hill.	CO5
2	MULTIPROCESSOR	Computer Organization and Architecture – William Stallings Sixth Edition, Pearson/PHI.	CO5

CONTENT BEYOND THE SYLLABUS			
S.No.	Topics	Books&Journals	CourseOutcomes
1	ETHICS IN HARDWARE DESIGN	IEEE MICRO, 5th Edition	CO5
2	PHOTONIC COMPUTING	HPCA CONFERENCE	CO5

WEBLINKS:

<https://www.edx.org/learn/computer-networking>
https://onlinecourses.nptel.ac.in/noc21_cs61/preview

<https://www.edx.org/course/computer-networks>

MID QUESTION PAPERS
&
END SEMESTER QUESTION PAPERS

BR-22

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY
II B.Tech - I Semester - I Mid Term Examination, SEP/OCT - 2024
(R22CSE2114) COMPUTER ORGANIZATION AND ARCHITECTURE
(For CSE, CS, AIML, AIDS and DS)

D4

Duration: 2 Hrs

Dt: 01-10-2024, Day-2 (AN)

Max Marks: 30M

Part - AAnswer All multiple choice questions.

Marks: 10Qx1/2M = 5M

* (L1-Remembering, L2-Understanding, L3-Applying, L4-Analyzing, L5-Evaluating, and L6-Creating.)

Blended Taxonomy Levels	Course Outcome
I	CO1
II	CO1
II	CO1
II	CO1
II	CO2
I	CO2
III	CO2
II	CO2
I	CO3
II	CO3

- What is computer architecture?
 A) set of categories and methods that specify the functioning, organisation, and implementation of computer systems
 B) set of principles and methods that specify the functioning, organisation, and implementation of computer systems
 C) set of functions and methods that specify the functioning, organisation, and implementation of computer systems
 D) None of the mentioned
 [] I CO1
- What is the purpose of the Program Counter Register?
 A) Contains the Address of a variable
 B) Contains the Address of the next instruction to be executed
 C) Contains the Address of the Memory
 D) Contains the Address of the Branch Instruction
 [] II CO1
- Which of the following allows simultaneous write and read operations?
 A) ROM B) EROM C) RAM D) None of the above
 [] II CO1
- Which of the following operations is/are performed by the ALU?
 A) Data manipulation B) Exponential
 C) Square root D) All of the above
 [] II CO1
- The address in the main memory is known as _____
 A) Logical address B) Physical address
 C) Effective address D) None of the above
 [] II CO2
- The decoded instruction placed at the _____ register
 A) Registers B) MDR C) PC D) IR
 [] I CO2
- The address of the instruction for execution at control memory is maintained by _____
 A) Control Buffer Register B) Control Address Register
 C) Program Counter D) Both B & C
 [] III CO2
- The decoder is a circuit to convert _____
 A) Decimal to Binary B) Decimal to Octal
 C) Binary to Octal D) Binary to Decimal
 [] II CO2
- 2's complement is also called as _____
 A) Mantissa B) 1's Complement + 1
 C) Negate D) None of above
 [] I CO3
- The signed-1's complement representation of (-14) is _____.
 A) 10001110 B) 11110010
 C) 10100101 D) 11110001
 [] II CO3

Answer All fill in the blank questions.

Marks: 6Qx1/2M = 3M

- | | | |
|--|-----|-----|
| 11. The full form of EPROM _____ | II | CO1 |
| 12. Computer can understand only _____ language. | I | CO1 |
| 13. ASCII stands for _____ | II | CO1 |
| 14. Cache memory placed between _____ and _____ to improve the computer performance. | IV | CO2 |
| 15. _____ is a general purpose processing register. | I | CO2 |
| 16. Individual control words of the micro routine are called as _____ | III | CO3 |

Answer All Match the following questions.

Marks: 2Qx1M = 2M

- | | | | | |
|-----|--|--------|----|-----|
| 17. | 1. Address of the next instruction for execution | A. MAR | IV | CO1 |
| | 2. Address of memory unit | B. PC | | |
| | 3. Register to maintain an instruction ready for execution | C. MBR | | |
| | 4. Register to hold the value of memory | D. IR | | |
-
- | | | | | |
|-----|------------------------|---------------------------|----|-----|
| 18. | 1. Booths Algorithm | A. 9's complement +1 | IV | CO4 |
| | 2. 10's complement | B. To Complement the bits | | |
| | 3. Full Adder | C. Multiplication | | |
| | 4. Controlled Invertor | D. For addition of 3 bits | | |

Part – B

Answer any FOUR questions.

Marks: 4Qx5M = 20M

- | | | |
|---|----|-----|
| 19. Give the design of basic arithmetic and logic operations of ALU. | VI | CO1 |
| 20. Explain in detail about Common Bus System for basic computer register. | IV | CO1 |
| 21. Explain general register organization in detail with neat diagrams. | IV | CO2 |
| 22. To illustrate the influence of the number of address on computer programs, we will evaluate the arithmetic statement $X=(A+B)*(C+D)$ using ZERO address Instruction format. | V | CO2 |
| 23. Explain in detail about various addressing modes. | II | CO2 |
| 24. Justify the addition and subtraction operations with signed 2's complement data. | V | CO3 |

BR-22

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY
II B.Tech - I Semester - II Mid Term Examination, December – 2024
(R22CSE2114) COMPUTER ORGANIZATION AND ARCHITECTURE
(For CSE, CS, AIML, AIDS and DS)

D4

Duration: 2 Hrs

Dt: 18-12-2024, Day-2 (AN)

Max Marks: 30M

Part – A**Answer All multiple choice questions.****Marks: 10Qx1/2M = 5M**

* (L1-Remembering, L2-Understanding, L3-Appling, L4-Analyzing, L5-Evaluating, and L6-Creating.)

* **Blanks**
Exercises
Level**Course**
Outcomes

- | | | | |
|--|-------|-----|-----|
| 1. A 4 digit decimal number equal-lent BCD number can be represented with the help of _____ bits
A) 10 bits B) 08 bits C) 12 bits D) 16 bits | [] | I | CO4 |
| 2. The full form of BCD is _____
A) Binary Calculation for Decimal B) Binary Count for Decimal
C) Binary Coded Decimal D) None of the above | [] | I | CO4 |
| 3. Most computers use the _____ representation when performing arithmetic operations with integers.
A) signed-magnitude B) signed-1's complement
C) signed-2's complement D) any of the above | [] | II | CO4 |
| 4. The method which offers higher speeds of I/O transfers is _____
A) Interrupts B) Memory mapping
C) Program-controlled I/O D) DMA | [] | II | CO5 |
| 5. Which of the following is true about DMA?
A) DMA is an approach of performing data transfers in bulk between memory and the external device without the intervention of the processor.
B) The DMA controller acts as a processor for DMA transfers and overlooks the entire process.
C) The DMA controller has 3 registers.
D) All of the above | [] | II | CO5 |
| 6. Which of the following is correct example for Auxiliary Memory?
A) Magnetic disks B) Tapes C) Flash memory. D) Both A and B | [] | II | CO5 |
| 7. Which of the following is the full form of CISC?
A) Complex Instruction Sequential Compilation
B) Complete Instruction Sequential Compilation
C) Computer Integrated Sequential Compiler
D) Complex Instruction Set Computer | [] | II | CO6 |
| 8. RISC stands for _____
A) Reduce Instruction Set Computer
B) Risk Instruction Sequential Compilation
C) Risk Instruction Source Compiler
D) None of the above | [] | I | CO6 |
| 9. In CISC architecture most of the complex instructions are stored in _____
A) Register B) Diodes
C) CMOS D) Transistors | [] | I | CO6 |
| 10. Which of the following is not one of the interconnection structures?
A) Crossbar switch B) Hypercube system
C) Single port memory D) Time-shared common bus | [] | III | CO6 |

Answer All fill in the blank questions.

Marks: 6Qx1/2M = 3M

- | | | |
|---|-----|-----|
| 11. Individual control words of the micro routine are called as _____ | III | CO3 |
| 12. The Sun micro systems processors usually follow _____ architecture | III | CO5 |
| 13. MIMD stands for _____ | I | CO5 |
| 14. A crossbar switch is an interconnection between CPUs and _____. | IV | CO5 |
| 15. _____ is the process of ensuring that shared data is consistent across multiple caches in a multiprocessor system | III | CO6 |
| 16. Multiprocessors are classified as _____ | II | CO6 |

Answer All Match the following questions.

Marks: 2Qx1M = 2M

- | | | | | | | | | | | | |
|---------------------------------|---|--------------------|--|---------------------------------|--|----------------------------|--|----------------------|---|----|-----|
| 17. | <table border="1"> <tr> <td>1. Handshaking</td> <td>A. I/O interface informs the CPU that device is ready for transfer</td> </tr> <tr> <td>2. Programmed I/O</td> <td>B. Requires two control signals working in opposite directions</td> </tr> <tr> <td>3. Interrupt-initiated I/O</td> <td>C. Has local memory & control large set of I/O devices</td> </tr> <tr> <td>4. I/O processor</td> <td>D. require CPU to check the I/O flag & perform transfer</td> </tr> </table> | 1. Handshaking | A. I/O interface informs the CPU that device is ready for transfer | 2. Programmed I/O | B. Requires two control signals working in opposite directions | 3. Interrupt-initiated I/O | C. Has local memory & control large set of I/O devices | 4. I/O processor | D. require CPU to check the I/O flag & perform transfer | IV | CO5 |
| 1. Handshaking | A. I/O interface informs the CPU that device is ready for transfer | | | | | | | | | | |
| 2. Programmed I/O | B. Requires two control signals working in opposite directions | | | | | | | | | | |
| 3. Interrupt-initiated I/O | C. Has local memory & control large set of I/O devices | | | | | | | | | | |
| 4. I/O processor | D. require CPU to check the I/O flag & perform transfer | | | | | | | | | | |
| 18. | <table border="1"> <tr> <td>1. Micro Operation</td> <td>A. Specify micro operation</td> </tr> <tr> <td>2. Micro Programed control unit</td> <td>B. Improve CPU utilization</td> </tr> <tr> <td>3. Interrupts</td> <td>C. Control Memory</td> </tr> <tr> <td>4. Micro Instruction</td> <td>D. Elementary operation performed on data stored in registers</td> </tr> </table> | 1. Micro Operation | A. Specify micro operation | 2. Micro Programed control unit | B. Improve CPU utilization | 3. Interrupts | C. Control Memory | 4. Micro Instruction | D. Elementary operation performed on data stored in registers | IV | CO6 |
| 1. Micro Operation | A. Specify micro operation | | | | | | | | | | |
| 2. Micro Programed control unit | B. Improve CPU utilization | | | | | | | | | | |
| 3. Interrupts | C. Control Memory | | | | | | | | | | |
| 4. Micro Instruction | D. Elementary operation performed on data stored in registers | | | | | | | | | | |

Part – B

Answer any FOUR questions.

Marks: 4Qx5M = 20M

- | | | |
|---|----|-----|
| 19. Explain the booth's multiplication algorithm with neat sketch of hardware design. | VI | CO3 |
| 20. Explain in detail about floating point arithmetic operations | II | CO4 |
| 21. Design and explain in detail about DMA operation. | VI | CO5 |
| 22. Explain in detail about associative memory mechanisms. | II | CO5 |
| 23. Give a review on the CISC Characteristics. | V | CO6 |
| 24. Explain in detail about the Instruction Pipeline. | II | CO6 |

DEPARTMENT OF CSE-AIML

B.TECH (BR 22) MID TERM EXAMINATION QUESTION PAPER MODEL**COMPUTER ORGANIZATION & ARCHITECTURE****Time: 2Hrs****Max Marks:30****PART A(Total Marks: 10M)****Answer all the multiple-choice questions****(10×1/2M=5 M)**

		Marks	CO	BT Level
1	What is computer architecture? a) set of categories and methods that specify the functioning, organisation, and implementation of computer systems b) set of principles and methods that specify the functioning, organisation, and implementation of computer systems c) set of functions and methods that specify the functioning, organisation, and implementation of computer systems d) None of the mentione	(1/2)	L1	CO1
2	Which of the following is the subcategories of computer architecture? a) Microarchitecture b) Instruction set architecture c) Systems design d) All of the mentioned	(1/2)	L1	CO1
3	What is computer organization? a) structure and behaviour of a computer system as observed by the user b) structure of a computer system as observed by the developer c) structure and behaviour of a computer system as	(1/2)	L2	CO2

	observed by the developer d) All of the mentioned			
4	Which of the following allows simultaneous write and read operations? a) ROM b) EROM c) RAM d) None of the above	(1/2)	L1	CO3
5	The address in the main memory is known as – a) Logical address b) Physical address c) Memory address d) None of the above	(1/2)	L2	CO1
6	_____ are the different type/s of generating control signals. a) Hardwired b) Micro-instruction c) Micro-programmed d) Both Micro-programmed and Hardwire	(1/2)	L2	CO2
7	Which of the following register can interact with the secondary storage? a) PC b) MAR c) MDR d) IR	(1/2)	L2	CO1
8	The Program Counter is also called as – a) Instruction Pointer b) Data Counter c) Memory pointer d) None of the above	(1/2)	L1	CO1
9	In floating-point representation, the part represents a signed & fixed-point number is called as? a) Exponent b) Mantissa c) Normalized d) Float	(1/2)	L1	CO1

10	The signed-1's complement representation of (-14) is? a) 10001110 b) 11110010 c) 10100101 d) 11110001	(1/2)	L2	CO2
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Answer All Fill in the blanks questions

(6×1/2=3M)

		Marks	CO	BT Level
11	The communication line between the CPU, memory and other devices is called _____	1/2	L1	CO1
12	Stored program concept was introduced by _____	1/2	L2	CO2
13	CPU stands for _____	1/2	L1	CO3
14	In micro-programmed approach, the signals are generated by _____	1/2	L1	CO1
15	_____ is a general purpose processing register.	1/2	L2	CO1
16	A sequence of control words corresponding to a control sequence is called _____.	1/2	L3	CO1

Answer match the following questions

2Q×1=2 Marks

				Marks	CO	BT Level
17		List I	List II	1	L2	CO3
		a) Program counter	i) MAR			
		b) Address for memory Unit	ii) PC			
		c) Register transfer the instruction register	iii)IR			
		d) Register transfer the processor register	iv)RI			

18	a) Compute	i) Volatile memory	1	L1	CO1
	b) Central Processing unit	ii) Compiler			
	c) Random Access Memory	iii) System unit			
	d) Programming Language Translator	iv) to calculate			

PART B(Total Marks=20M)

Answer any four questions from the given six questions

4Q×5=20M

		Marks	CO	BT Level
19	Draw and explain about Micro Program Control Organization.	5	L1	CO1
20	Explain in detail about the Address Sequencing process in Micro program control unit.	5	L2	CO2
21	Explain the stored program organization with neat diagram	5	L1	CO3
22	How to construct an ALU, which perform basic arithmetic and logic operations?	5	L1	CO1
23	Draw and explain the hardware for signed – magnitude addition and subtraction.	5	L2	CO1
24	Explain in detail about floating point arithmetic operations.	5	L3	CO1

HR-22

HT.No.

D4
QC2602

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi) - Recognized under 2(f) and 12(B) of UGC Act 1956

II B.Tech. I Semester (REG & SUPPL) End Examinations, JANUARY- 2025.

(R22CSE2114) COMPUTER ORGANIZATION AND ARCHITECTURE

08/01/2025

(For CSE, CS, AIML, AIDS & DS)

Day-4(FN)

Duration: 3 Hrs**Maximum Marks: 60M**

Blooms Taxonomy : (I-Remembering, II-Understanding, III-Applying, IV-Analyzing, V-Evaluating and VI-Creating)

Course Outcomes : CO

PART - A

Answer ALL the following questions.

(10Qx1M=10M)

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|--|----|-----|
| 1. a) Distinguish among computer organization and computer architecture. | I | CO1 |
| b) What do you mean by register transfer language? | II | CO1 |
| c) What is data path in the basic processing unit or the central processor unit? | II | CO2 |
| d) Draw the diagram of micro program control unit. | V | CO2 |
| e) Distinguish between fixed point representation and floating-point representation. | I | CO3 |
| f) Explain the 2's complement with an example. | IV | CO3 |
| g) Illustrate in brief the associative mapping technique with its advantages. | V | CO4 |
| h) Compare and contrast I/O versus Memory Bus. | V | CO4 |
| i) Summarize the concept arithmetic pipeline. | VI | CO5 |
| j) Explain the characteristics of a multiprocessor. | V | CO5 |

PART - B

Answer FIVE questions choosing at least one from each unit.

(5Qx10M=50M)

UNIT-I

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|--|----|-----|
| 2a. Explain about the basic functional units of digital computers. Explain the ways of handling information by each of them. | II | CO1 |
| (OR) | | |
| 2b. Registers R1 and R2 of a computer contain the decimal values 1200 and 4600. What is the effective address of the memory operand in each of the following instructions? | II | CO1 |
| a) LOAD R5, 20(R1) | | |
| b) MOVE R5, #3000 | | |
| c) STORE 30(R1,R2), R5 | | |
| d) ADD R5, -(R2) | | |

UNIT-II

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|---|-----|-----|
| 3a. Analyze the instruction formats for zero address, one address and two address machines with appropriate examples. | III | CO2 |
| (OR) | | |
| 3b. Examine the execution of complete instruction in a micro programmed control unit with an example. | IV | CO2 |

UNIT-III

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|---|-----|-----|
| 4a. Apply booth's algorithm to multiply 15 (multiplicand) and -7(multiplier) in a step by step process. | II | CO3 |
| (OR) | | |
| 4b. Describe non-restoring division algorithm with an example. | III | CO3 |

P.T.O.

UNIT-IV

5a. Compare and contrast different mapping techniques that give correspondence between memory and cache blocks.

VI CO4

(OR)

5b. Compare and contrast typical registers in a DMA controller with a neat diagram and describe in detail how data is transferred in DMA?

IV CO

UNIT-V

6a. Analyze the pipelining processing with an example.

V CO

(OR)

6b. Distinguish between RISC and CISC. Give the characteristics of each.

VI CO

04 - AUTONOMOUS

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